RoHS

HALOGEN

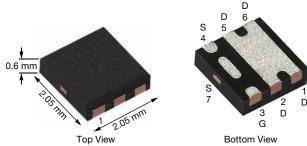
FREE

Vishay Siliconix

N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY									
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) b, c	Q _g (Typ.)						
20	0.0135 at V _{GS} = 10 V	12 ^a	5.3 nC						
	0.0185 at V _{GS} = 4.5 V	10.8	5.5 110						

Thin PowerPAK® SC-70-6L Single



Marking Code: AY **Ordering Information:**

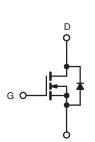
SiA430DJT-T1-GE3 (Lead (Pb)-free and halogen-free)

FEATURES

- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
 - Small footprint area
 - Ultra-thin 0.6 mm height
- 100 % R_a tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- · Load switch
- DC/DC conversion



N-Channel MOSFET

ABSOLUTE MAXIMUM RATING	S (T _A = 25 °C, u	nless otherv	wise noted)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	20	V
Gate-Source Voltage		V_{GS}	± 20	v
	T _C = 25 °C		12 ^a	
Continuous Proin Current (T = 150 °C)	T _C = 70 °C	† . !	12 ^a	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	- I _D	12 ^{a, b, c}	
	T _A = 70 °C		10.1 ^{b, c}	A
Pulsed Drain Current (t = 100 μs)		I _{DM}	40	
Continuous Source-Drain Diode Current	T _C = 25 °C		12 ^a	
Continuous Source-Drain Diode Current	T _A = 25 °C	l _S	2.9 ^{b, c}	
	T _C = 25 °C		19.2	
Maximum Payer Dissination	T _C = 70 °C		12.3	W
Maximum Power Dissipation	T _A = 25 °C	P _D	3.5 ^{b, c}	VV
	T _A = 70 °C		2.2 b, c	
Operating Junction and Storage Temperatur	T _J , T _{stg}	-55 to +150	°C	
Soldering Recommendations (Peak Tempera		260		

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum Junction-to-Ambient b, f	t ≤ 5 s	R_{thJA}	28	36	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	5.3	6.5	G/ VV				

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. See solder profile (www.vishay.com/doc?73257). The Thin PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 80 °C/W.

Document Number: 62991

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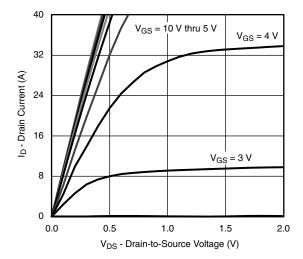
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static				•	•	ı
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050 ·· A	-	24	-	mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	1	-5.6	-	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \ \mu A$	1	-	3	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	1	-	± 100	nA
Zawa Cata Waltana Busin Commant		V _{DS} = 20 V, V _{GS} = 0 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	μΑ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20	-	-	Α
D : 0	,	V _{GS} = 10 V, I _D = 7 A	-	0.0108	0.0135	Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 5 A	-	0.0146	0.0185	
Forward Transconductance a	9 _{fs}	V _{DS} = 10 V, I _D = 7 A	-	16		S
Dynamic ^b		-				L
Input Capacitance	C _{iss}		-	800	-	
Output Capacitance	C _{oss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	200	-	pF
Reverse Transfer Capacitance	C _{rss}		-	90	-	
	Q_g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 12 A	-	12	18	nC
Total Gate Charge			-	5.3	9	
Gate-Source Charge	Q _{as}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 12 \text{ A}$	-	2	-	
Gate-Drain Charge	Q _{gd}		-	1.4	-	
Gate Resistance	Ra	f = 1 MHz	0.5	2.5	5	Ω
Turn-On Delay Time	t _{d(on)}		-	16	25	
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_L = 1 \Omega$	-	10	15	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	15	25	
Fall Time	t _f		-	10	15	
Turn-On Delay Time	· ·		-	10	15	ns
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_{I} = 1 \Omega$	-	8	15	- - -
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	17	30	
Fall Time	t _f		-	8	15	
Drain-Source Body Diode Characteristic	s			1	1	I
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	12	
Pulse Diode Forward Current (t = 100 μs)	I _{SM}	-	-	-	40	A
Body Diode Voltage			-	0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _S = 5 A, V _{GS} = 0 V	-	18	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}	1	-	7	15	nC
Reverse Recovery Fall Time	ta	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	8	-	
	a	-	_	10	_	ns

Notes

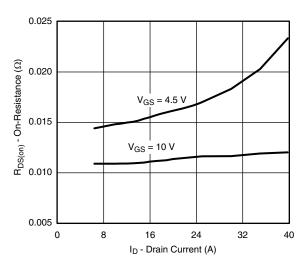
- a. Pulse test; pulse width $\leq 300 \,\mu\text{s}$, duty cycle $\leq 2 \,\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

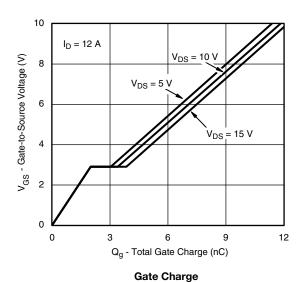


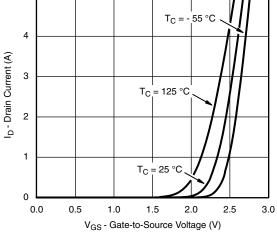


Output Characteristics

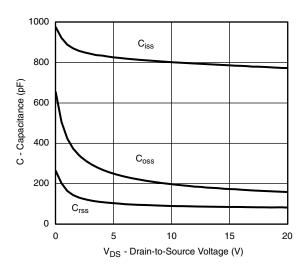


On-Resistance vs. Drain Current and Gate Voltage

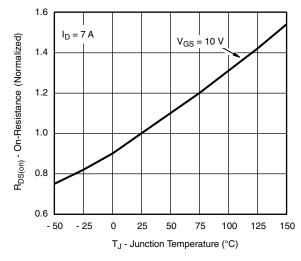




Transfer Characteristics

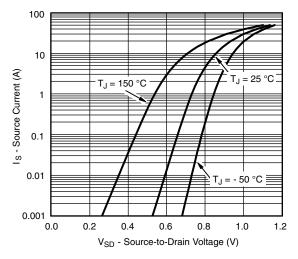


Capacitance

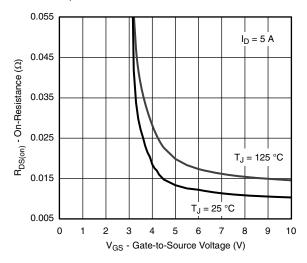


On-Resistance vs. Junction Temperature

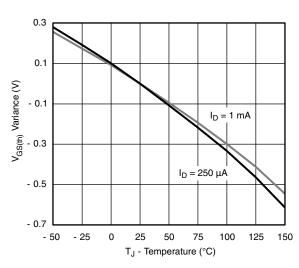




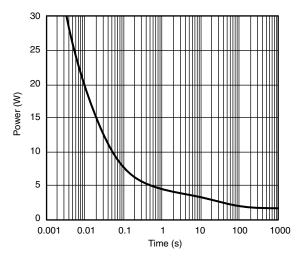
Source-Drain Diode Forward Voltage



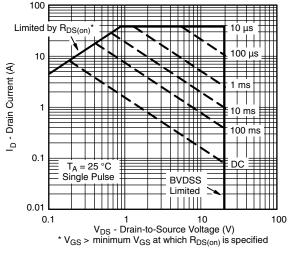
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

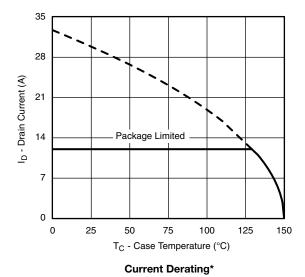


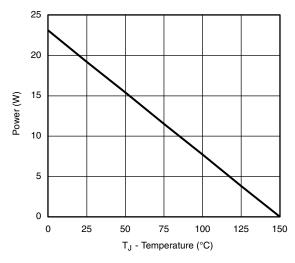
Single Pulse Power (Junction-to-Ambient)



Safe Operating Area, Junction-to-Ambient



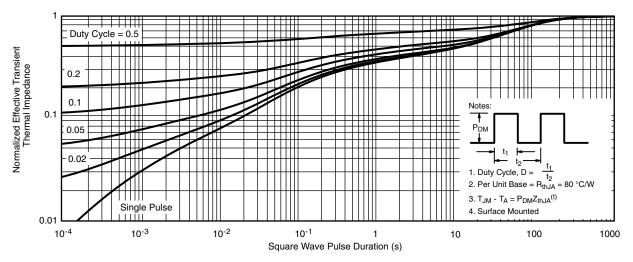




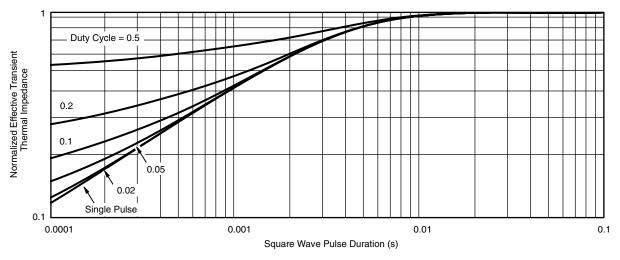
Power Derating

^{*} The power dissipation P_D is based on $T_{J \text{ (max.)}} = 150 \,^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



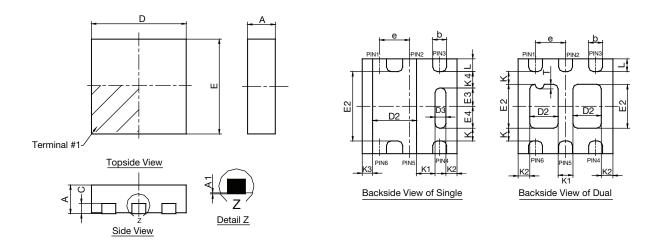
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62991.





Case Outline for PowerPAK® SC70T



DIM.	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α	0.525	0.60	0.65	0.0206	0.024	0.026	0.525	0.60	0.65	0.0206	0.024	0.026
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D2	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D3	0.135	0.235	0.335	0.005	0.009	0.013						
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E2	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E3	0.345	0.395	0.445	0.014	0.016	0.018						
E4	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC 0.026 BSC				0.65 BSC 0.026 BSC						
K	0.275 TYP.				0.011 TYP		0.275 TYP. 0.011 TYP.					
K1	0.400 TYP.				0.016 TYP.			0.320 TYP.		0.013 TYP.		
K2	0.240 TYP.				0.009 TYP.		0.252 TYP.		0.010 TYP.			
K3		0.225 TYP.		0.009 TYP.								
K4		0.355 TYP.		0.014 TYP.								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
Т							0.05	0.10	0.15	0.002	0.004	0.006

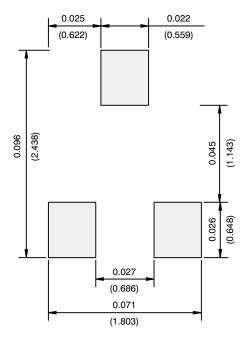
ECN: C12-0160-Rev. B, 05-Mar-12 DWG: 5994

Notes

- 1. All dimensions are in millimeter. Millimeters will govern.
- 2. Package outline exculsive of mold flash and metal burr.
- 3. Package outline inclusive of plating



RECOMMENDED MINIMUM PADS FOR SC-70: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

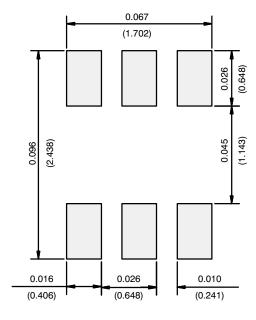
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APPLICATION NOTE

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RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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