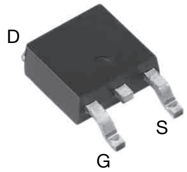
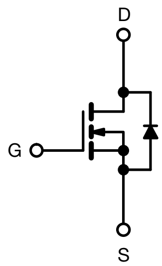
D Series Power MOSFET

DPAK (TO-252)





N-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. (Ω) at 25 °C	V_{GS} = 10 V	3.2
Q_g max. (nC)	12	
Q_{gs} (nC)	2	
Q_{gd} (nC)	3	
Configuration	Single	

FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (C_{iss})
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): R_{on} x Q_g
  - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers

ORDERING INFORMATION			
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)
Lead (Pb)-free and halogen-free	SiHD3N50D-GE3	SiHD3N50DT1-GE3	SiHD3N50DT4-GE3
	SiHD3N50DT5-GE3	SiHD3N50D-BE3	-
Lead (Pb)-free	SiHD3N50D-E3	-	-

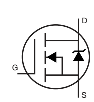
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	500	V
Gate-source voltage			V_{GS}	± 30	
Gate-source voltage AC (f > 1 Hz)				30	
Continuous drain current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	3.0	A
		T_C = 100 °C		1.9	
Pulsed drain current [a]			I_{DM}	5.5	
Linear derating factor				0.56	W/°C
Single pulse avalanche energy [b]			E_{AS}	10.4	mJ
Maximum power dissipation			P_D	69	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse diode dV/dt [d]				0.22	
Soldering recommendations (peak temperature) [c]	For 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = 3 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, starting T_J = 25 °C

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	1.8	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	500	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 250 μA	-	0.56	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	3	-	5	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 1.5 A	-	2.6	3.2	Ω
Forward transconductance [a]	g_{fs}	V_{DS} = 8 V, I_D = 1.5 A	-	1	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	175	-	pF
Output capacitance	C_{oss}		-	21	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Effective output capacitance, energy related [b]	$C_{o(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	21	-	
Effective output capacitance, time related [c]	$C_{o(tr)}$		-	26	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 1.5 A, V_{DS} = 400 V	-	6	12	nC
Gate-source charge	Q_{gs}		-	2	-	
Gate-drain charge	Q_{gd}		-	3	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 1.5 A, R_g = 9.1 Ω, V_{GS} = 10 V	-	12	24	ns
Rise time	t_r		-	9	18	
Turn-off delay time	$t_{d(off)}$		-	11	22	
Fall time	t_f		-	13	26	
Gate input resistance	R_g	f = 1 MHz, open drain	-	3.3	-	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse P - N junction diode 	-	-	3	A
Pulsed diode forward current	I_{SM}		-	-	12	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 1.5 A, V_{GS} = 0 V	-	-	1.2	V
Reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S = 1.5 A, dI/dt = 100 A/μs, V_R = 20 V	-	293	-	ns
Reverse recovery charge	Q_{rr}		-	0.74	-	μC
Reverse recovery current	I_{RRM}		-	5	-	A

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
c. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

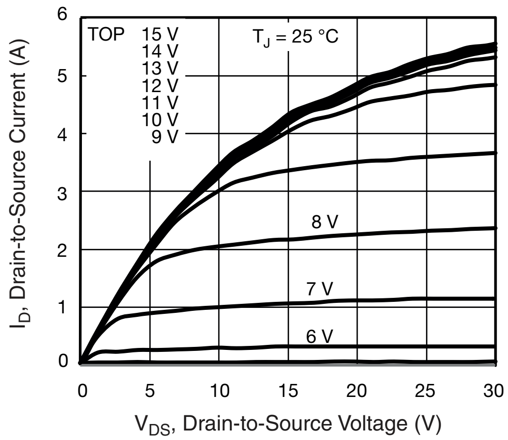


Fig. 1 - Typical Output Characteristics

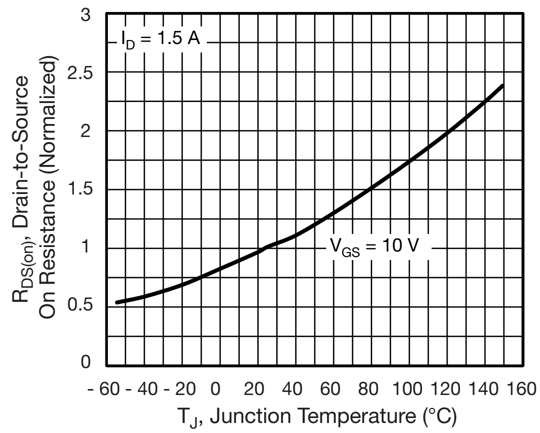


Fig. 4 - Normalized On-Resistance vs. Temperature

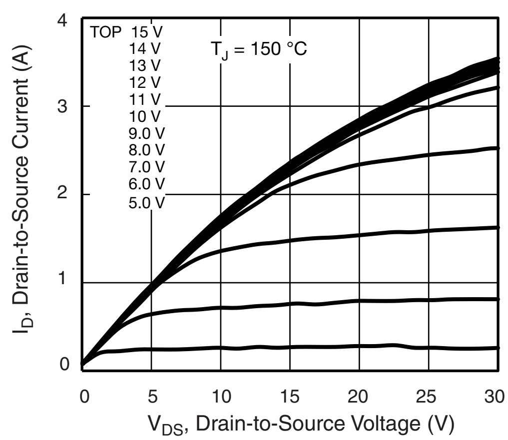


Fig. 2 - Typical Output Characteristics

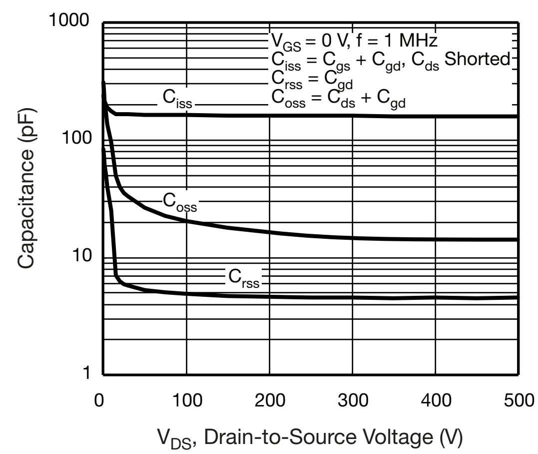


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

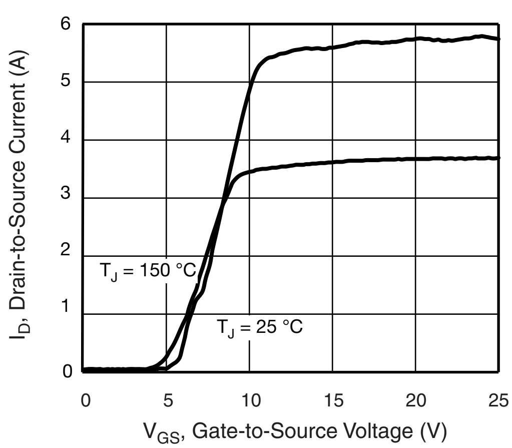


Fig. 3 - Typical Transfer Characteristics

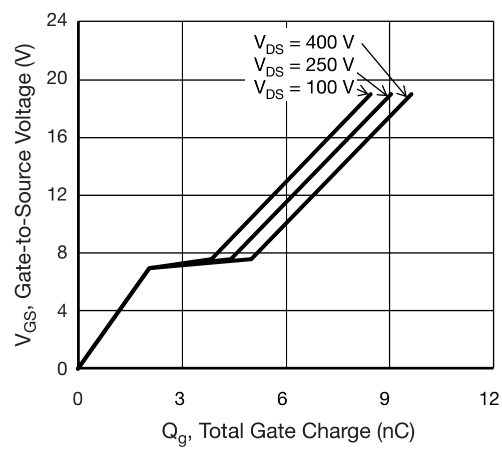


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

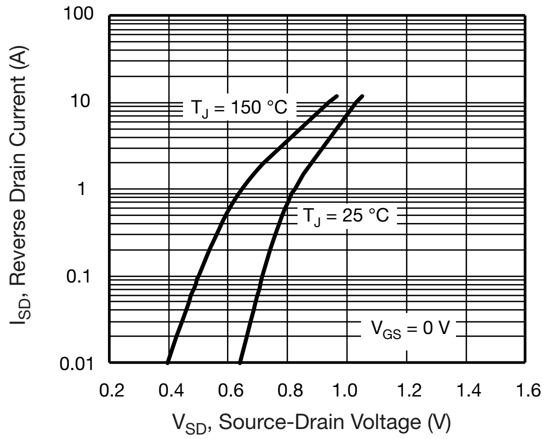


Fig. 7 - Typical Source-Drain Diode Forward Voltage

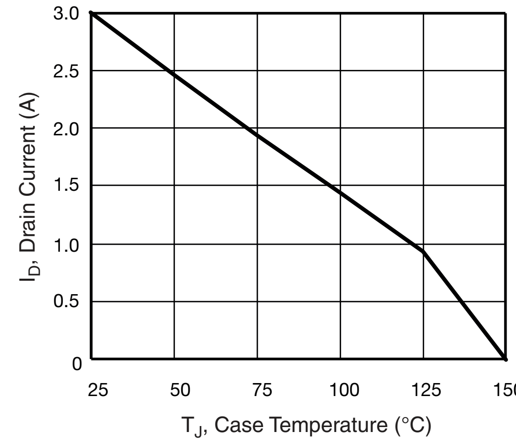


Fig. 9 - Maximum Drain Current vs. Case Temperature

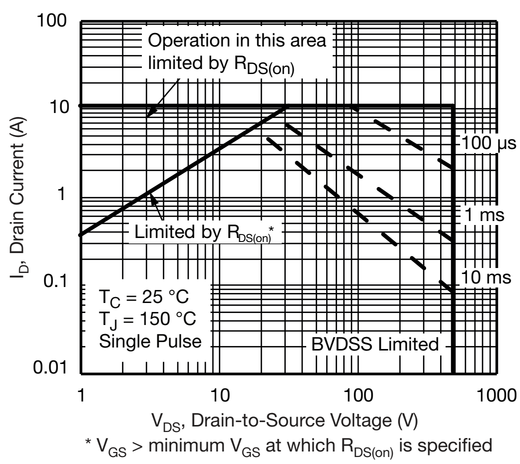


Fig. 8 - Maximum Safe Operating Area

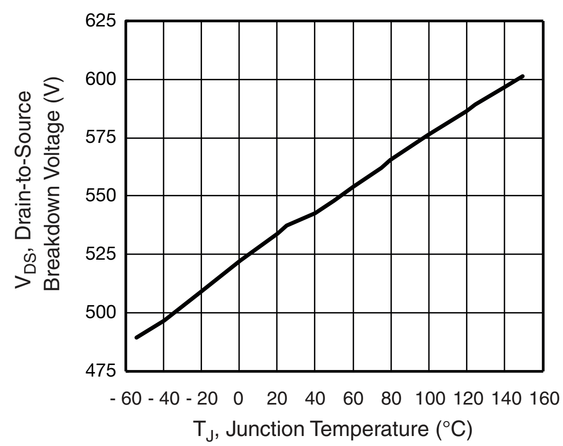


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

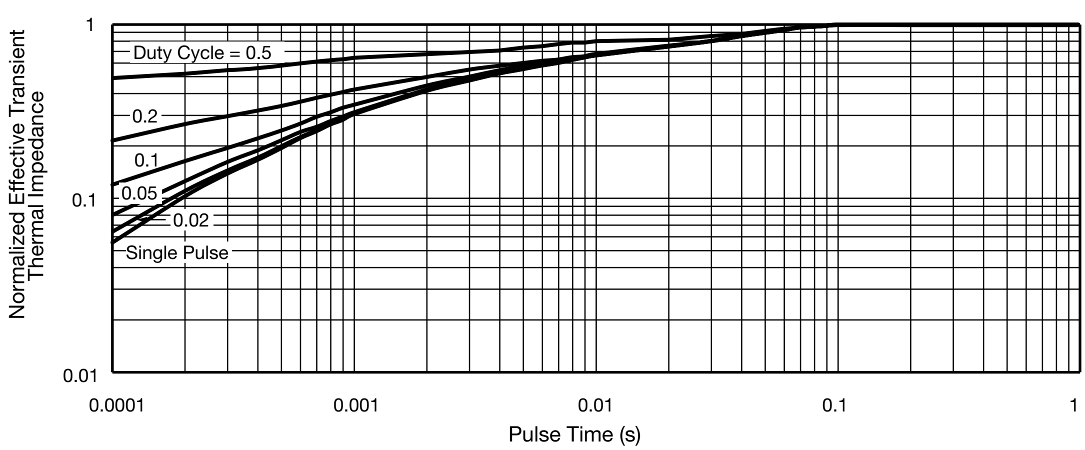


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

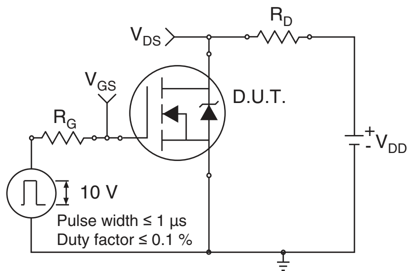


Fig. 12 - Switching Time Test Circuit

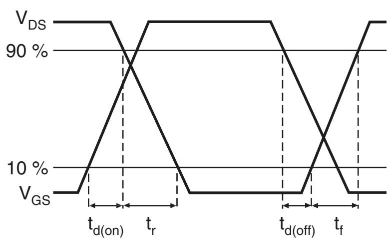


Fig. 13 - Switching Time Waveforms

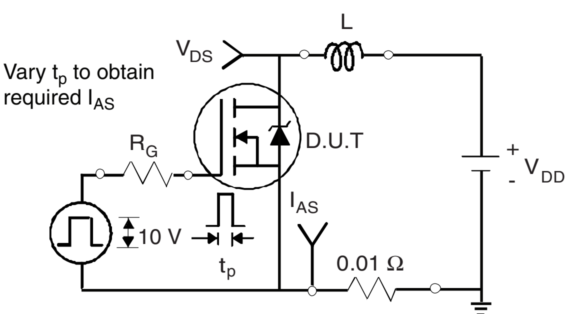


Fig. 14 - Unclamped Inductive Test Circuit

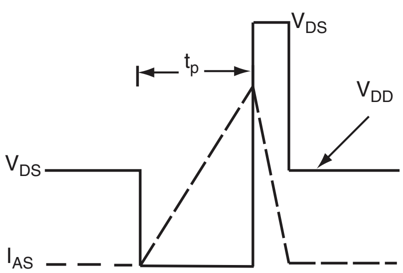


Fig. 15 - Unclamped Inductive Waveforms

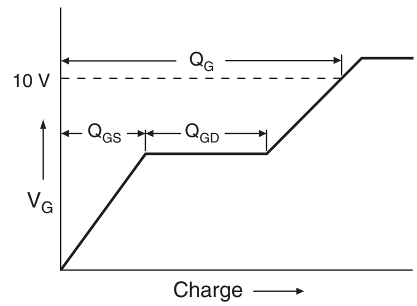


Fig. 16 - Basic Gate Charge Waveform

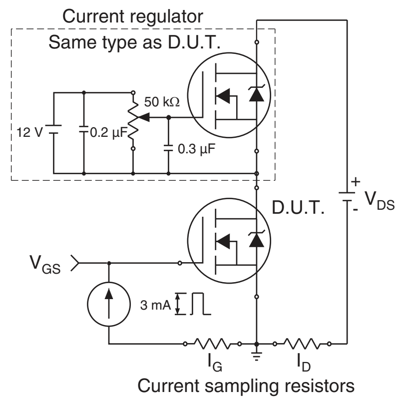
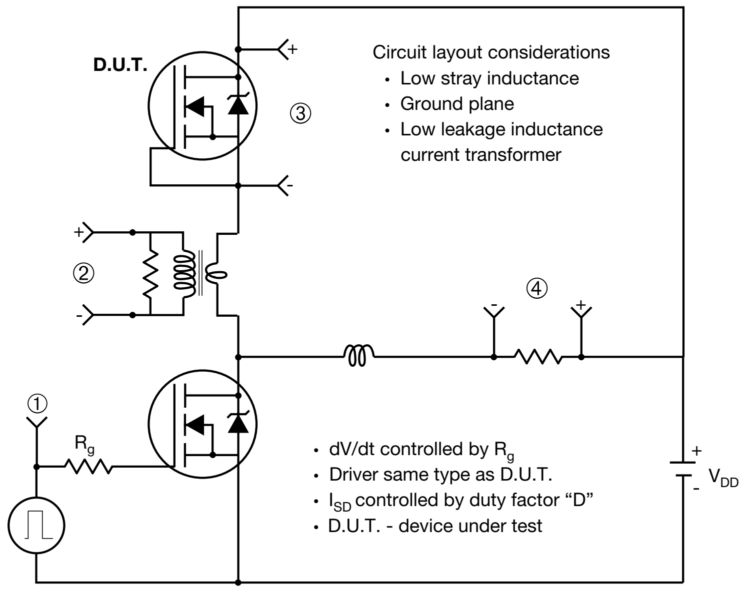
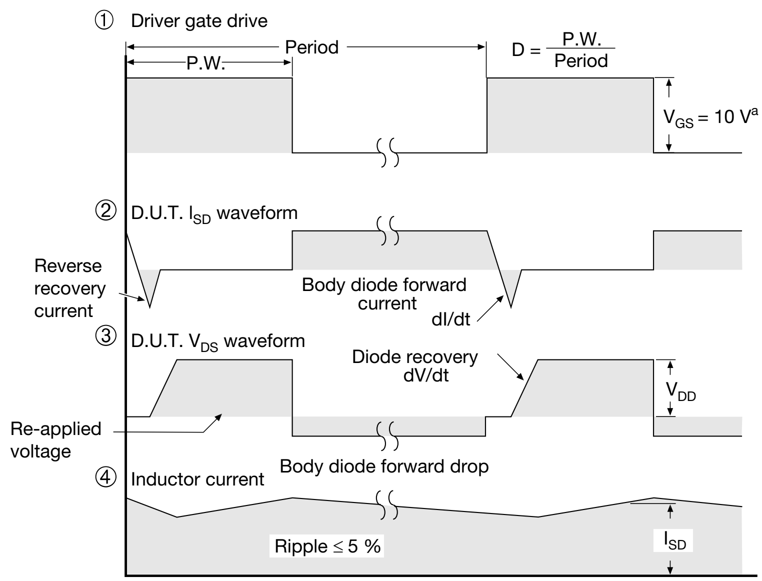


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

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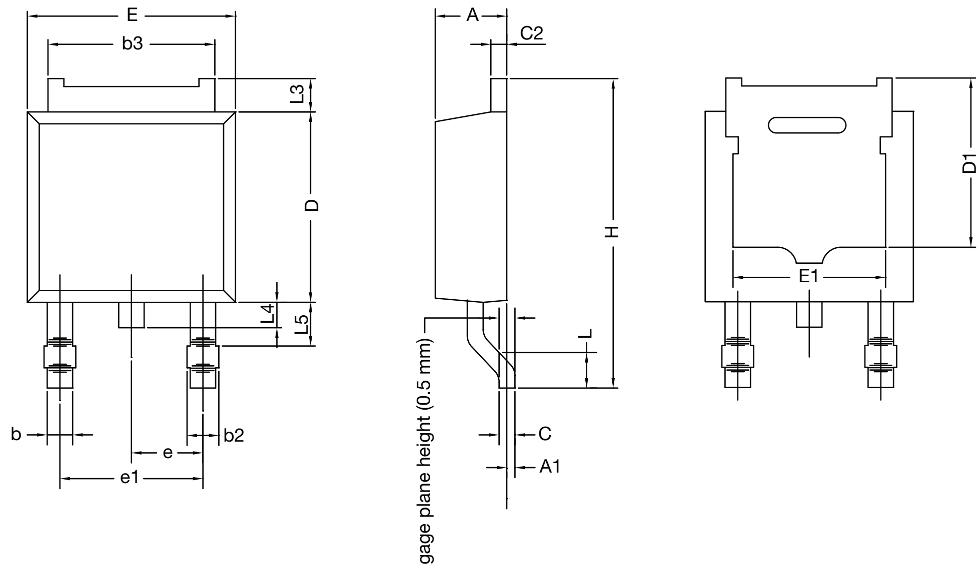
TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y

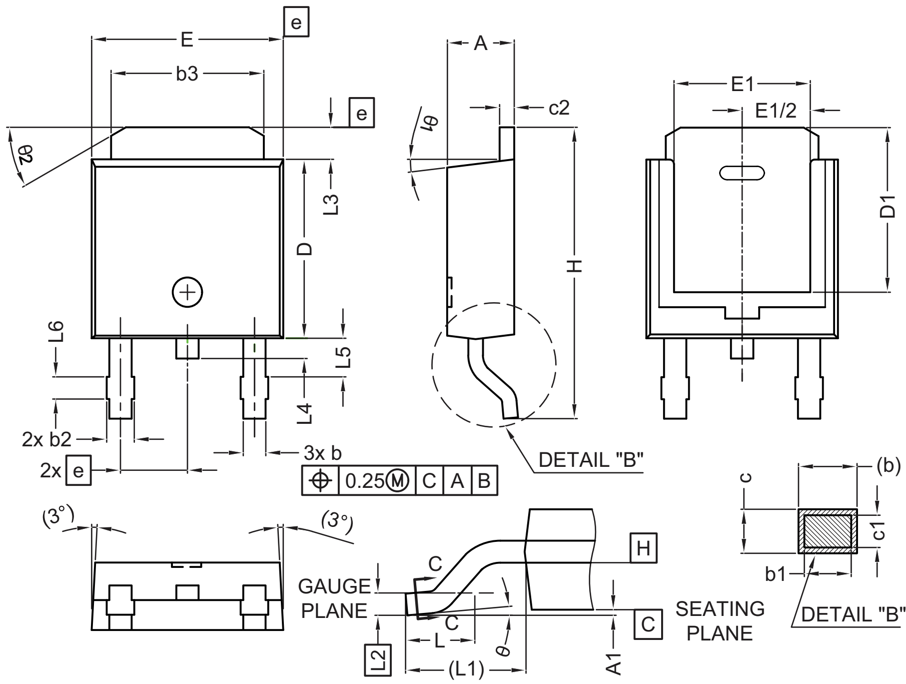


	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only

VERSION 2: FACILITY CODE = N



	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

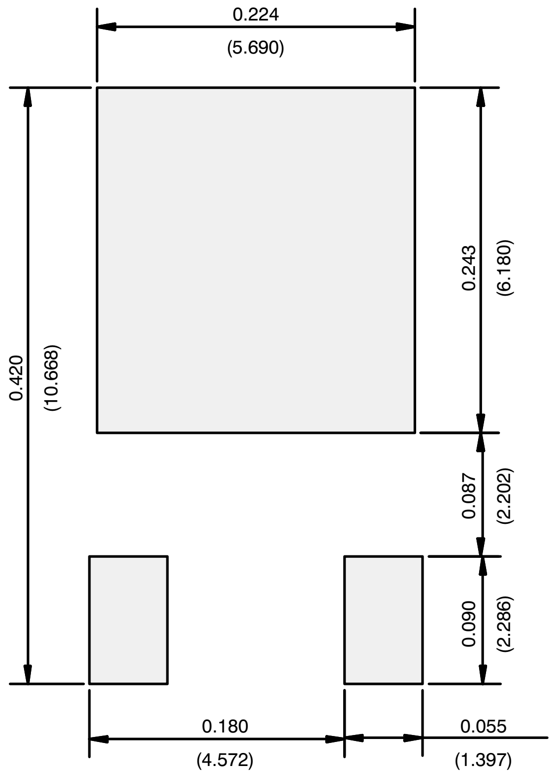
	MILLIMETERS	
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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