Powered-off Protection, High Speed, 1.65 V to 5.5 V, SPDT Analog Switch (2:1 Multiplexer / Demultiplexer Bus Switch)

DESCRIPTION

The DG3157E is a high speed single-pole double-throw analog switch designed for +1.65 V to +5.5 V single power rail operation.

Fabricated with high density CMOS technology, the DG3157E achieves low on-resistance, fast switching speed, and high bandwidth while maintains low power consumption.

The DG3157E can handle both analog and digital signals and permits signals with amplitudes of up to V+ to be transmitted in either direction.

When the select pin is low, B_0 is connected to the output A pin. When the select pin is high, B_1 is connected to the output A pin. The path that is open will have a high impedance state with respect to the output. Break before make switching performance is guaranteed.

A powered-off protection circuit is built into the switch to prevent an abnormal current flow from COM pin to V+ during the power-down condition. Each output pin can withstand greater than 7 kV (human body model).

Operation temperature is specified from -40 °C to +85 °C. The DG3157E is available in the compact SC-70-6L package.

FEATURES

- Direct cross to industry standard SN74LVC1G3157, NC7SB3157, NLASB3157, PI5A3157, and STG3157
- Low switch on-resistance (6 Ω)
- +1.65 V to +5.5 V single supply operation
- Powered-off protection
- Control logic inputs can go over V+ up to 5.5 V
- Low parasitic capacitance, 7 pF at switch off
- Break before make switching
- Latch-up performance exceeds 200 mA per JESD 78
- High ESD rating
  - 7000 V human body model (JS-001)
  - 1000 V charge device model (JS-002)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

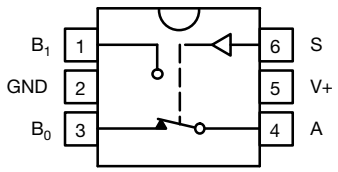
HALOGEN FREE

APPLICATIONS

- Battery powered devices
- Consumer and computing
- Instrumentation
- Medical equipment
- Control and automation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

SC-70
6-Pin



Top view

Device marking: H0

TRUTH TABLE	
LOGIC INPUT (S)	FUNCTION
0	B_0 connected to A
1	B_1 connected to A

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	SC-70-6	DG3157EDL-T1-GE3 (halogen-free)

ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
V+, A, B_0, B_1, S reference to GND		-0.3 to 6	V
Continuous current (any terminal)		± 50	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage temperature	D suffix	-65 to +150	°C
Power dissipation (packages) [a]	6-pin SC-70 [b]	250	mW
ESD / HBM	JS-001	7000	V
ESD / CDM	JS-002	1000	
Latch up	Per JESD78 with 1.5 x V_{abs} max. clamp	200	mA

Notes
a. All leads welded or soldered to PC board
b. Derate 3.1 mW/°C above 70 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V_S = 0.25 V+ or 0.75 V+, V+ = 1.65 V to 1.95 V [e] V_S = 0.2 V+ or 0.65 V+, V+ = 2.3 V to 5.5 V [e]		TEMP. [a]	LIMITS -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
DC Characteristics								
High level input voltage	V_{SH}	V+ = 1.65 V to 1.95 V		Full	0.75 V+	-	-	V
		V+ = 2.3 V to 5.5 V		Full	0.65 V+	-	-	
Low level input voltage	V_{SL}	V+ = 1.65 V to 1.95 V		Full	-	-	0.25 V+	
		V+ = 2.3 V to 5.5 V		Full	-	-	0.2 V+	
On resistance	R_{ON}	V+ = 4.5 V	V_{BN} = 0 V, I_A = 30 mA	Full	-	8	11	Ω
			V_{BN} = 2.3 V, I_A = -30 mA	Full	-	6	9	
			V_{BN} = 4.5 V, I_A = -30 mA	Full	-	7	9	
		V+ = 3 V	V_{BN} = 0 V, I_A = 24 mA	Full	-	10	14	
			V_{BN} = 3 V, I_A = -24 mA	Full	-	9	12	
		V+ = 2.3 V	V_{BN} = 0 V, I_A = 8 mA	Full	-	13	18	
			V_{BN} = 2.3 V, I_A = -8 mA	Full	-	12	16	
		V+ = 1.65 V	V_{BN} = 0 V, I_A = 4 mA	Full	-	20	26	
			V_{BN} = 1.65 V, I_A = -4 mA	Full	-	18	23	
On resistance flatness	R_{FLAT}	0 < V_{BN} < V+	V+ = 4.5 V, I_A = -30 mA	Room	-	2	-	
			V+ = 3 V, I_A = -24 mA	Room	-	4	-	
			V+ = 2.3 V, I_A = -8 mA	Room	-	10	-	
			V+ = 1.65 V, I_A = -4 mA	Room	-	58	-	
On resistance matching between channels	ΔR_{ON}	V+ = 4.5 V, V_{BN} = 3.15 V, I_A = -30 mA		Room	-	0.09	-	
		V+ = 3 V, V_{BN} = 2.1 V, I_A = -24 mA		Room	-	0.13	-	
		V+ = 2.3 V, V_{BN} = 1.6 V, I_A = -8 mA		Room	-	0.15	-	
		V+ = 1.65 V, V_{BN} = 1.15 V, I_A = -4 mA		Room	-	0.16	-	
Input leakage current	I_S	V+ = 5.5 V, V_S = 5.5 V		Room	-0.1	-	0.1	µA
				Full	-1	-	1	
Off stage switch leakage	$I_{BN(off)}$	V+ = 5.5 V, V_A = 1 V / 4.5 V, V_B = 4.5 V / 1 V		Room	-0.1	-	0.1	
				Full	-1	-	1	
On state switch leakage	$I_{BN(on)}$	V+ = 5.5 V, V_A = V_B = 1 V or 4.5 V		Room	-0.1	-	0.1	
				Full	-1	-	1	
Power down leakage	I_{PD}	V+ = 0 V, V_A = 5 V, B_0, B_1 open, V_S = GND		Full	-	-	5	
		V+ = 0 V, V_{B0}, V_{B1} = 5 V, A open, V_S = GND		Full	-	-	5	
Power Supply								
Power supply range	V+			Full	1.65	-	5.5	V
Quiescent supply current	I+	V+ = 5.5 V, V_S = V+ or GND		Room	-	-	1	µA
				Full	-	-	5	

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V_S = 0.25 V+ or 0.75 V+, V+ = 1.65 V to 1.95 V [e] V_S = 0.2 V+ or 0.65 V+, V+ = 2.3 V to 5.5 V [e]		TEMP. [a]	LIMITS -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
AC Electrical Characteristics [e]								
Prop delay time [f]	t_{PHL}/t_{PLH}	V_A = 0 V, see Fig. 3	V+ = 1.65 V to 1.95 V	Full	-	4	-	ns
			V+ = 2.3 V to 2.7 V	Full	-	3	-	
			V+ = 3 V to 3.6 V	Full	-	2	-	
			V+ = 4.5 V to 5.5 V	Full	-	2	-	
Output enable time [f]	t_{PZL}/t_{PZH}	V_{LOAD} = 2 x V+ for t_{PZL}, V_{LOAD} = 0 V for t_{PZH}, see Fig. 4	V+ = 1.65 V to 1.95 V	Room	-	32	-	
				Full	-	34	-	
			V+ = 2.3 V to 2.7 V	Room	-	22	-	
				Full	-	23	-	
			V+ = 3 V to 3.6 V	Room	-	19	-	
				Full	-	20	-	
			V+ = 4.5 V to 5.5 V	Room	-	16	-	
				Full	-	16	-	
Output disable time [f]	t_{PLZ}/t_{PHZ}	V_{LOAD} = 2 x V+ for t_{PLZ}, V_{LOAD} = 0 V for t_{PHZ}, see Fig. 4	V+ = 1.65 V to 1.95 V	Room	-	22	-	
				Full	-	23	-	
			V+ = 2.3 V to 2.7 V	Room	-	18	-	
				Full	-	19	-	
			V+ = 3 V to 3.6 V	Room	-	16	-	
				Full	-	16	-	
			V+ = 4.5 V to 5.5 V	Room	-	13	-	
				Full	-	14	-	
Break-before-make time [d]	t_{BBM}	V+ = 1.65 V to 1.95 V		Full	0.5	-	-	
		V+ = 2.3 V to 2.7 V		Full	0.5	-	-	
		V+ = 3 V to 3.65 V		Full	0.5	-	-	
		V+ = 4.5 V to 5.5 V		Full	0.5	-	-	
Charge injection [d]	Q	C_L = 0.1 nF, V_{GEN} = 0 V R_{GEN} = 0 Ω	V+ = 5 V	Room	-	1.3	-	pC
			V+ = 3.3 V	Room	-	0.5	-	
Analog Switch Characteristics								
Off isolation [d]	OIRR	R_L = 50 Ω, f = 10 MHz		Room	-	-61	-	dB
Crosstalk [d]	X_{TALK}			Room	-	-61	-	
-3 dB bandwidth [d]	BW	R_L = 50 Ω		Room	-	580	-	MHz
Capacitance								
Control pin capacitance [d]	C_{IN}	V+ = 0 V		Room	-	6	-	pF
B port off capacitance [d]	C_{IO-B}	V+ = 5 V		Room	-	7	-	
A port capacitance when switch enable [d]	$C_{IO-A(on)}$			Room	-	12	-	

Notes

a. Room = 25 °C, full = as determined by the operating suffix
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
c. Typical values are for design aid only, not guaranteed nor subject to production testing
d. Guarantee by design, nor subjected to production test
e. V_S = input voltage to perform proper function
f. Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch

LOGIC DIAGRAM POSITIVE LOGIC

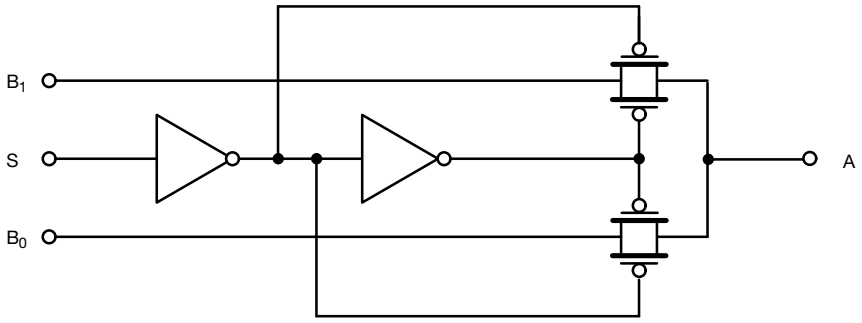
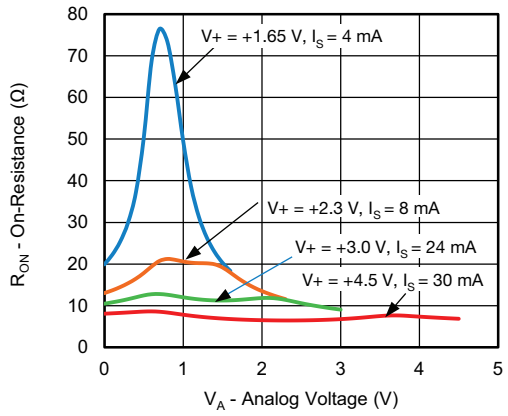
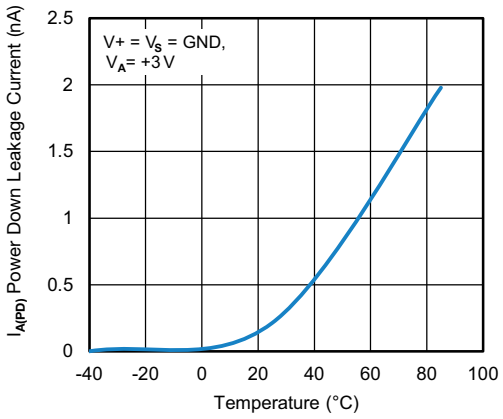


Fig. 1

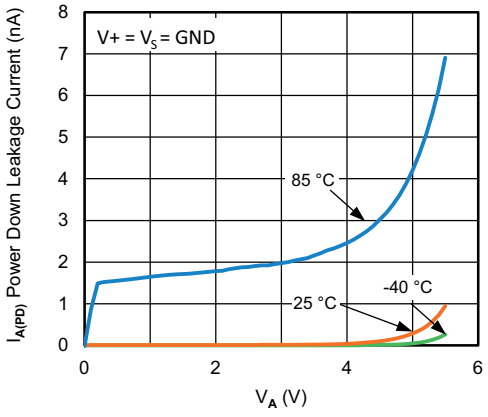
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



R_{ON} vs. V_A vs. V+

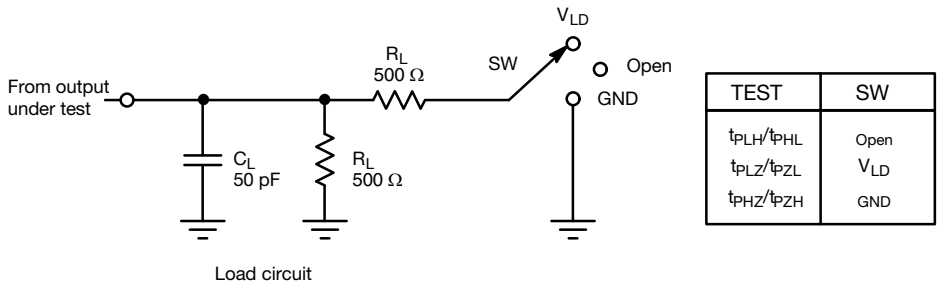


Power Down Leakage Current vs. Temperature



Power Down Leakage Current vs. V_A

AC LOADING AND WAVEFORMS



TEST	SW
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LD}
t_{PHZ}/t_{PZH}	GND

Fig. 2 - AC Test Circuit

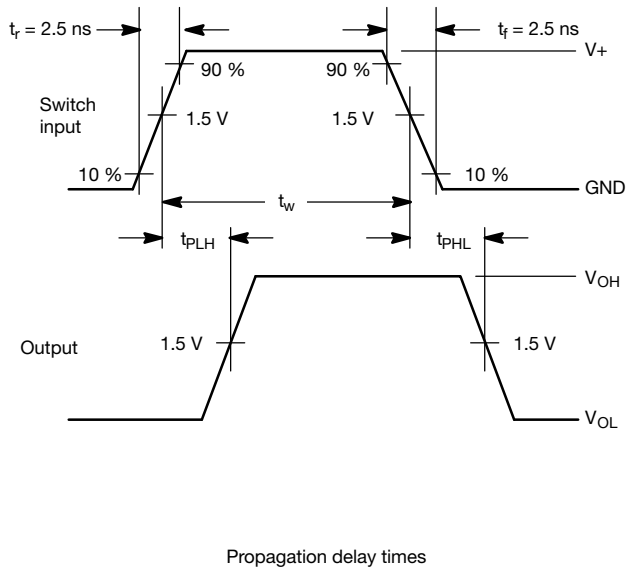


Fig. 3 - AC Waveforms

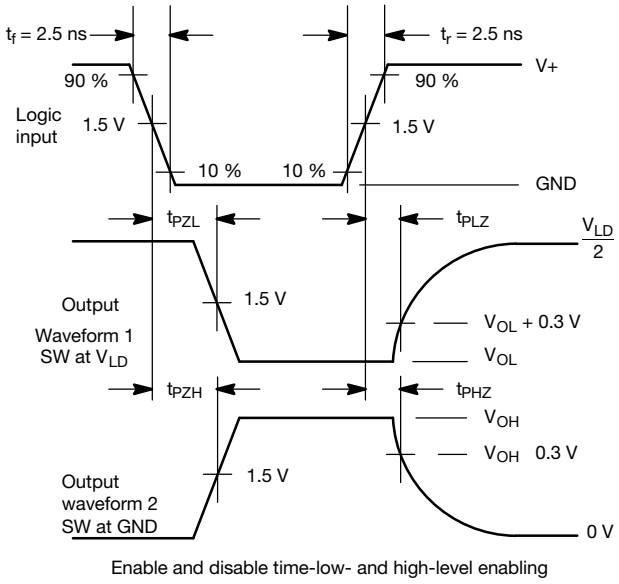
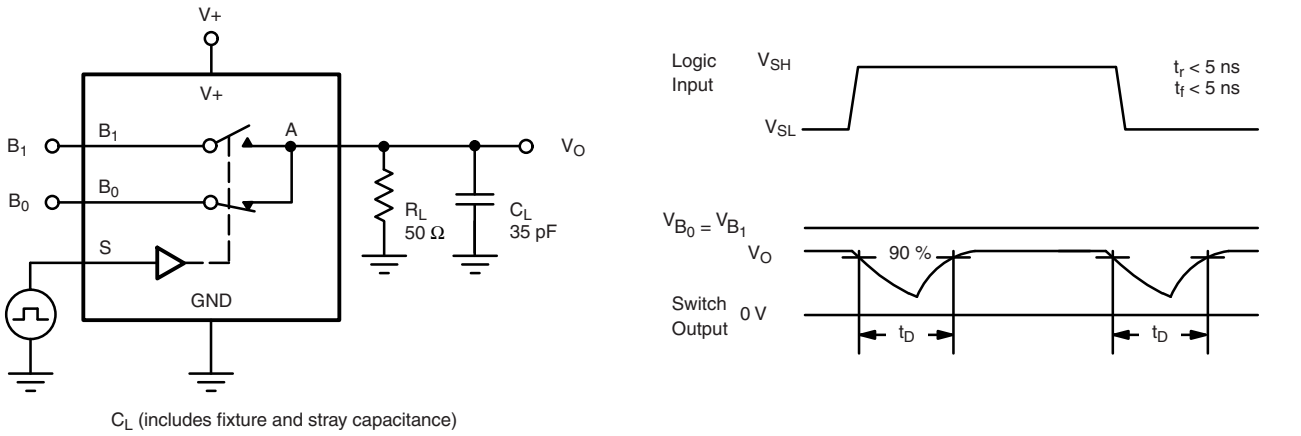


Fig. 4 - AC Waveforms

Notes

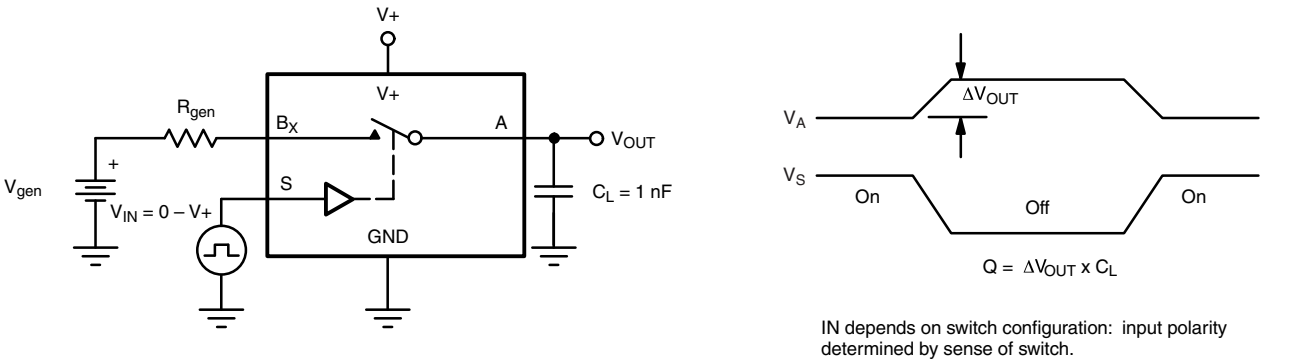
- C_L includes probe and jig capacitance
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω
- The outputs are measured one at a time with one transition per measurement
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{dis}
- t_{PLH} and t_{PHL} are the same as t_{dis}
- V_{LD} = 2 V+

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Fig. 5 - Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 6 - Charge Injection

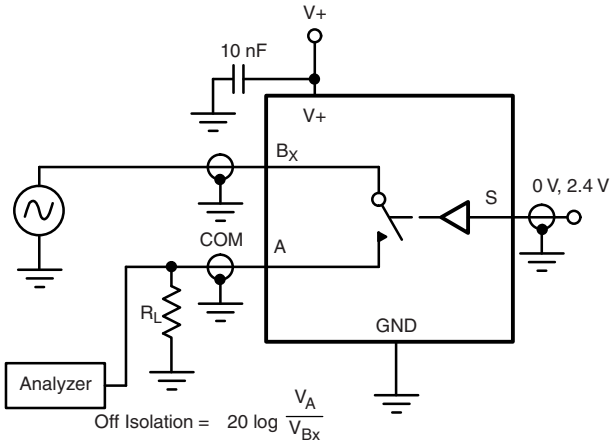


Fig. 7 - Off-Isolation

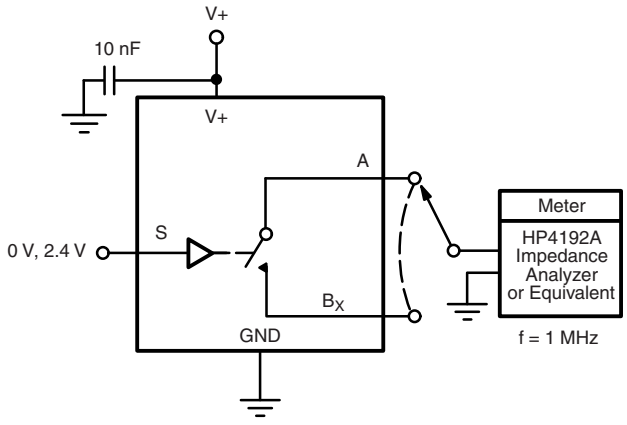


Fig. 8 - Channel Off/On Capacitance

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