Programmable Duty Cycle Controller

DESCRIPTION

The Si9118/Si9119 are a BiC/DMOS current-mode pulse width modulation (PWM) controller ICs for high-frequency dc/dc converters. Single-ended topologies (forward and flyback) can be implemented at frequencies up to 1 MHz. The controller operates in constant frequency mode during the full load and automatically switches to pulse skipping mode under light load to maintain high efficiency throughout the full load range. The maximum duty cycle is easily programmed with a resistor divider for optimum control.

The push-pull output driver provides high-speed switching to external MOSPOWER devices large enough to supply 50 W of output power. Shoot-through current for internal push-pull stage is almost eliminated to minimize quiescent supply current.

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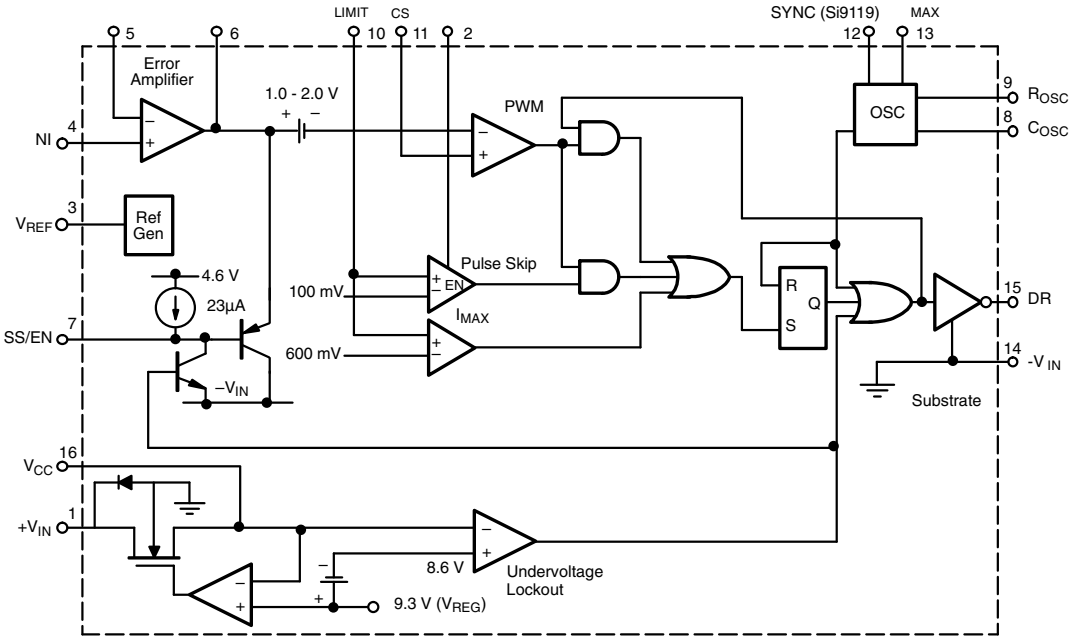
The high-voltage DMOS transistor permits direct operation from bus voltages of up to 200 V. Other features include a 1.5 % accurate voltage reference, 2.7 MHz bandwidth error amplifier, standby mode, soft-start and undervoltage lockout circuits.

The Si9118/Si9119 are available in both standard and lead (Pb)-free packages.

FEATURES

- 10 to 200 V Input Range
- Current-Mode Control
- Internal Start-Up Circuit
- Buffer Slope Compensation Voltage
- Soft-Start
- 2.7 MHz Error Amp
- 500 mA Output Drive Current
- Light Load Frequency Fold-Back
- Low Quiescent Current
- Programmable Maximum Duty Cycle, with 80 % as Default

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Parameter	**Symbol**	**Limit**	**Unit**
Voltage Reference V_{CC} to V_{IN}		18	V
$+V_{IN}$ (Note: V_{CC} < + V_{IN} + 0.3 V)		200	
Logic Input (SYNC)		- 0.3 to V_{cc} + 0.3	
Linear Input (FB, I_{CS}, I_{LIMIT}, SS/EN)		- 0.3 to V_{cc} + 0.3	
HV Pre-Regulator Input Current (continuous)		5	mA
Storage Temperature		- 65 to 150	°C
Operating Temperature		- 40 to 85	
D_{MAX}		3.2	V
Junction Temperature (T_J)		150	°C
Power Dissipation (Package)[a] 16-Pin SOIC (Y Suffix)[b]		900	mW
Thermal Impedance (θ_{JA}) 16-Pin SOIC		140	°C/W

Notes:
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25 °C.

* *Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.*

RECOMMENDED OPERATING RANGE		
Parameter	**Limit**	**Unit**
Voltage Reference V_{cc} to V_{IN}	10 to 16.5	V
$+V_{IN}$	10 to 200	
f_{OSC}	40 kHz to 1 MHz	
R_{OSC}	56 kΩ to 1 MΩ	
C_{OSC}	47 to 200	pF
Linear Inputs	0 to V_{cc} - 4	V
Digital Inputs	0 to V_{cc}	V

SPECIFICATIONS							
		Test Conditions Unless Otherwise Specified - V_{IN} = 0 V, V_{CC} = 10 V	**Limits** D Suffix - 40 to 85 °C				
Parameter	**Symbol**		**Temp.[a]**	**Min.**	**Typ.[b]**	**Max.**	**Unit**
Reference							
Output Voltage	V_{REF}	OSC Disabled, T_A = 25 °C	Room	3.94	4.0	4.06	V
		OSC Disabled, Over Voltage and Temperature Ranges[c]	Full	3.88	4.0	4.12	
Short Circuit Current	I_{SREF}	V_{REF} = -V_{IN}			- 30	- 5	mA
Load Regulation	$\Delta V_R/\Delta I_R$	I_{REF} = 0 to - 1mA			10	40	mV

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified - V_{IN} = 0 V, V_{CC} = 10 V	Limits D Suffix - 40 to 85 °C Temp.[a]	Min.	Typ.[b]	Max.	Unit
Oscillator							
Initial Accuracy[d]	f_{OSC}	R_{OSC} = 374 kΩ, C_{OSC} = 200 pF		90	100	110	kHz
	f_{OSC}[c]	R_{OSC} = 70 kΩ, C_{OSC} = 200 pF		450	500	550	
Voltage Stability[c]	Δf/f	R_{OSC} = 70 kΩ, C_{OSC} = 200 pF Δf/f = [f(16.5 V) - f(9.5 V)] / f(9.5 V)			1	2	%
Temperature Coefficient[c]	OSC TC	- 40 ≤ T_A ≤ 85 °C, f_{OSC} = 100 kHz			200	500	ppm/°C
Sync High Pulse Width (Si9119)				200			ns
Sync Low Pulse Width (Si9119)				200			
Sync Rise/Fall Time (Si9119)						200	
Sync Logic Low (Si9119)	V_{IL}					0.8	V
Sync Logic High (Si9119)	V_{IH}			4			
Sync Range[c] (Si9119)	f_{EXT}			1.05 x f_{OSC}			kHz
PWM/$\overline{PSM}$							
PWM/$\overline{PSM}$ Logic High	V_{IH}			4			V
PWM/$\overline{PSM}$ Logic Low	V_{IL}					0.8	
D_{MAX}							
Accuracy		f_{OSC} = 100 kHz with 1 % Resistor			± 10		%
Error Amplifier (OSC Disabled)							
Input BIAS Current	I_{FB}	V_{FB} = 5 V, NI = V_{REF}			< 1.0	± 200	nA
Input OFFSET Voltage	V_{OS2}				± 5	± 25	mV
Open Loop Voltage Gain[c]	A_{VOL}			65	80		dB
Unity Gain Bandwidth[c]	BW			1.8	2.7		MHz
Output Current	I_{OUT}	Source (V_{FB} = 3.5 V, NI = V_{REF})		- 1.0	- 2.7		mA
		Sink (V_{FB} = 4.5 V, NI = V_{REF})		1.0	2.4		
Power Supply Rejection	PSRR	10 V ≤ V_{CC} ≤ 16.5 V		50	80		dB
Pre-Regulator/Start-up							
Input Voltage[c]	$+V_{IN}$	I_{IN} = 10 µA	Room	200			V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = V_{ULVO}	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE\_REGULATOR}$ = 15 µA	Room	8.7	9.3	9.8	V
Undervoltage Lockout	V_{UVLO}		Room	8.0	8.6	9.3	
V_{REG} - V_{UVLO}	V_{DELTA}		Room	0.3	0.7		
Supply							
Supply Current	I_{CC}	C_{LOAD} ≤ 50 pF, f_{OSC} = 100 kHZ			1.9	3.0	mA

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified - V_{IN} = 0 V, V_{CC} = 10 V	Limits D Suffix - 40 to 85 °C Temp.[a]	Min.	Typ.[b]	Max.	Unit
Protection							
Current Limit Treshold Voltage	$V_{I(Limit)}$	V_{FB} = 0, NI = V_{REF}		0.5	0.6	0.7	V
Current Limit Delay to Output[c]	t_d	V_{SENSE} 0.85 V, See Figure 1			77	100	ns
Soft-Start Current	I_{SS}			- 12	- 23	- 30	µA
Output Inhibit Voltage	$V_{SS(off)}$	Soft-Start Voltage to Disable Driver Output		0.5	1.26		V
Pulse Skipping Threshold Voltage	V_{PS}			80	100	120	mV
Mosfet Driver							
Output High Voltage	V_{OH}	I_{OUT} = - 10 mA	Room Full	V_{CC} - 0.3 V_{CC} - 0.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.3 0.5	
Output Resistance[c]	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full		20 25	30 50	Ω
Rise Time[c]	t_r	C_L = 500 pF	Room		40	75	ns
Fall Time[c]	t_r		Room		40	75	

Notes:
a. Room = 25 °C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Guaranteed by design, not subject to production test.
d. $C_{STRAY} \leq 5$ pF on C_{OSC}

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING WAVEFORMS

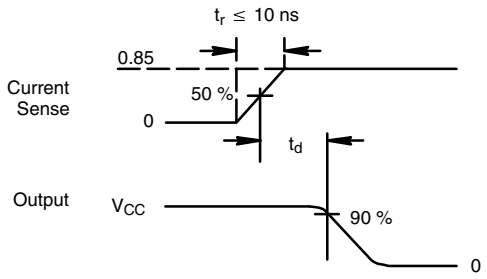
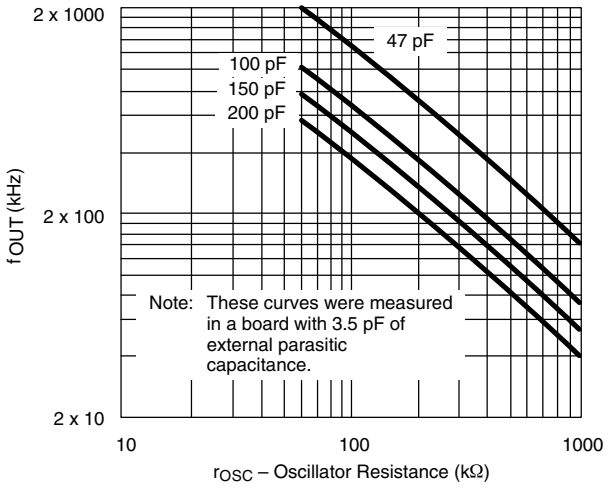
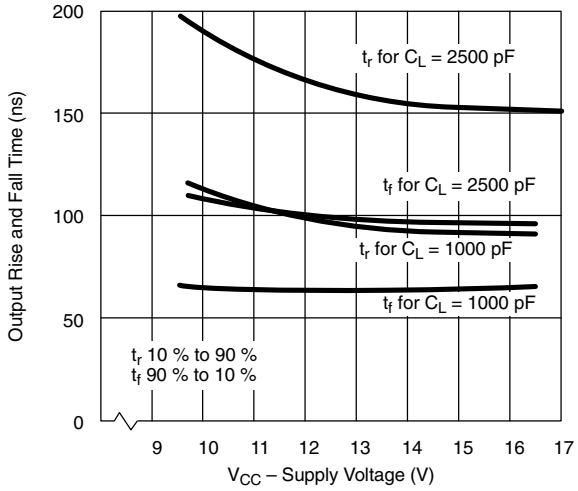


Figure 1.

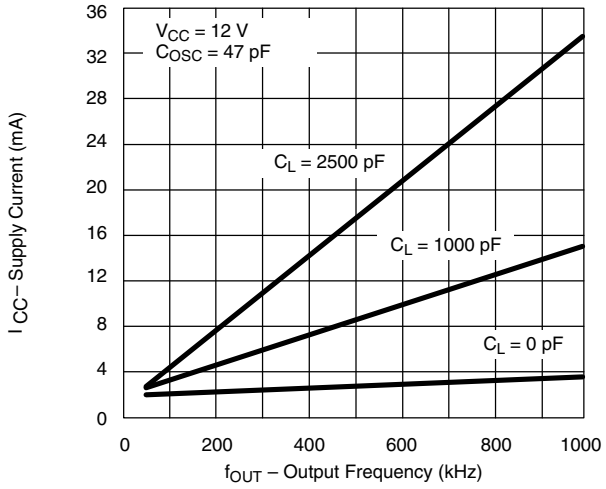
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless noted)



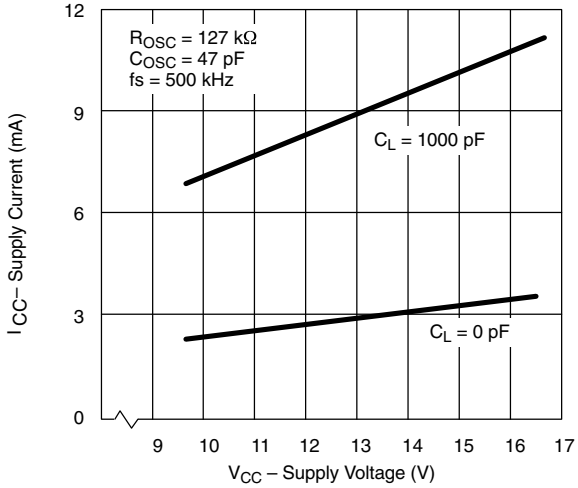
Oscillator Frequency



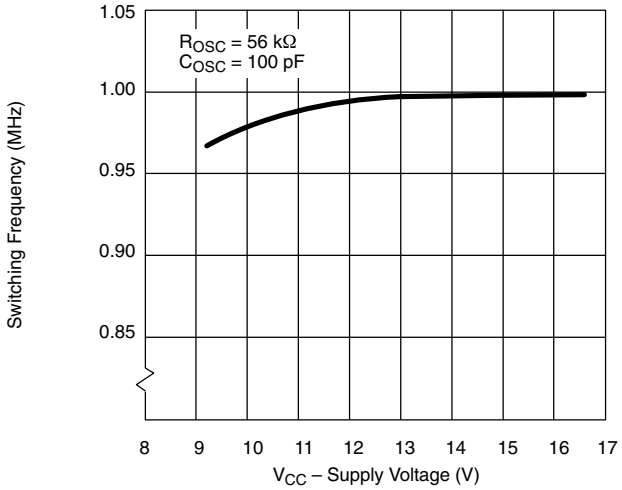
Output Driver Rise and Fall Time



Supply Current vs. Output Frequency

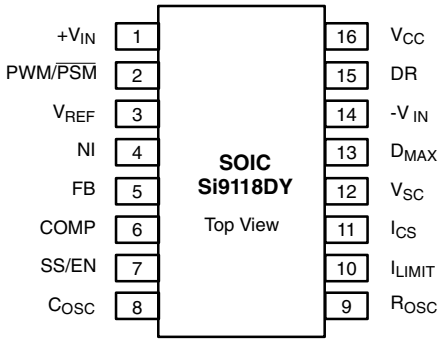


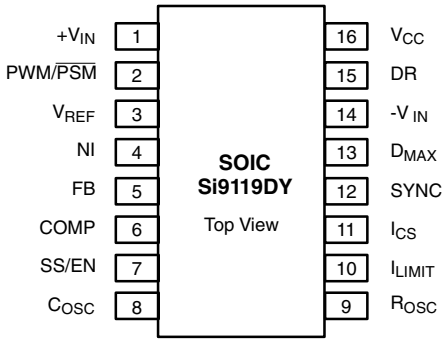
Supply Current vs. Supply Voltage



Switching Frequency vs. Supply Voltage

PIN CONFIGURATIONS AND ORDERING INFORMATION





ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9118DY-T1-E3	- 40 to 85 °C	SOIC-16

PIN DESCRIPTION		
Pin Number	**Symbol**	**Description**
1	$+V_{IN}$	Input bus voltage ranging from 10 V to 200 V.
2	PWM/$\overline{PSM}$	Connected to V_{REF} forces the converter into PWM mode. Connected to $-V_{IN}$ forces the converter into PSM mode.
3	V_{REF}	4 V reference voltage. Decouple with 0.1 µF ceramic capacitor.
4	NI	Non-inverting input of an error amplifier.
5	FB	Inverting input of an error amplifier.
6	COMP	Error amplifier output for external compensation network.
7	SS/EN	Programmable soft-start with external capacitor or externally controlled disable mode.
8	C_{OSC}	External capacitor to determine the switching frequency.
9	R_{OSC}	External resistor to determine the switching frequency.
10	I_{LIMIT}	Pulse by pulse peak current limiting pin. When the current sense voltage exceeds the current limit threshold, the gate drive signal is terminated. I_{LIMIT} is also used to sense the current in pulse skipping mode.
11	I_{CS}	Current sense input to control feedback response.
12	SYNC or V_{SC}	Si9118: slope compensation pin. Si9119: clock synchronization pin. Logic high to low transition from external signal synchronizes the internal clock frequency.
13	D_{MAX}	Sets the maximum duty cycle. Internally, the maximum duty cycle is clamped to 80 %.
14	$-V_{IN}$	Single point ground.
15	D_R	Gate drive for the external MOSFET switch.
16	V_{CC}	Supply voltage for the IC after the startup transition.

STANDARD APPLICATION CIRCUITS

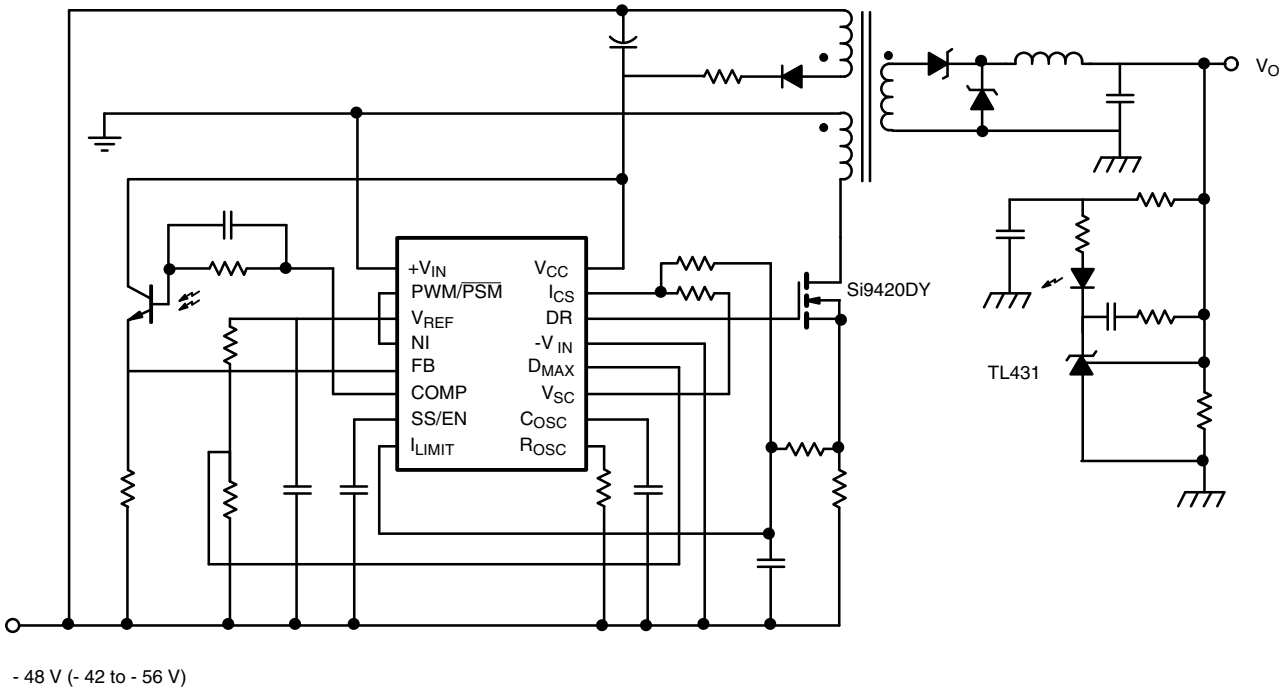


Figure 2. Si9118 15 W Forward Converter Schematic

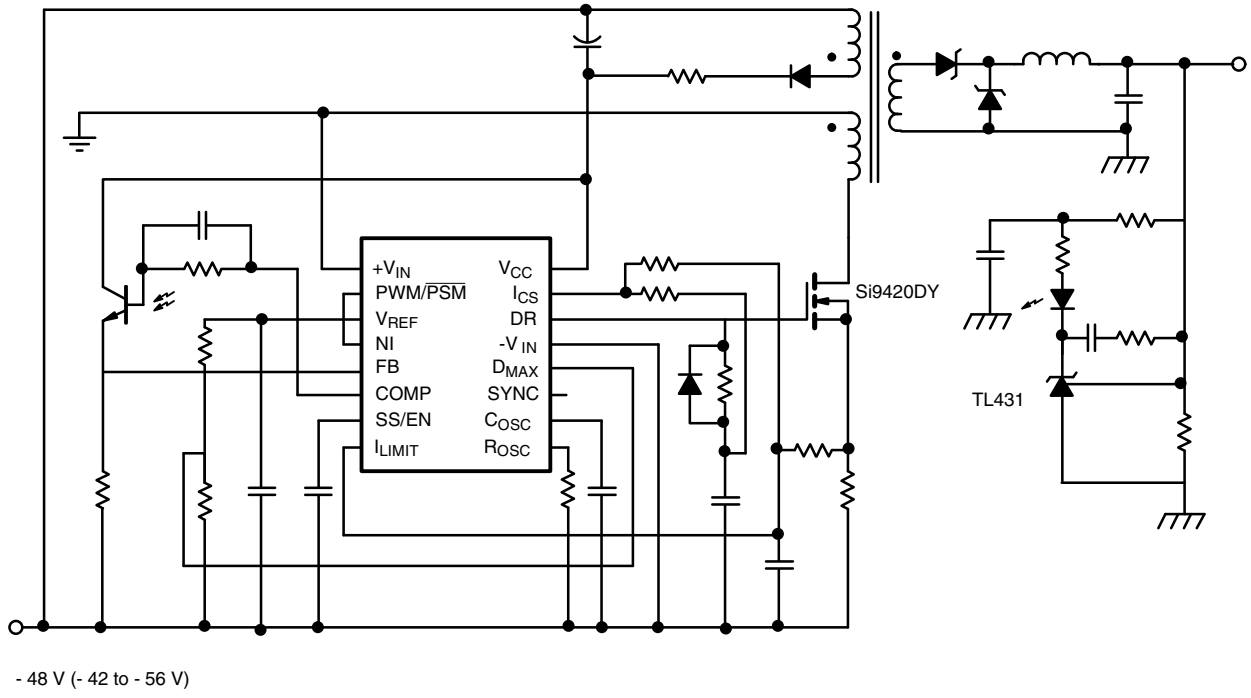


Figure 3. Si9119 Forward Converter With External Slope Compensation

DETAILED OPERATIONAL DESCRIPTION

Start-Up

Si9118/Si9119 are designed with internal depletion mode MOSFET capable of powering directly from the high input bus voltage. This feature eliminates the typical external start-up circuit saving valuable space and cost. But, most of all, this feature improves the converter efficiency during full load and has an even greater impact on light load. With an input bus voltage applied to the $+V_{IN}$ pin, the V_{CC} voltage is regulated to 9.3 V. The UVLO circuit prevents the controller output driver section from turning on, until V_{CC} voltage exceeds 8.7 V. In order to maximize converter efficiency, the designer should provide an external bootstrap winding to override the internal V_{CC} regulator. If external VCC voltage is greater than 9.3 V, the internal depletion mode MOSFET regulator is disabled and power is derived from the external V_{CC} supply. The V_{CC} supply provides power to the internal circuity as well as providing supply voltage to the gate drive circuit.

Soft-Start/Enable

The soft-start time is externally programmable with capacitor connected to the SS/EN pin. A constant current source provides the current to the SS/EN pin to generate a linear start-up time versus the capacitance value. The SS/EN pin clamps the error amplifier output voltage, limiting the rate of increase in duty cycle. By controlling the rate of rise in duty cycle gradually, the output voltage rises gradually preventing the output voltage from overshooting. The SS/EN pin can also be used to enable or disable the output driver section with an external logic signal.

Synchronization

The synchronization to external clock is easily accomplished by connecting the external clock into the SYNC pin (Si9119 only). The logic high to low transition synchronizes the clock. The external clock frequency must be at least 5 % faster than the internal clock frequency.

Reference Voltage

The reference voltage for the Si9118/Si9119 are set at 4.0 V. The reference voltage is not connected to the non-inverting inputs of the error amplifier, therefore, the minimum output voltage is not limited to reference voltage. The V_{REF} pin requires a 0.1 µF decoupling capacitor.

Error Amplifier

The error amplifier gain-bandwidth product is critical parameter which determines the transient response of converter. The transient response is function of both small and large signal responses. The small signal response is determined by the feedback compensation network while the large signal response is determined by the inductor di/dt slew rate. Besides the inductance value, the error amplifier gain-bandwidth determine the converter response time. In order to minimize the response time, Si9118/Si9119 is designed with a 2.7 MHz error amplifier gain-bandwidth product to provide the widest converter bandwidth possible.

PWM Mode

The converter operates in PWM mode if the PWM/$\overline{\text{PSM}}$ pin is connected to V_{REF} pin or logic high. As the load current and line voltage vary, the Si9118/Si9119 maintain constant switching frequency until they reach minimum duty cycle. Once the output voltage regulation is exceeded with minimum duty cycle, the switching frequency will continue to decrease until regulation is achieved. The switching frequency is controlled by the external R_{osc} and C_{osc} as shown by the typical oscillator frequency curve. In PWM mode, output ripple noise is constant reducing EMI concerns as well as simplifying the filter to minimize the system noise.

Pulse Skipping Mode

If the PWM/$\overline{\text{PSM}}$ pin is connected to $-V_{IN}$ pin (logic low), the converter can operate in either PWM or PSM mode depending on the load current. The converter automatically transitions from PWM to PSM or vise versa to maintain output voltage regulation. In PSM mode, the MOSFET switch is turned on until the peak current sensed voltage reaches 100 mV and the output voltage meets or exceeds its regulation voltage. The converter is operating in pulse skipping mode because each pulse delivers excess energy into the output capacitor forcing the output voltage to exceed its regulation voltage. By forcing the output voltage to exceed the regulation voltage, succeeding pulses are skipped until the output voltage drops below the regulation point. Therefore, switching frequency will continue to reduce during PSM control as the demand for output current decreases. The pulse skipping mode cuts down the switching losses, the dominant power consumed during low output current, thereby maintaining high efficiency throughout the entire load range. With PWM/$\overline{\text{PSM}}$ pin in logic low state, the converter transitions back into PWM mode, if the peak current sensed voltage of 100 mV does not generate the required output voltage. In the region between pulse skipping mode and PWM mode, the controller may transition between the two modes, delivering spurts of pulses. This may cause the current waveform to look irregular, but this will not overly affect the ripple voltage. Even in this transitional mode, efficiency remains high.

DETAILED OPERATIONAL DESCRIPTION (CONT'D)

Programmable Duty Cycle Control

The maximum duty cycle limit is controlled by the voltage on D_{MAX} pin. A D_{MAX} voltage of 3.2 V generates 80 % duty cycle while 0.0 V generates 0 % duty cycle. The 80 % duty cycle is maximum default condition at 1 MHz switching frequency. The D_{MAX} voltage can be easily generated using resistor divider from the reference voltage.The maximum duty cycle limitation will be different when the converter is synchronized by an external frequency. If the internal free running frequency is much slower than the external SYNC signal (SYNC signal causes the internal clock to reset before the Cosc voltage ramps to 3.2 V) , duty cycle is determined by the one shot discharge time of the oscillator capacitor (100 ns). Therefore, with 1 MHz SYNC signal, maximum duty cycle of 90 % can be achieved (100 ns is 10 % of 1 MHz). If the internal free running frequency is very close to the external SYNC frequency (SYNC signal causes the internal clock to reset somewhere between 3.2 V to 4 V), duty cycle is determined by the ratio of C_{osc} voltage at the SYNC point and the 3.2 V. At this condition, the maximum duty cycle can be greater than 90 %. Therefore, D_{MAX} voltage must be modified in order to maintain desired maximum duty cycle.

Slope Compensation

Slope compensation is necessary for duty cycles greater than 50 % to stabilize the inner current loop and maintain overall loop stability. In order to simplify the slope compensation circuitry, the Si9118 provides the buffered oscillator ramp signal, V_{SC} to be used for external slope compensation. V_{SC} is only available when DR is high. The V_{SC} signal super-imposed with actual current sense signal should be used by the PWM comparator to determine the duty cycle. The summation of this signal should be fed into I_{CS} pin. For optimum performance, proper slope compensation is required. The amount of slope compensation is determined by the resistors connected to the I_{CS} pin. The amplitude of the V_{SC} signal is same as the C_{OSC} pin voltage (≈ 4 V). For designs which use with SYNC pin, instead of V_{SC} pin, the converter can still operate at duty cycles greater than 50 % by generating an external slope compensation ramp using a

simple RC circuit from the MOSFET driver output pin as shown on the application circuit.

Over Current Protection

Si9118/Si9119 are designed with a pulse-to-pulse peak

current limiting protection circuit to protect itself, and the load in case of a failure. The voltage across the sense resistor is monitored continuously and if the voltage reaches its trigger level, the duty cycle is terminated. This limits the maximum current delivered to the load. In order to improve the accuracy of over current protection from traditional controllers, Si9118/ Si9119 are designed with separate I_{LIMIT} and I_{CS} pins. Voltage on the I_{LIMIT} pin does not sum in the traditional slope compensation voltage, which adds error into the detection level. I_{CS} pin is used to sum the current sense signal and the slope compensation for loop stability.

Output Driver Stage

The DR pin is designed to drive a low-side N-Channel MOSFET. The driver stage is sized to sink and source peak currents up to 500 mA with V_{CC} = 12 V. This provides ample drive capability for 50 W of output power.

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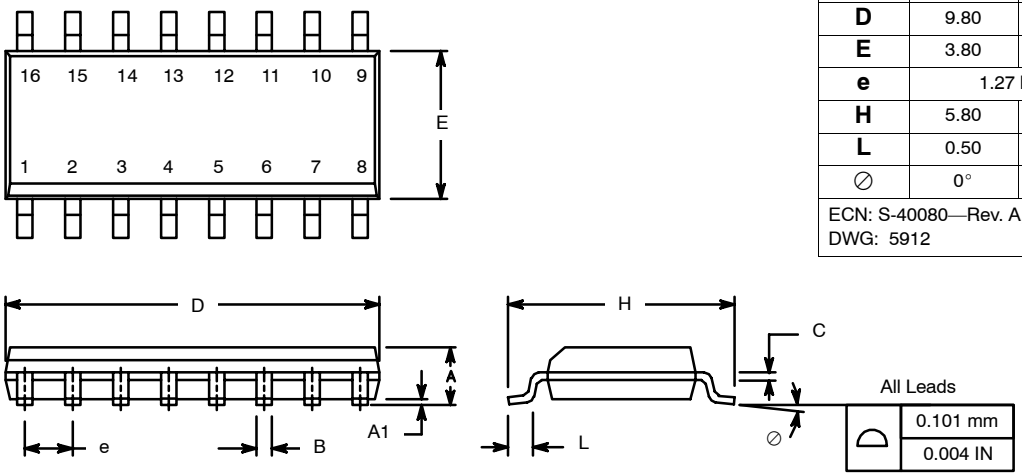
SOIC (NARROW): 16-LEAD (POWER IC ONLY)

JEDEC Part Number: MS-012



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-40080—Rev. A, 02-Feb-04
DWG: 5912

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