



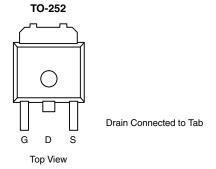
N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a			
30	0.0120 at V _{GS} = 10 V	17.5			
30	0.0175 at V _{GS} = 4.5 V	14.5			

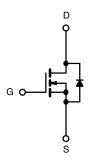
FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC





Ordering Information: SUD50N03-12P-E3 (Lead (PB) free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage	V _{DS}	30	V			
Gate-Source Voltage	V _{GS}	± 20				
Outliness Durin Oursell	T _A = 25 °C	I_	17.5			
Continuous Drain Current ^a	T _A = 100 °C	I _D	12.4			
Pulsed Drain Current	I _{DM}	40	Α			
Continuous Source Current (Diode Conduction) ^a	I _S	5				
Avalanche Current	L = 0.1 mH	I _{AS}	30			
Single Pulse Avalanche Energy	L=0.1 IIII	E _{AS}	45	mJ		
Maximum Dawar Dissination	T _C = 25 °C	В	46.8	w		
Maximum Power Dissipation	T _A = 25 °C	P _D	6.5 ^a	¬		
Operating Junction and Storage Temperature Range	•	T _J , T _{stg}	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Mariana Landia La Anticala	t ≤ 10 s	- R _{thJA}	18	23	°C/W	
Maximum Junction-to-Ambient ^a	Steady State		40	50		
Maximum Junction-to-Case		R _{thJC}	2.6	3.2		

a. Surface mounted on FR4 board, $t \le 10 \text{ s.}$

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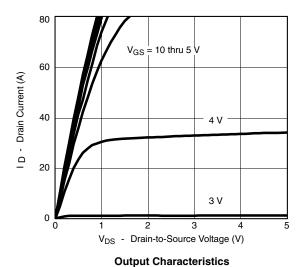
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min .	Typ. ^a	Max.	Unit	
Static	Static						
Drain-Source Breakdown Voltage	V _{DS}	V_{DS} $V_{GS} = 0 \text{ V, I}_{D} = 250 \mu\text{A}$				٧	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		± 100	nA	
Zero Gate Voltage Drain Current	l	V _{DS} = 24 V, V _{GS} = 0 V			1 ,,,		
Zero Gate voltage Drain Current	I _{DSS}	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50	μΑ	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	40			Α	
		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0100	0.0120	Ω	
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C			0.0170		
		V _{GS} = 4.5 V, I _D = 15 A		0.0138	0.0175		
Forward Transconductance ^b	9 _{fs}	V _{DS} = 15 V, I _D = 20 A	15			S	
Dynamic ^a							
Input Capacitance	C _{iss}			1600		pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		285			
Reverse Transfer Capacitance	C _{rss}			140			
Total Gate Charge ^c	Q_{g}			28	42		
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$		6		nC	
Gate-Drain Charge ^c	Q_{gd}			5		1	
Gate Resistance	R_{g}	f = 1 MHz	0.3	1.5	3.0	Ω	
Turn-On Delay Time ^c	t _{d(on)}			9	15		
Rise Time ^c	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 0.3 \Omega$		15	25	ns	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 2.5 \Omega$		20	30		
Fall Time ^c	t _f			12	20		
Source-Drain Diode Ratings and Characteristics ($T_C = 25 ^{\circ}C$)							
Pulsed Current	I _{SM}				100	Α	
Diode Forward Voltage ^b	V_{SD}	I _F = 40 A, V _{GS} = 0 V		1.2	1.5	V	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 50 A, dl/dt = 100 A/μs		25	70	ns	

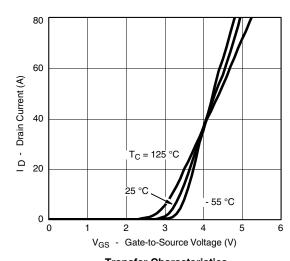
Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C unless noted)

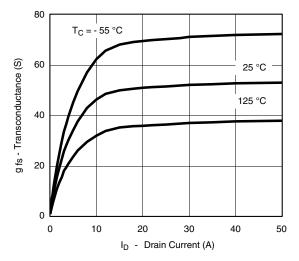




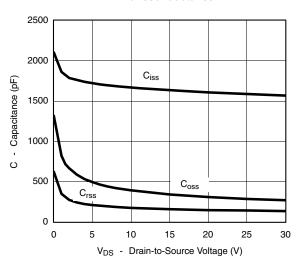
Transfer Characteristics



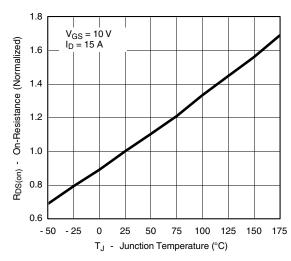
TYPICAL CHARACTERISTICS (25 °C unless noted)



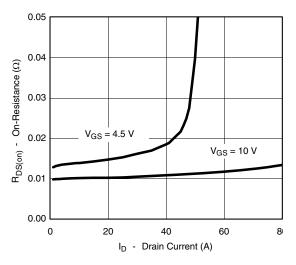
Transconductance



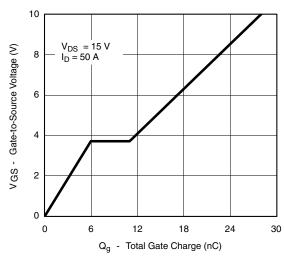
Capacitance



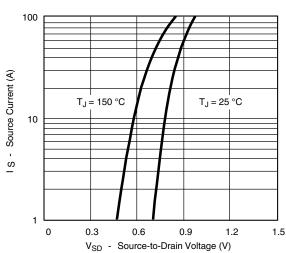
On-Resistance vs. Junction Temperature



On-Resistance vs. Drain Current



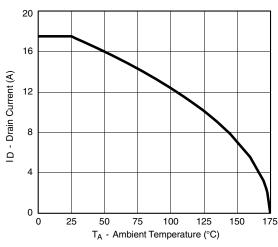
Gate Charge

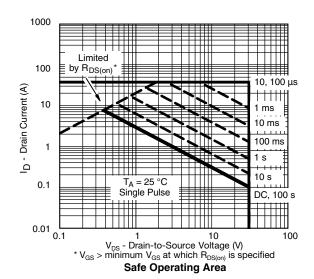


Source-Drain Diode Forward Voltage

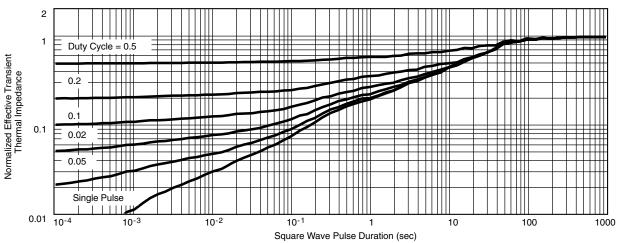
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THERMAL RATINGS

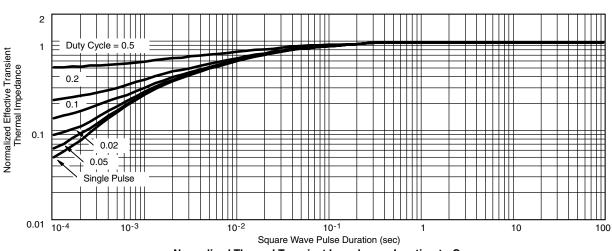




Maximum Drain Current vs. Ambient Temperature



Normalized Thermal Transient Impedance, Junction-to-Ambient



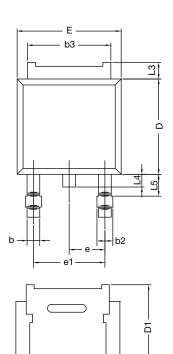
Normalized Thermal Transient Impedance, Junction-to-Case

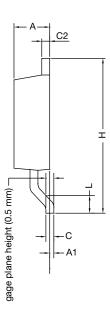
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TO-252AA Case Outline





	MILLIMETERS		INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
Е	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28 BSC		0.090	BSC	
e1	4.56	BSC	0.180	BSC	
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T16-0236-Rev. P, 16-May-16					

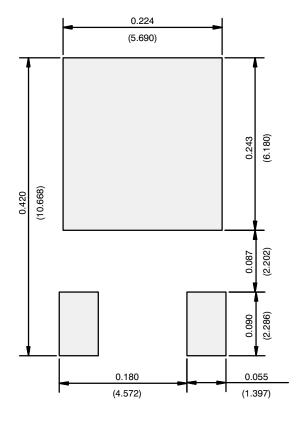
DWG: 5347 Notes

• Dimension L3 is for reference only.

Revision: 16-May-16 Document Number: 71197



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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