# N-Channel 100-V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A) | $Q_g$ (Typ.) |
| 100 | 0.0183 at $V_{GS}$ = 10 V | 60 | 48 |
| | 0.023 at $V_{GS}$ = 8.0 V | 53 | |

## FEATURES

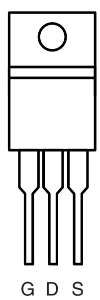
- TrenchFET® Power MOSFET
- 100 % $R_g$ and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT

## APPLICATIONS

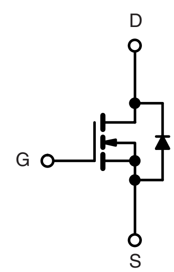
- Industrial
- Power Supply

TO-220AB




Top View

**Ordering Information:** SUP60N10-18P-E3 (Lead (Pb)-free)




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS $T_C$ = 25 °C, unless otherwise noted | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Limit** | **Unit** |
| Drain-Source Voltage | | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current ($T_J$ = 175 °C) | $T_C$ = 25 °C | $I_D$ | 60 | A |
| | $T_C$ = 70 °C | | 50 | |
| Pulsed Drain Current | | $I_{DM}$ | 100 | |
| Avalanche Current | | $I_{AS}$ | 45 | |
| Single Avalanche Energy[a] | L = 0.1 mH | $E_{AS}$ | 101 | mJ |
| Maximum Power Dissipation[a] | $T_C$ = 25 °C | $P_D$ | 150[b] | W |
| | $T_A$ = 25 °C[c] | | 3.75 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 175 | °C |

| THERMAL RESISTANCE RATINGS | | | |
|---|---|---|---|
| **Parameter** | **Symbol** | **Limit** | **Unit** |
| Junction-to-Ambient (PCB Mount)[c] | $R_{thJA}$ | 40 | °C/W |
| Junction-to-Case (Drain) | $R_{thJC}$ | 1.0 | |

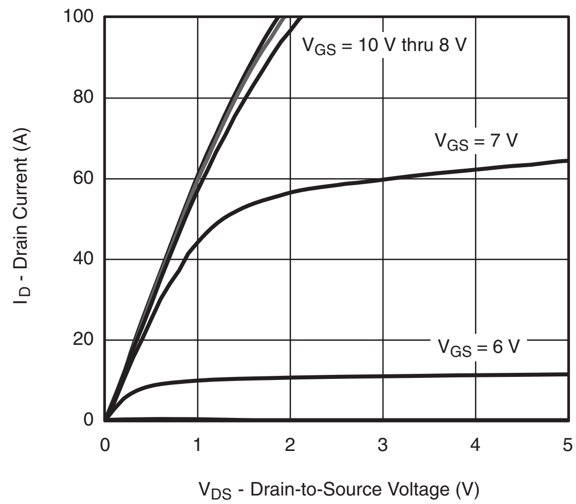
Notes:
a. Duty cycle ≤ 1 %.
b. See SOA curve for voltage derating.
c. When Mounted on 1" square PCB (FR-4 material).

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{DS}$ = 0 V, $I_D$ = 250 µA | 100 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 µA | 2.5 | | 4.5 | |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | | | ± 250 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | | 50 | |
| | | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V, $T_J$ = 175 °C | | | 250 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS} \geq$ 10 V, $V_{GS}$ = 10 V | 50 | | | A |
| Drain-Source On-State Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 15 A | | 0.015 | 0.0183 | Ω |
| | | $V_{GS}$ = 10 V, $I_D$ = 15 A, $T_J$ = 125 °C | | 0.027 | 0.033 | |
| | | $V_{GS}$ = 8.0 V, $I_D$ = 10 A | | 0.018 | 0.023 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 15 A | | 33 | | S |
| **Dynamic**[b] | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 50 V, f = 1 MHz | | 2600 | | pF |
| Output Capacitance | $C_{oss}$ | | | 230 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 80 | | |
| Total Gate Charge[c] | $Q_g$ | $V_{DS}$ = 50 V, $V_{GS}$ = 10 V, $I_D$ = 50 A | | 48 | 75 | nC |
| Gate-Source Charge[c] | $Q_{gs}$ | | | 16 | | |
| Gate-Drain Charge[c] | $Q_{gd}$ | | | 13 | | |
| Gate Resistance | $R_g$ | f = 1 MHz | 0.25 | 1.1 | 2.4 | Ω |
| Turn-On Delay Time[c] | $t_{d(on)}$ | $V_{DD}$ = 50 V, $R_L$ = 1.0 Ω<br>$I_D \cong$ 50 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω | | 12 | 20 | ns |
| Rise Time[c] | $t_r$ | | | 10 | 20 | |
| Turn-Off Delay Time[c] | $t_{d(off)}$ | | | 18 | 35 | |
| Fall Time[c] | $t_f$ | | | 8 | 15 | |
| **Drain-Source Body Diode Characteristics** $T_C$ = 25 °C[b] | | | | | | |
| Continuous Current | $I_S$ | | | | 60 | A |
| Pulsed Current | $I_{SM}$ | | | | 100 | |
| Forward Voltage[a] | $V_{SD}$ | $I_F$ = 15 A, $V_{GS}$ = 0 V | | 0.85 | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 50 A, dI/dt = 100 A/µs | | 80 | 120 | ns |
| Peak Reverse Recovery Current | $I_{RM(REC)}$ | | | 4 | | A |
| Reverse Recovery Charge | $Q_{rr}$ | | | 160 | 240 | nC |

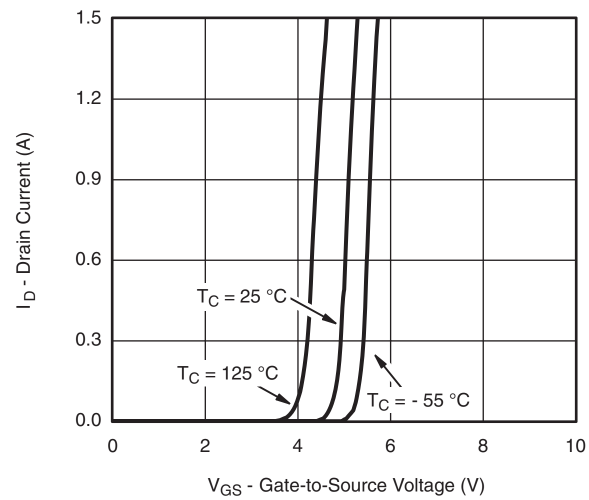
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

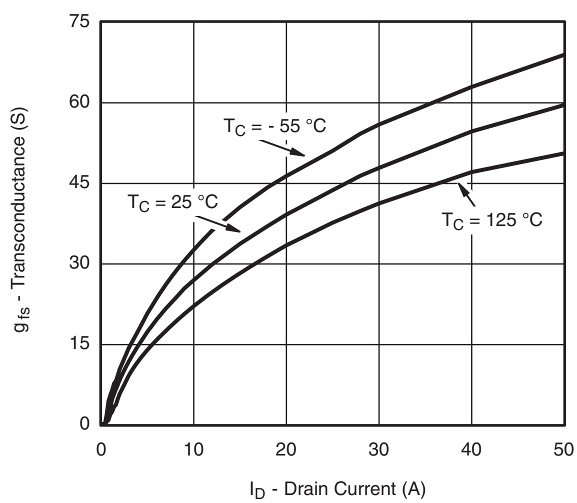
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



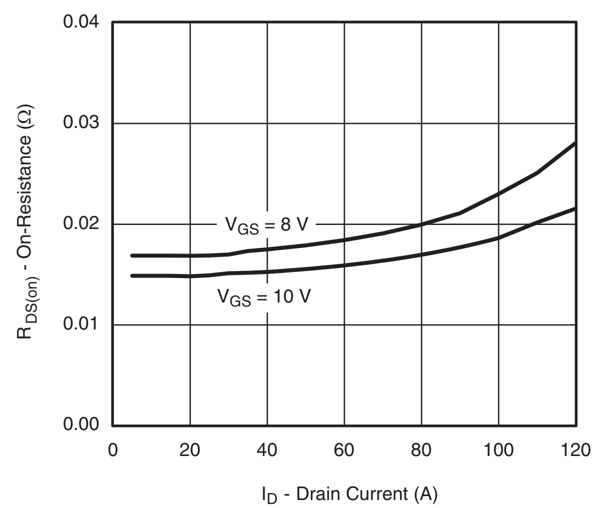

**Output Characteristics**



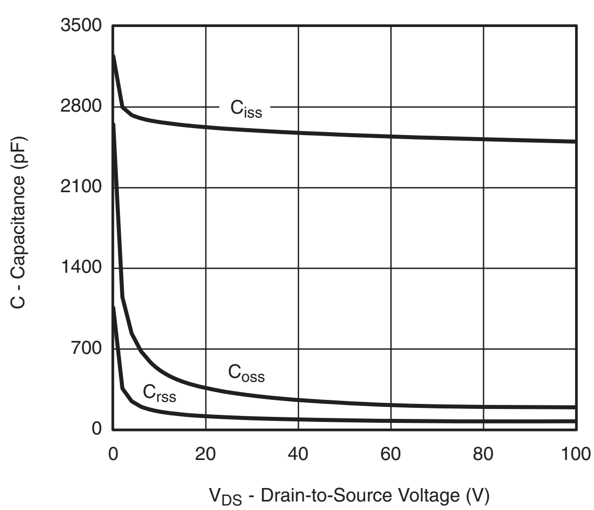

**Transfer Characteristics**



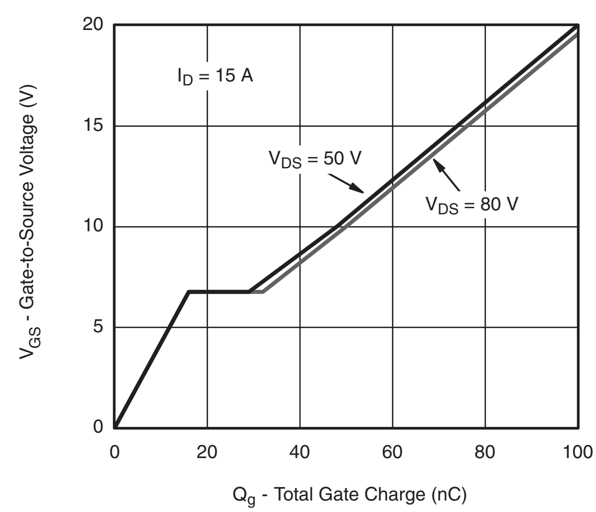

**Transconductance**




**On-Resistance vs. Drain Current**

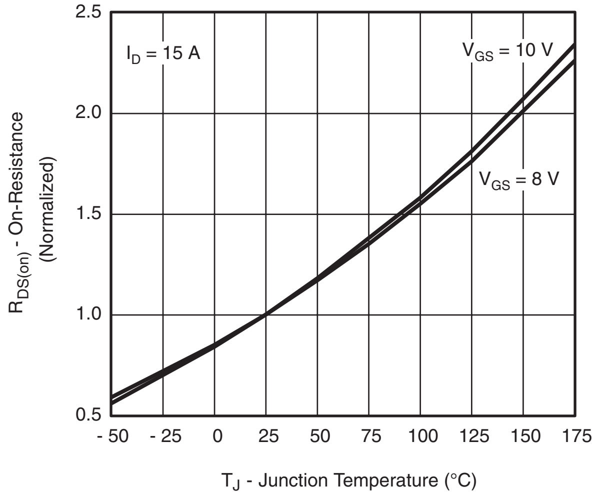



**Capacitance**

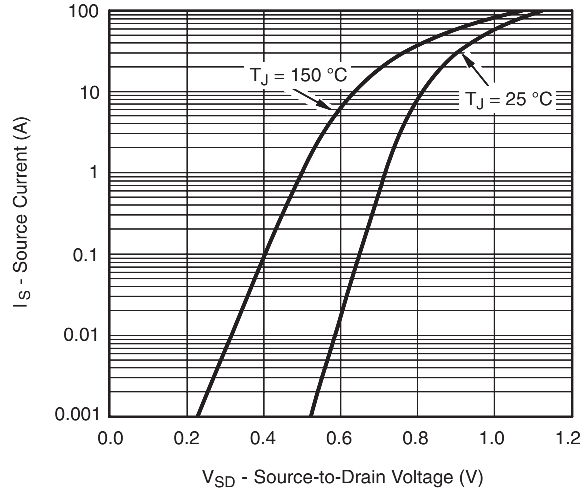



**Gate Charge**

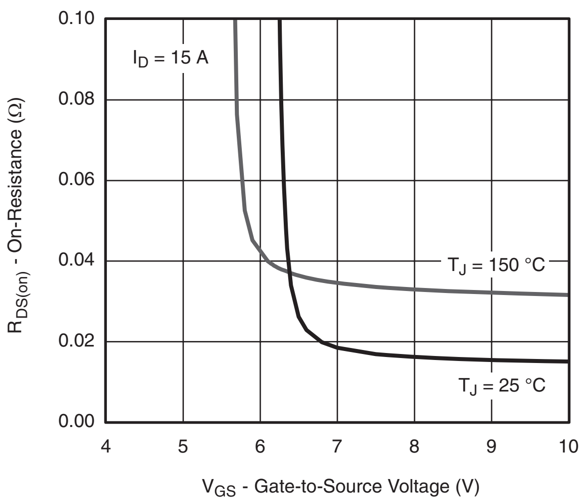
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



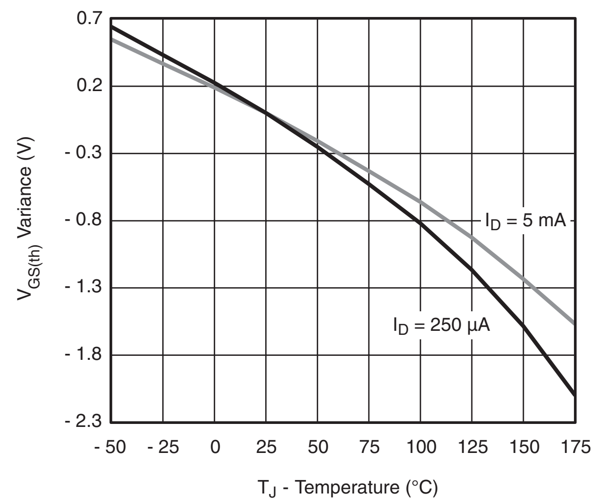

**On-Resistance vs. Junction Temperature**



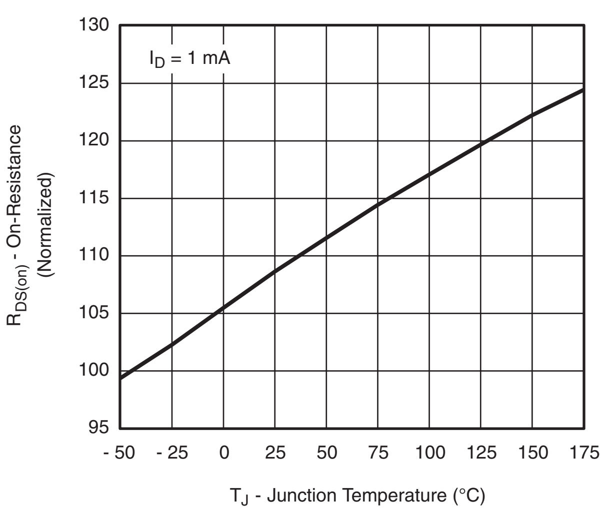

**Source-Drain Diode Forward Voltage**



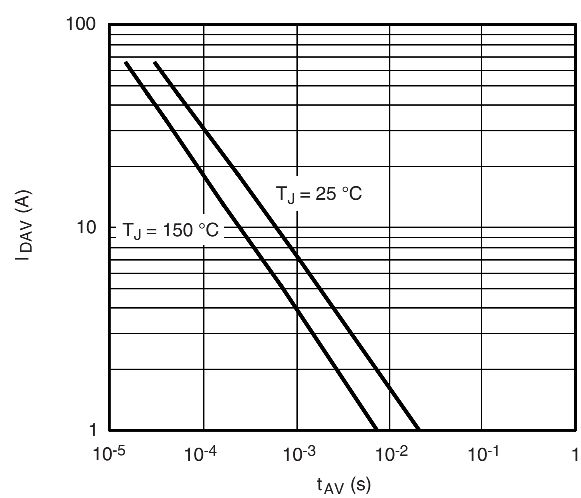

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**




**On-Resistance vs. Junction Temperature**




**Avalanche Current vs. Time**



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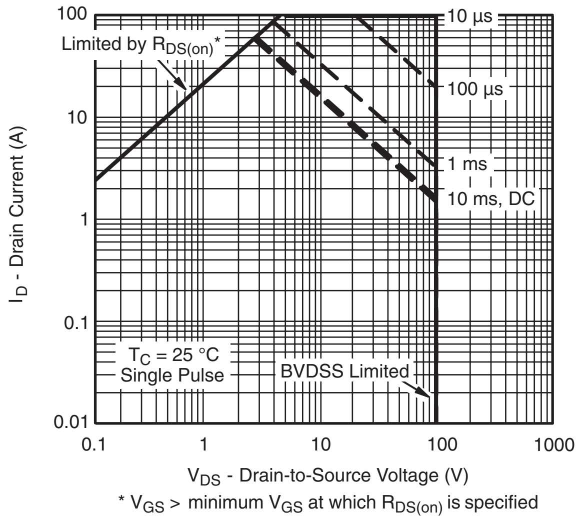
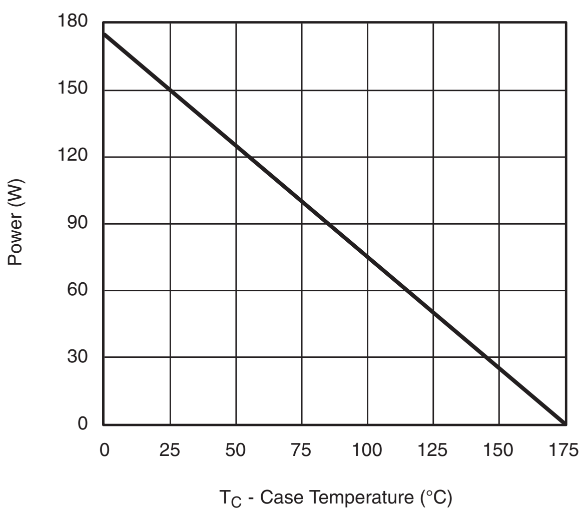
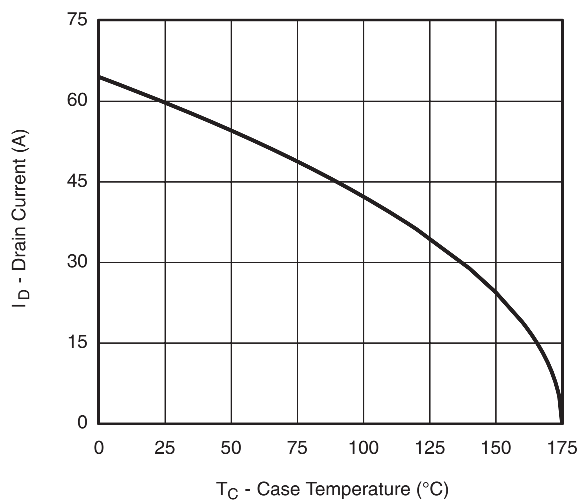
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted




**Safe Operating Area**



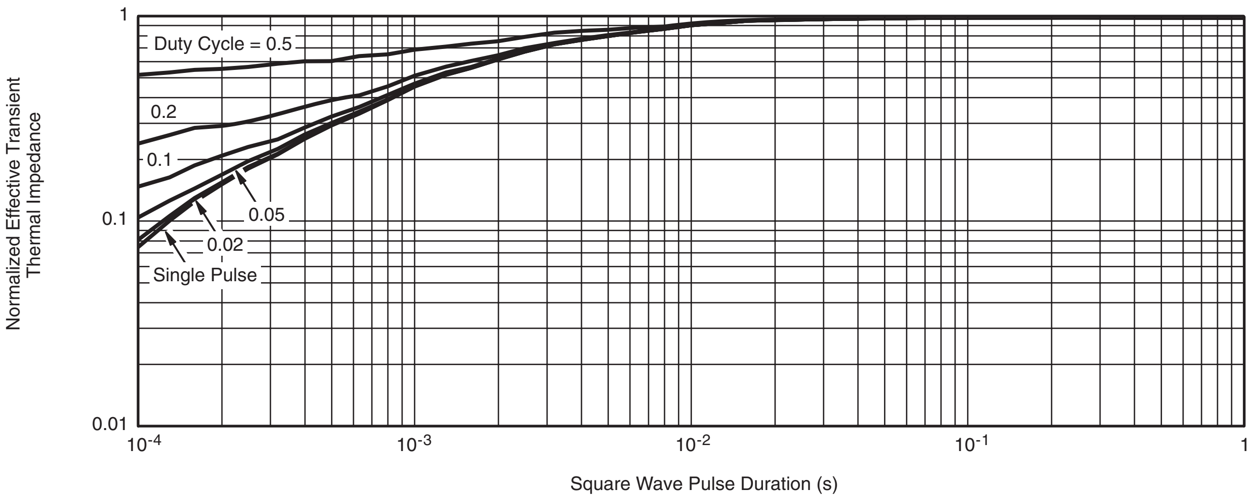

**Power Derating, Junction-to-Case**




**Current Derating***

* The power dissipation $P_D$ is based on $T_{J(max.)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted




**Normalized Thermal Transient Impedance, Junction-to-Case**

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