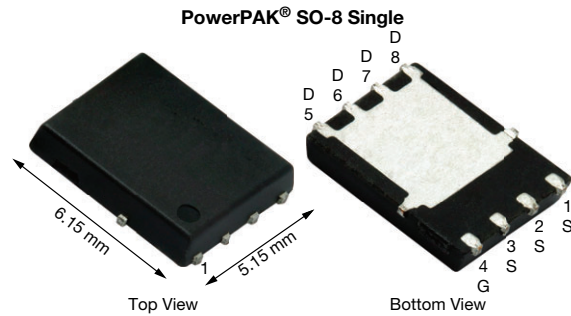


N-Channel 200 V (D-S) MOSFET

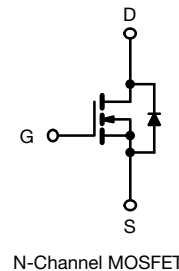


FEATURES

- TrenchFET® power MOSFETs
- New low thermal resistance PowerPAK® package with low 1.07 mm profile
- PWM optimized for fast switching

APPLICATIONS

- Primary side switch



PRODUCT SUMMARY	
V_{DS} (V)	200
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.130
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 6$ V	0.142
Q_g typ. (nC)	20
I_D (A)	4.1
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free	Si7462DP-T1-E3
Lead (Pb)-free and halogen-free	Si7462DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL	10 s	STEADY STATE	UNIT	
Drain-source voltage	V_{DS}	200	200	V	
Gate-source voltage	V_{GS}	± 20	± 20		
Continuous drain current ($T_J = 150$ °C) ^a	$T_A = 25$ °C	4.1	2.6	A	
	$T_A = 85$ °C	3	1.9		
Pulsed drain current	I_{DM}	12	12		
Avalanche current	$L = 0.1$ mH	I_{AS}	6	6	
Single avalanche energy (duty cycle ≤ 1 %)		E_{AS}	1.8	1.8	mJ
Continuous source current (diode conduction) ^a		I_S	4	1.6	A
Maximum power dissipation ^a	$T_A = 25$ °C	P_D	4.8	1.9	W
	$T_A = 85$ °C		2.6	1	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^a	R_{thJA}	$t \leq 10$ s	21	26	°C/W
		Steady state	55	65	
Maximum junction-to-case (drain)	R_{thJC}	1.7	2.1		

Notes

- Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^\circ\text{C}$	-	-	20	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	12	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 4.1\text{ A}$	-	0.110	0.130	Ω
		$V_{GS} = 6\text{ V}$, $I_D = 3.9\text{ A}$	-	0.120	0.142	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 4.1\text{ A}$	-	13	-	S
Diode forward voltage ^a	V_{SD}	$I_S = 4\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Dynamic ^b						
Total gate charge	Q_g	$V_{DS} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 4.1\text{ A}$	-	20	30	nC
Gate-source charge	Q_{gs}		-	4.5	-	
Gate-drain charge	Q_{gd}		-	6.5	-	
Gate resistance	R_g		-	2	-	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 100\text{ V}$, $R_L = 100\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$	-	15	25	ns
Rise time	t_r		-	15	25	
Turn-off delay time	$t_{d(off)}$		-	40	60	
Fall time	t_f		-	20	30	
Source-drain reverse recovery time	t_{rr}	$I_F = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	70	110	

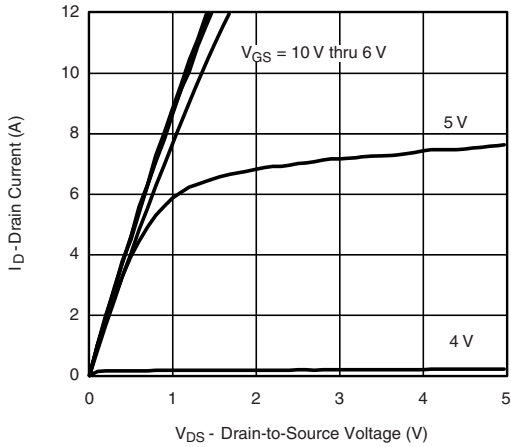
Notes

- a. Pulse test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

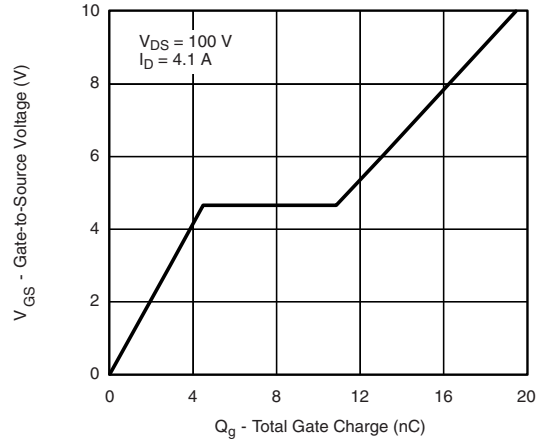
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



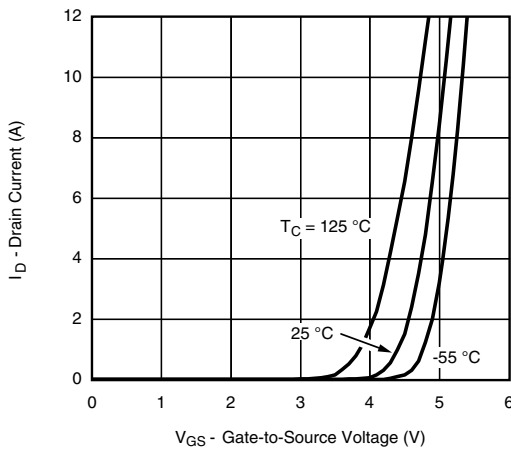
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



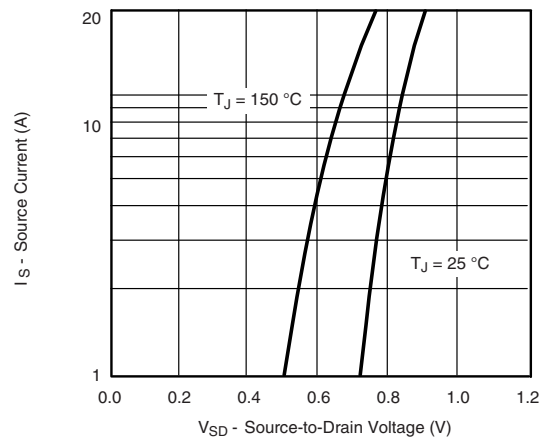
Output Characteristics



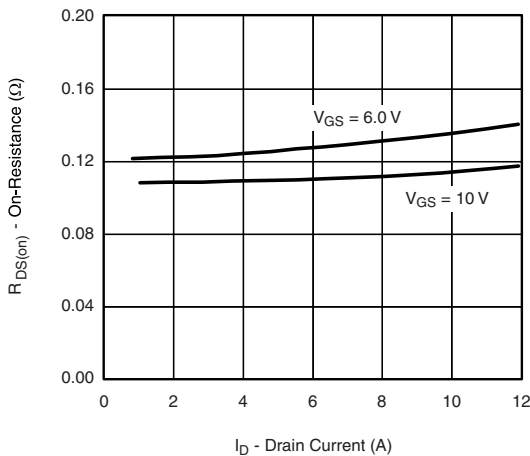
Gate Charge



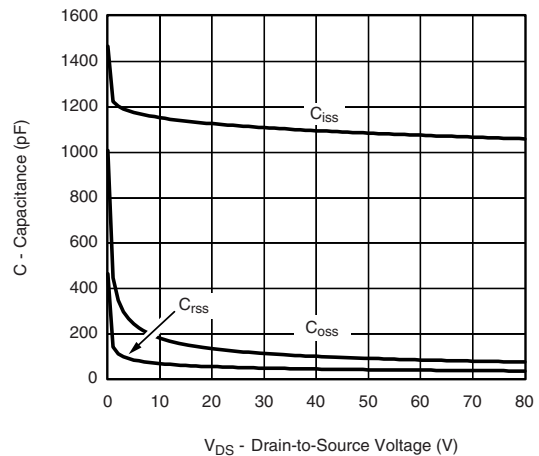
Transfer Characteristics



Source-Drain Diode Forward Voltage



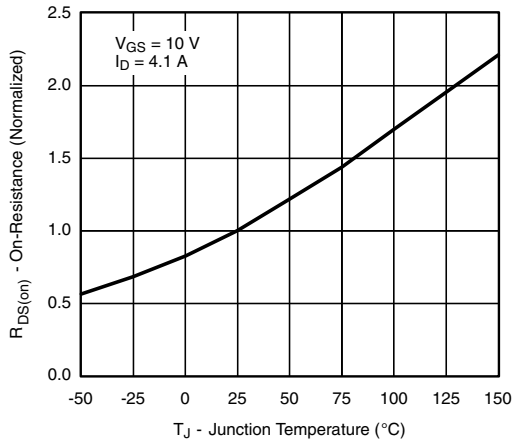
On-Resistance vs. Drain Current



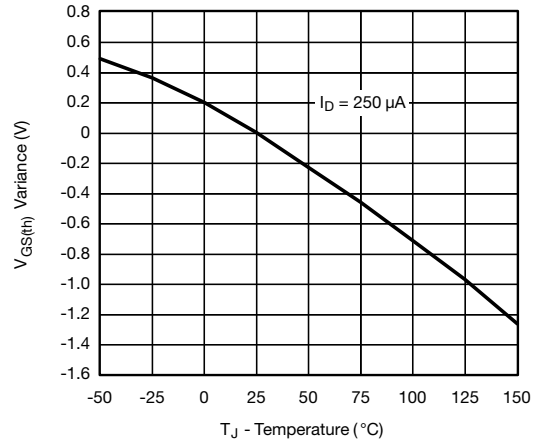
Capacitance



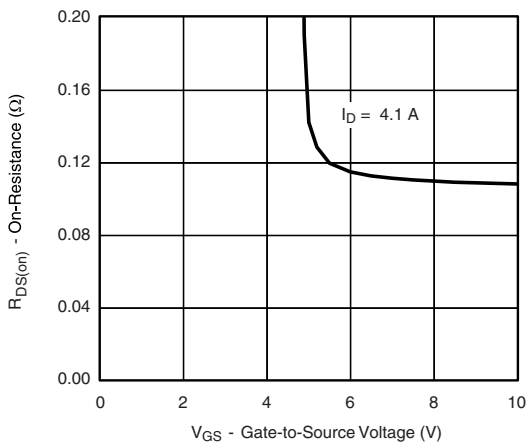
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



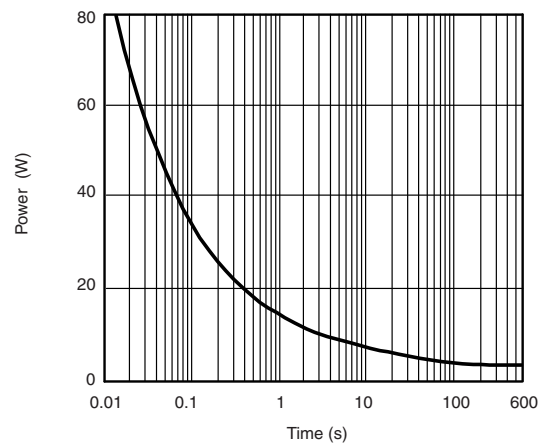
On-Resistance vs. Junction Temperature



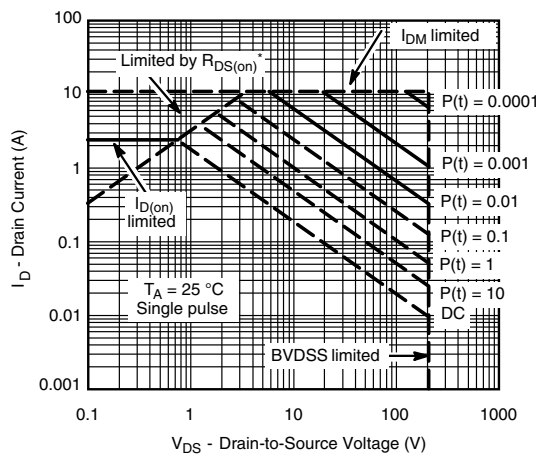
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



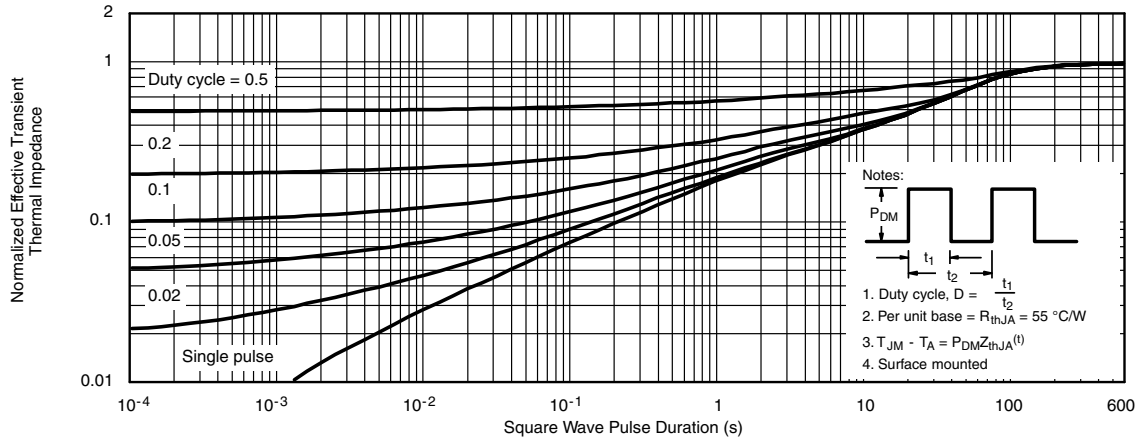
Single Pulse Power



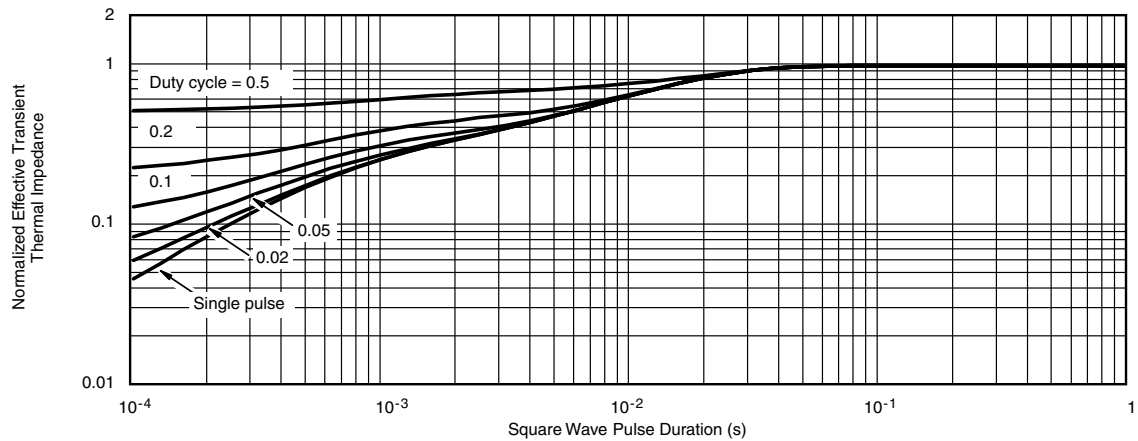
Safe Operating Area



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

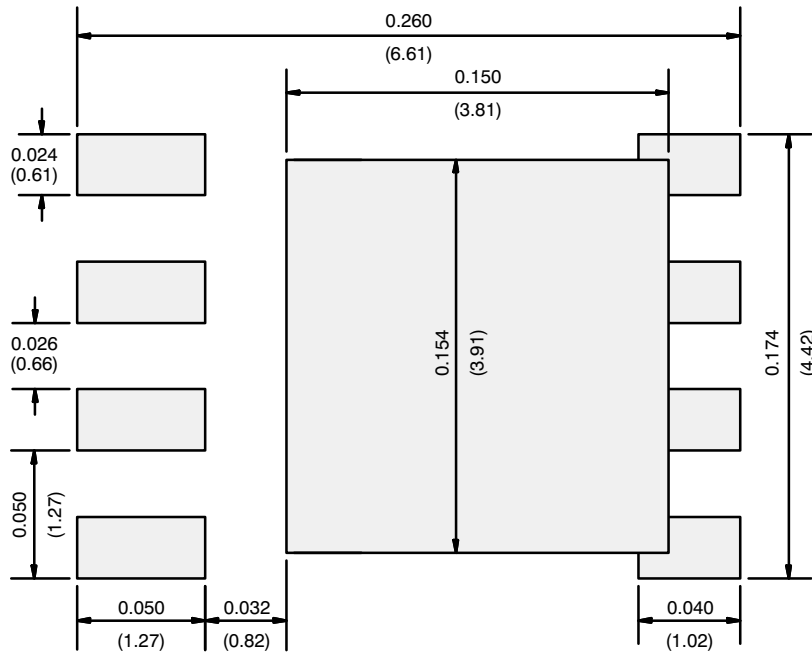
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PowerPAK[®] SO-8, (Single/Dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S17-0173-Rev. L, 13-Feb-17						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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