200 Ω, Low Leakage, Low Parasitic and Low Charge Injection, Quad SPST Analog Switches

DESCRIPTION

The DG2501, DG2502, and DG2503 are monolithic quad single-pole single-throw (SPST) analog switches that operate from a single 1.8 V to 5.5 V power supply.

These switches are fully specified at 3 V and 5 V. The parts feature low parasitic capacitance, low charge injection, and low leakage performance over the full operating temperature range of -40 °C to +85 °C. Their ESD/HBM tolerance is over 8 kV.

The DG2501, DG2502, and DG2503 each feature four independently selectable SPST switches with closely matched channel resistance. The DG2501 is normally closed, while the DG2502 is normally open.

The DG2503 has two normally open and two normally closed switches. All parts are guaranteed break-before-make operation for use in multiplexer applications. The parts have a guaranteed control logic high of 1.4 V when V+ is 3 V and 1.8 V when V+ is 5 V.

Each switch conducts equally well in both directions when on, and each has an input signal range that extends to the supplies.

The DG2501, DG2502, and DG2503 are ideal for portable healthcare, instrument, and communication devices.

The DG2501, DG2502, and DG2503 are available in wafer level CSP package with top side lamination.

The package has a 4 x 4 bump array, 0.35 mm pitch, and 1.44 mm x 1.44 mm length and width.

FEATURES

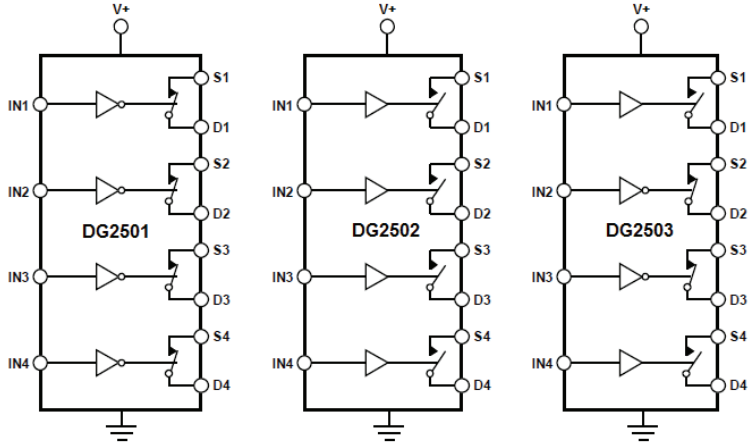
- 1.8 V to 5.5 V single supply operation
- Low leakage, 1 nA / max. at 85 °C
- Low switch off capacitance
- Rail-to-rail signal handling
- Latch up current > 800 mA (JESD78)
- ESD: 8000 V/HBM
- Typical power consumption (< 0.01 µW)
- TTL/CMOS compatible
- Compact WCSP16 1.44 mm x 1.44 mm
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

APPLICATIONS

- Analog front end signal switching
- Sample-and-hold circuits
- Battery-powered systems
- Portable meters
- Automatic test equipment
- Medical and healthcare equipment
- Communication systems

FUNCTIONAL BLOCK DIAGRAM



Switches are shown for a Logic 0 Input

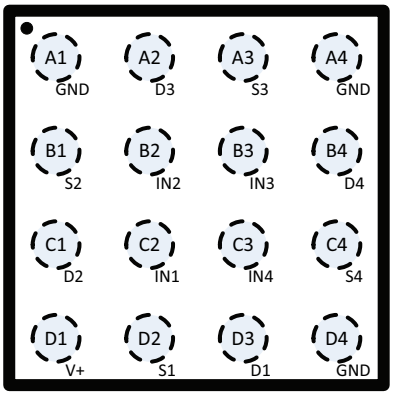
TRUTH TABLE

DG2501		DG2502		DG2503		
LOGIC	SWITCH	LOGIC	SWITCH	LOGIC	SW1, SW4	SW2, SW3
0	ON	0	OFF	0	OFF	ON
1	OFF	1	ON	1	ON	OFF

ORDERING INFORMATION

PART NUMBER	CONFIGURATION	SWITCH FUNCTION	TEMPERATURE RANGE	PACKAGE	REEL QUANTITY
DG2501DB-T2-GE1	Quad SPST	NC	-40 °C to +85 °C	WCSP16, 1.44 mm x 1.44 mm	3000
DG2501DB-T4-GE1	Quad SPST	NC	-40 °C to +85 °C	WCSP16, 1.44 mm x 1.44 mm	10 000
DG2502DB-T2-GE1	Quad SPST	NO	-40 °C to +85 °C	WCSP16, 1.44 mm x 1.44 mm	3000
DG2502DB-T4-GE1	Quad SPST	NO	-40 °C to +85 °C	WCSP16, 1.44 mm x 1.44 mm	10 000
DG2503DB-T2-GE1	Quad SPST	NC/NO	-40 °C to +85 °C	WCSP16, 1.44 mm x 1.44 mm	3000
DG2503DB-T4-GE1	Quad SPST	NC/NO	-40 °C to +85 °C	WCSP16, 1.44 mm x 1.44 mm	10 000

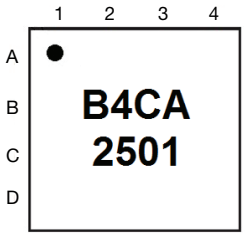
PACKAGE OUTLINE



Top View
(Bump Side Down)

Fig. 1 - Package Outline for WCSP16, 1.44 mm x 1.44 mm, 0.35 mm Pitch

DEVICE MARKING



Row 1 Dot = Pin A1 Locator
Row 2 B = Fab, 4 = Year, C = Week Code, A = Lot Code
Row 3 2501 = Part Code

Fig. 2 - Device Marking

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL PARAMETERS	CONDITIONS	LIMITS	UNIT
V+, INx	Reference to GND	-0.3 to +6	V
Sx, Dx	Reference to GND	-0.3 to (V+) +0.3	
Maximum continuous switch current		5	mA
Maximum peak current (Pulsed 1 ms, 10 % duty cycle)		20	
Thermal resistance		80	°C/W
Latch up current	JESD78	> 800	mA
ESD - HBM	ANSI / ESDA / JEDEC® JS-001	> 8000	V
Temperature			
Operating temperature		-40 to +85	°C
Storage temperature		-65 to +150	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

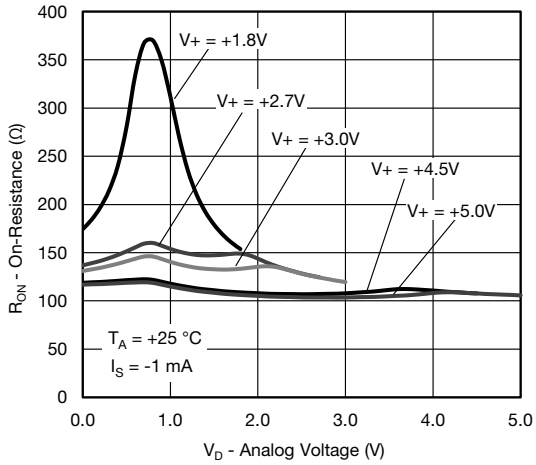
ELECTRICAL CHARACTERISTICS 3 V Supply							
PARAMETER	SYMBOL	TEST CONDITION UNLESS OTHERWISE SPECIFIED, V+ = 3 V V_{INH} = 1.4 V, V_{INL} = 0.4 V [a]	TEMP. [b]	TYP. [c]	-40 °C to +85 °C MIN. [d]	-40 °C to +85 °C MAX. [d]	UNIT
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	-	0	3	V
Drain-source on resistance	$R_{DS(on)}$	V_S = 1.5 V, I_S = -1 mA	Room	133	-	200	Ω
			Full	-	-	250	
On-resistance matching	ΔR_{on}		Room	0.83	-	10	
			Full	-	-	13	
Switch off leakage current	$I_S/I_{D(off)}$	V+ = 3.3 V, V_S = 0.3 V/3 V, V_D = 3 V / 0.3 V	Room	± 0.016	-0.4	+0.4	nA
			Full	-	-1	+1	
Channel on leakage current	$I_{D(on)}$	V+ = 3.3 V, V_D = 0.3 V / 3 V	Room	± 0.009	-0.4	+0.4	
			Full	-	-1	+1	
Digital Control							
Input, high voltage	V_{INH}		Full	-	1.4	-	V
Input, low voltage	V_{INL}		Full	-	-	0.4	
Input leakage	I_{IN}	V_{IN} = V_{GND} or V+	Room	± 0.001	-	-	µA
			Full	-	-0.1	+0.1	
Digital input capacitance [e]	C_{IN}	f = 1 MHz	Room	2	-	-	pF
Dynamic Characteristics							
Break-before make time	t_{BBM}	DG2503 only, V_{S1} = V_{S2} = 1.5 V, R_L = 300 Ω C_L = 35 pF	Room	47	10	-	ns
			Full	-	10	-	
Turn-on time	t_{ON}	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF	Room	175	-	220	
			Full	-	-	250	
Turn-off time	t_{OFF}		Room	77	-	100	
			Full	-	-	120	
Charge injection [e]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_S = 1.5 V	Room	-0.7	-	-	pC
Off isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1MHz	Room	-83	-	-	dB
Cross talk [e]	X Talk		Room	-85	-	-	
3 dB bandwidth [e]	BW	R_L = 50 Ω, C_L = 5 pF	Room	510	-	-	MHz
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz, V_S = 1.5 V	Room	2.9	-	-	pF
Drain off capacitance [e]	$C_{D(off)}$		Room	2.8	-	-	
Drain on capacitance [e]	$C_{D(on)}$		Room	7.8	-	-	
Power Requirements							
Power supply current	I+	Digital input 0 or V+	Room	0.001	-	-	µA
			Full	-	-	1	

ELECTRICAL CHARACTERISTICS 5 V Supply							
PARAMETER	SYMBOL	TEST CONDITION UNLESS OTHERWISE SPECIFIED, V+ = 5 V V_{INH} = 1.8 V, V_{INL} = 0.5 V [a]	TEMP. [b]	TYP. [c]	-40 °C to +85 °C MIN. [d]	-40 °C to +85 °C MAX. [d]	UNIT
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	-	0	5	V
Drain-source on resistance	$R_{DS(on)}$	V_S = 2.5 V, I_S = -1 mA	Room	104	-	150	Ω
			Full	-	-	200	
On-resistance matching	ΔR_{on}		Room	0.39	-	8	
			Full	-	-	10	
Switch off leakage current	$I_S/I_{D(off)}$	V+ = 5.5 V, V_S = 1 V/4.5 V, V_D = 4.5 V/1 V	Room	± 0.022	-0.4	+0.4	nA
			Full	-	-1	+1	
Channel on leakage current	$I_{D(on)}$	V+ = 5.5 V, V_D = 4.5 V/1 V	Room	± 0.017	-0.4	+0.4	
			Full	-	-1	+1	
Digital Control							
Input, high voltage	V_{INH}		Full	-	1.8	-	V
Input, low voltage	V_{INL}		Full	-	-	0.5	
Input leakage	I_{IN}	V_{IN} = V_{GND} or V+	Room	± 0.001	-	-	µA
			Full	-	-1	+1	
Digital input capacitance [e]	C_{IN}	f = 1 MHz	Room	2	-	-	pF
Dynamic Characteristics							
Break-before make time	t_{BBM}	DG2503 only, V_{S1} = V_{S2} = 3 V, R_L = 300 Ω C_L = 35 pF	Room	25	10	-	ns
			Full	-	10	-	
Turn-on time	t_{ON}	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF	Room	64	-	100	
			Full	-	-	150	
Turn-off time	t_{OFF}		Room	38	-	60	
			Full	-	-	100	
Charge injection [e]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_S = 3 V	Room	-2	-	-	pC
Off isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1MHz	Room	-84	-	-	dB
Cross talk [e]	X Talk		Room	-83	-	-	
3 dB bandwidth [e]	BW	R_L = 50 Ω, C_L = 5 pF	Room	550	-	-	MHz
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz, V_S = 3 V	Room	2.7	-	-	pF
Drain off capacitance [e]	$C_{D(off)}$		Room	2.6	-	-	
Drain on capacitance [e]	$C_{D(on)}$		Room	7.6	-	-	
Power Requirements							
Power supply current	I+	Digital input = 1.8 V, at one channel V+ = 5 V	Room	4.6	-	-	µA
			Full	-	-	30	
		Digital input 0 or V+	Room	0.001	-	-	
			Full	-	-	2	

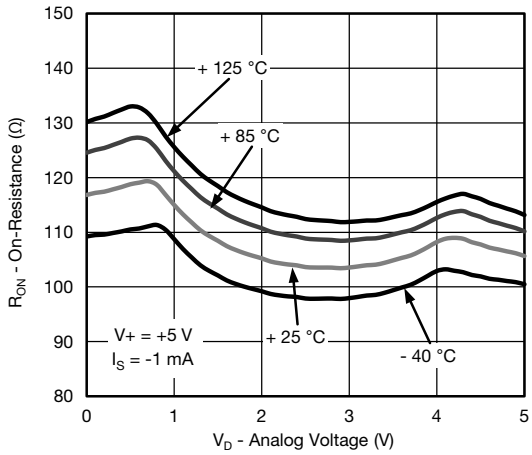
Notes

a. V_{IN} = input voltage to perform proper function
b. Room = 25 °C, Full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The convention where the most negative value is a minimum and the most positive a maximum, is used in this data sheet
e. Guaranteed by design, not subject to production test

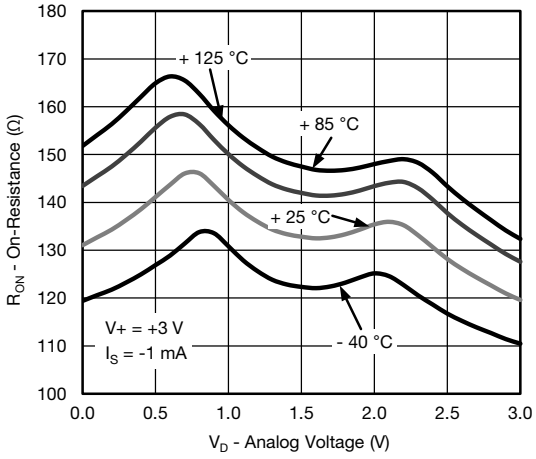
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



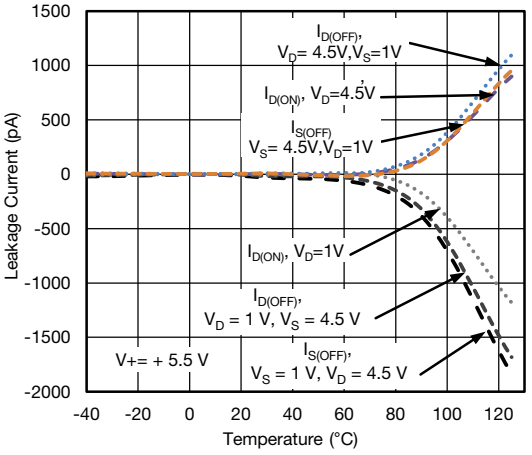
On-Resistance vs. Analog Voltage



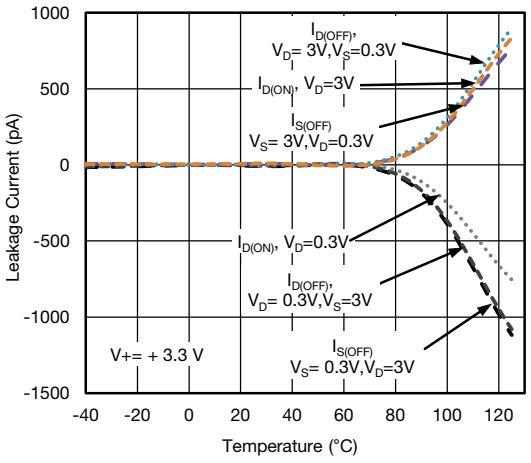
On-Resistance vs. Analog Voltage



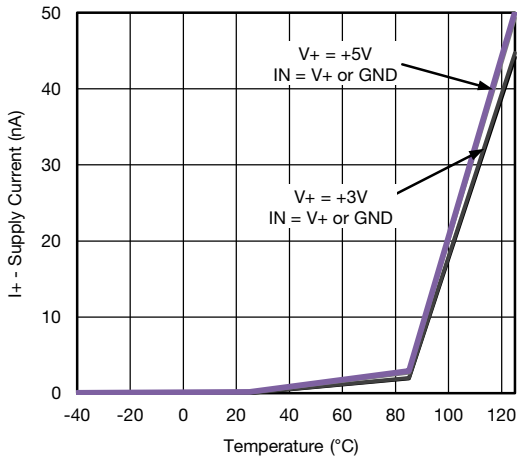
On-Resistance vs. Analog Voltage



Leakage Current vs. Temperature

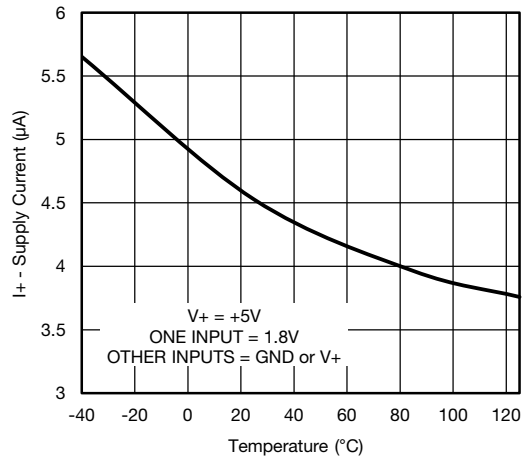


Leakage Current vs. Temperature

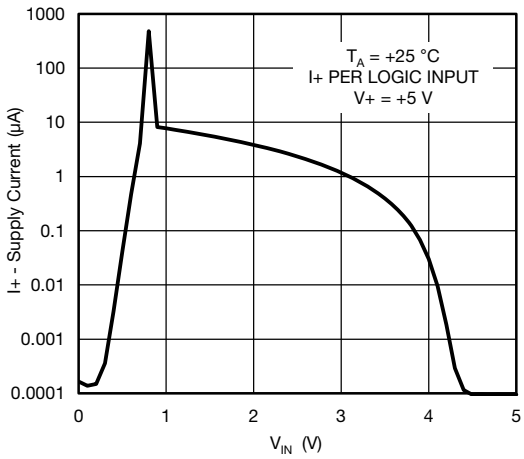


Supply Current vs. Temperature

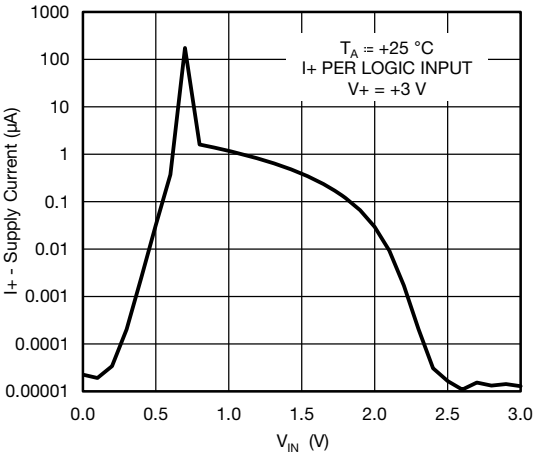
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



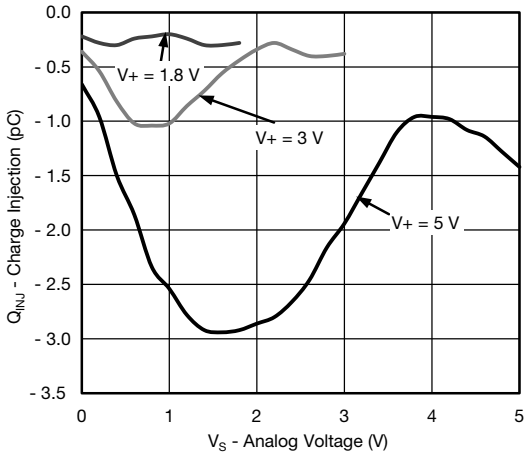
Supply Current vs. Temperature



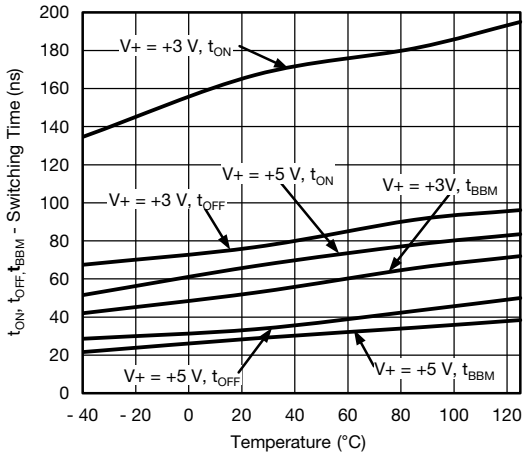
Supply Current vs. V_{IN}



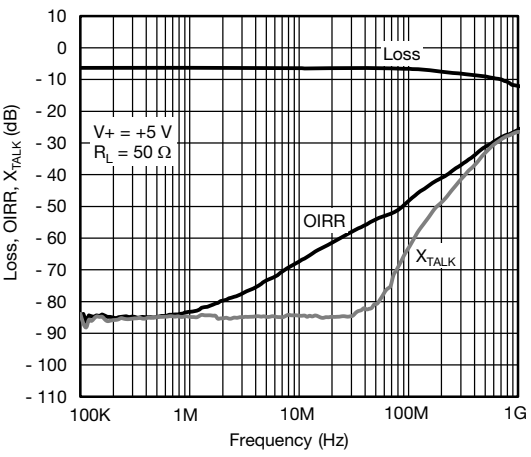
Supply Current vs. V_{IN}



Charge Injection vs. Analog Voltage

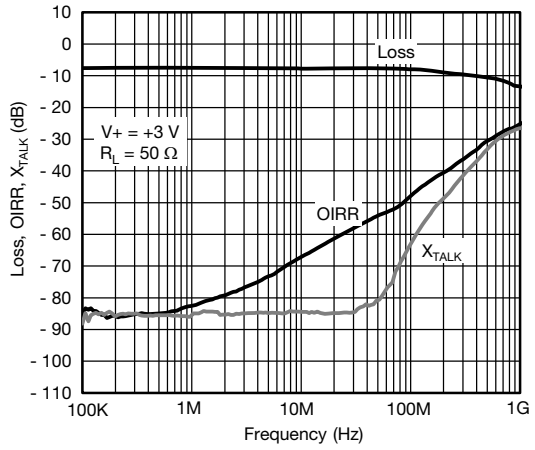


Switching Time vs. Temperature

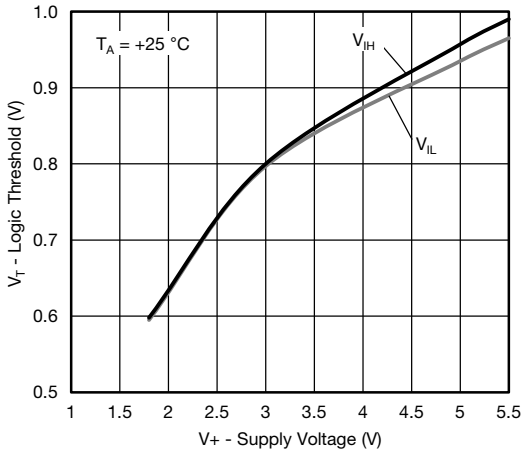


Loss, OIRR, X_{TALK} vs. Frequency

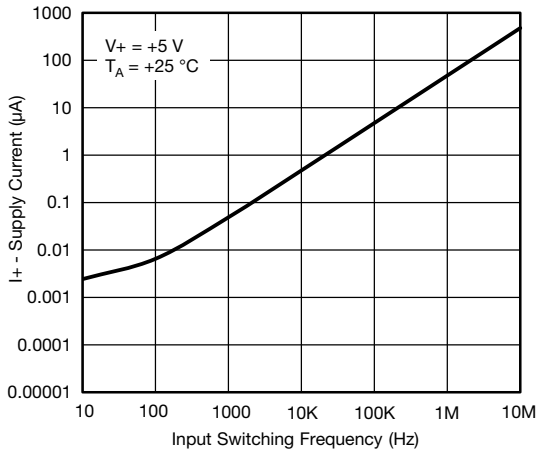
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



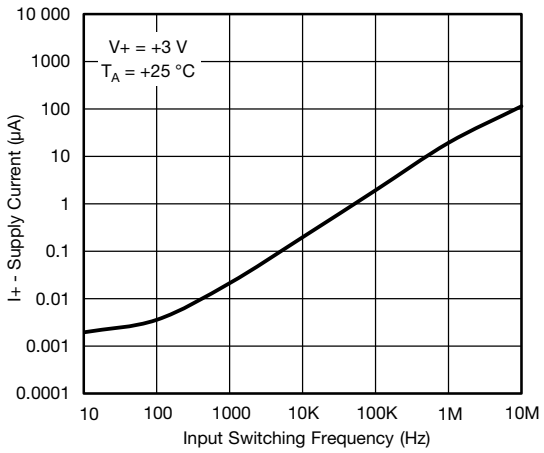
Loss, OIRR, X_{TALK} vs. Frequency



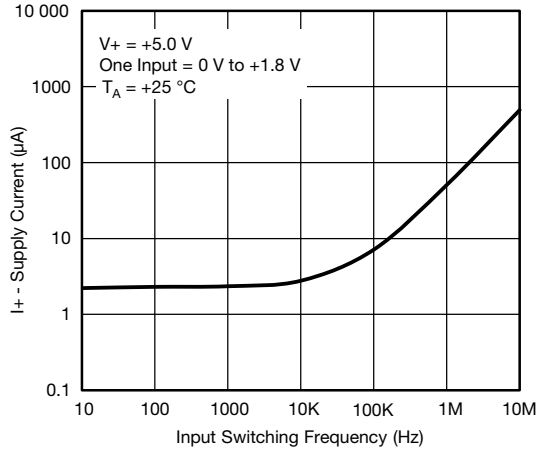
Logic Threshold vs. Supply Voltage



Supply Current vs. Input Switching Frequency

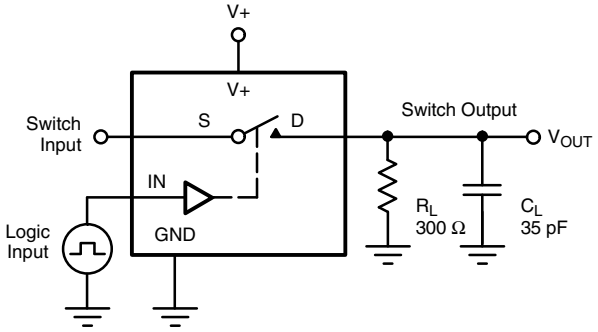


Supply Current vs. Input Switching Frequency



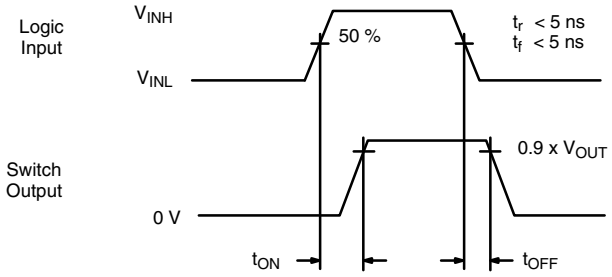
Supply Current vs. Input Switching Frequency

TEST CIRCUIT



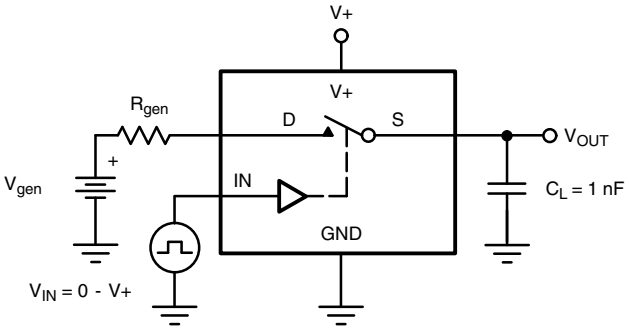
C_L (includes fixture and stray capacitance)

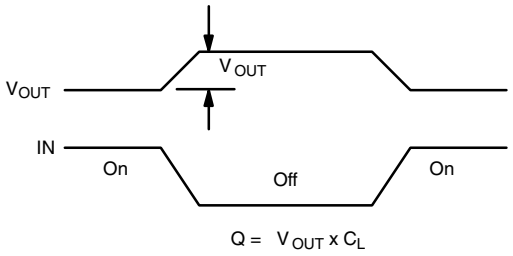
$$V_{OUT} = V_D \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 3 - Switching Time





IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 4 - Charge Injection

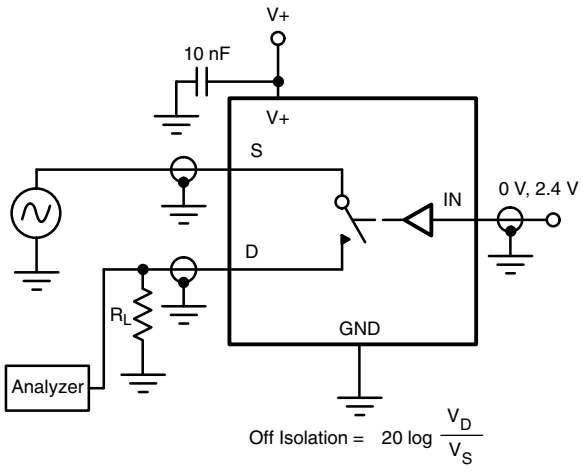


Fig. 5 - Off-Isolation

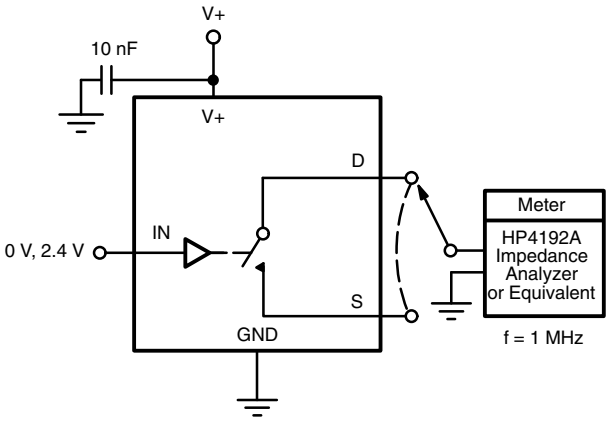
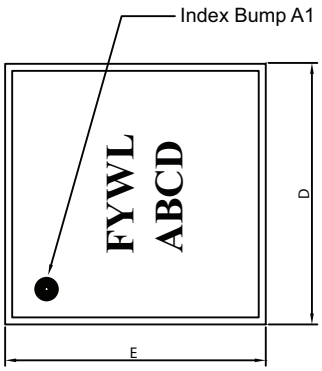


Fig. 6 - Channel Off/On Capacitance

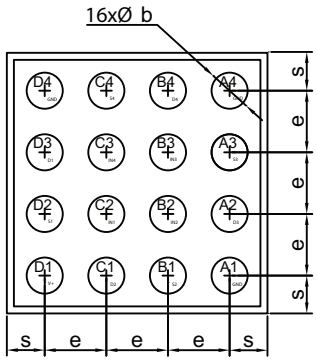
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62962.

WCSP 4 x 4: 16 Bumps

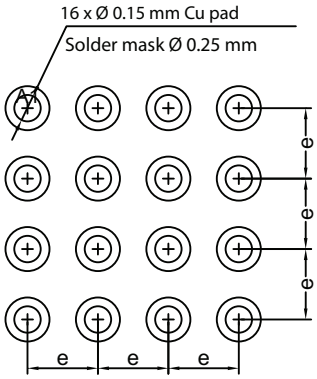
(4 x 4, 0.35 mm pitch, 172 µm bump height, 1.48 mm x 1.48 mm die size)

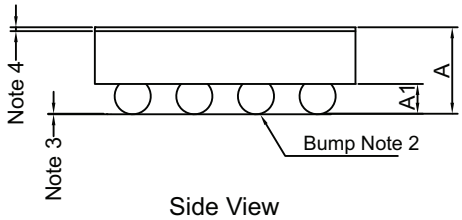


Top View



Bottom View





Side View

Recommended Land Pattern (NSMD)

DWG: 6022

Notes

(1) Laser mark on the silicon die back, coated with an epoxy film
(2) Bumps are SAC405
(3) 0.05 max. co-planarity
(4) Laminate tape thickness is 0.022 mm

DIM.	MILLIMETERS [a]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.444	0.474	0.504	0.0175	0.0187	0.0198
A1	0.146	0.172	0.198	0.0057	0.0068	0.0078
b	0.165	0.205	0.245	0.0065	0.0081	0.0096
e		0.350			0.0138	
s	0.175	0.195	0.215	0.0069	0.0077	0.0085
D	1.400	1.440	1.480	0.0551	0.0567	0.0583
E	1.400	1.440	1.480	0.0551	0.0567	0.0583

Note

a. Use millimeters as the primary measurement.

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