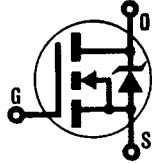


INTERNATIONAL RECTIFIER **IR**

AVALANCHE AND dv/dt RATED

HEXFET® TRANSISTORS

- IRFR010**
- IRFR012**
- IRFU010**
- IRFU012**



N-CHANNEL

50 Volt, 0.20 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. Efficient geometry and unique processing of the HEXFET® design achieve a very low on-state resistance combined with high transconductance and great device ruggedness. HEXFETs® feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The D-Pak (TO-252AA) surface mount package brings the advantages of HEXFETs to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR010 is provided on 16mm tape. The straight lead option IRFU010 of the device is called the I-Pak (TO-251AA).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunications equipment, DC/DC converters, and a wide range of consumer products.

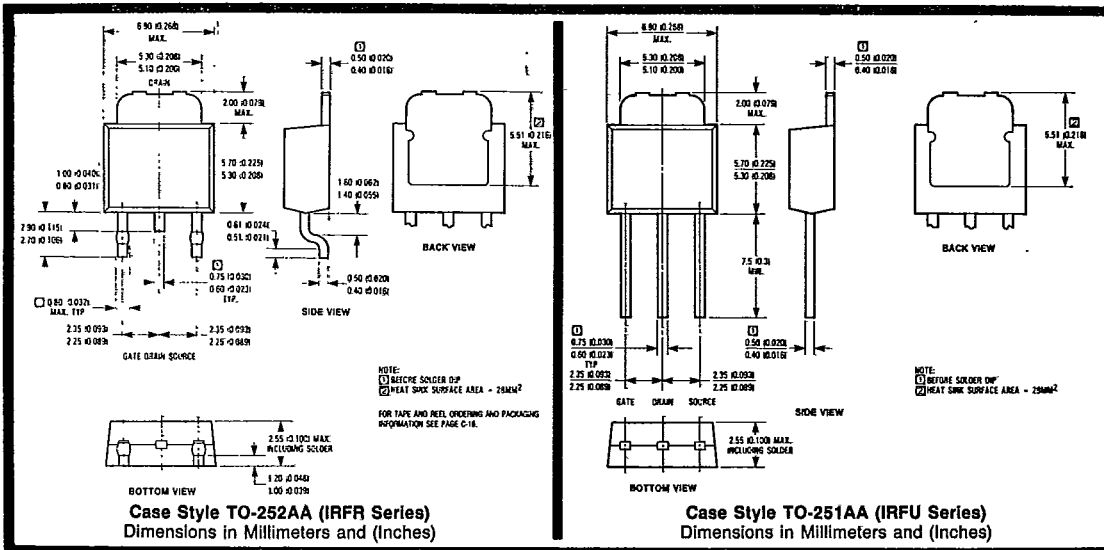
Product Summary

| Part Number | BV _{DSS} | R _{DS(on)} | I _D |
|-------------|-------------------|---------------------|----------------|
| IRFR010 | 50V | 0.20Ω | 8.2A |
| IRFR012 | 50V | 0.30Ω | 6.7A |
| IRFU010 | 50V | 0.20Ω | 8.2A |
| IRFU012 | 50V | 0.30Ω | 6.7A |



FEATURES:

- Surface Mountable (Order As IRFR010)
- Straight Lead Option (Order As IRFU010)
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Excellent Temperature Stability

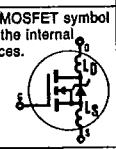


Absolute Maximum Ratings


| Parameter | IFR010, IRFU010 | IFR012, IRFU012 | Units |
|--|---|-----------------|------------------|
| $I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current | 8.2 | 6.7 | A |
| $I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current | 5.2 | 4.2 | A |
| I_{DM} Pulsed Drain Current ① | 33 | 27 | A |
| $P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation | 25 | | W |
| Linear Derating Factor | 0.20 | | W/K ⑤ |
| V_{GS} Gate-to-Source Voltage | ± 20 | | V |
| I_L Avalanche Current ② | 1.5 (See Fig. 14) | | A |
| dv/dt Peak Diode recovery dv/dt ③ | 2.0 (See Fig. 17) | | V/ns |
| T_J Operating Junction Temperature Range | -55 to 150 | | $^\circ\text{C}$ |
| T_{STA} Storage Temperature Range | -55 to 150 | | $^\circ\text{C}$ |
| Lead Temperature | 300 (0.063 in. (1.6mm) from case for 10s) | | $^\circ\text{C}$ |

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

| Parameter | Type | Min. | Typ. | Max. | Units | Test Conditions |
|---|-------------------|------|------|------|---------------|---|
| BV_{DSS} Drain-to-Source Breakdown Voltage | All | 50 | — | — | V | $V_{GS} = 0V, I_D = 250\mu\text{A}$ |
| $R_{DS(on)}$ Static Drain-to-Source On-State Resistance ④ | IFR010 IRFU010 | — | 0.16 | 0.20 | Ω | $V_{GS} = 10V, I_D = 4.2A$ |
| | IFR012 IRFU012 | — | 0.20 | 0.30 | | |
| $I_{D(on)}$ On-State Drain Current ④ | IFR010 IRFU010 | 8.2 | — | — | A | $V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. $V_{GS} = -10V$ |
| | IFR012 IRFU012 | 6.7 | — | — | | |
| $V_{GS(th)}$ Gate Threshold Voltage | ALL | 2.0 | — | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu\text{A}$ |
| g_{fs} Forward Transconductance ④ | ALL | 2.1 | 3.1 | — | S(D) | $V_{DS} \geq 50V, I_{DS} = 3.6A$ |
| I_{DSS} Zero Gate Voltage Drain Current | ALL | — | — | 250 | μA | $V_{DS} = \text{Max. Rating}, V_{GS} = 0V$ |
| | | — | — | 1000 | | $V_{DS} = 0.8 \times \text{Max. Rating}$ $V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| I_{GSS} Gate-to-Source Leakage Forward | ALL | — | — | 500 | nA | $V_{GS} = 20V$ |
| I_{GSS} Gate-to-Source Leakage Reverse | ALL | — | — | -500 | nA | $V_{GS} = -20V$ |
| Q_g Total Gate Charge | ALL | — | 6.7 | 10 | nC | $V_{GS} = 10V, I_D = 7.3A$ $V_{DS} = 0.8 \times \text{Max. Rating}$ See Fig. 16 (Independent of operating temperature) |
| Q_{gs} Gate-to-Source Charge | ALL | — | 1.8 | 2.6 | nC | See Fig. 15 (Independent of operating temperature) |
| Q_{gd} Gate-to-Drain ("Miller") Charge | ALL | — | 3.2 | 4.8 | nC | |
| $t_{d(on)}$ Turn-On Delay Time | ALL | — | 11 | 17 | ns | |
| t_r Rise Time | ALL | — | 33 | 50 | ns | $R_D = 3.3\Omega$ |
| $t_{d(off)}$ Turn-Off Delay Time | ALL | — | 12 | 18 | ns | See Fig. 15 |
| t_f Fall Time | ALL | — | 23 | 35 | ns | (Independent of operating temperature) |
| L_D Internal Drain Inductance | ALL | — | 4.5 | — | nH | Measured from the drain lead, 6mm (0.25 in.) from package to center of die. |
| L_S Internal Source Inductance | ALL | — | 7.5 | — | nH | Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad. |
| C_{iss} Input Capacitance | ALL | — | 250 | — | pF | $V_{GS} = 0V, V_{DS} = 25V$ |
| C_{oss} Output Capacitance | ALL | — | 150 | — | pF | $f = 1.0 \text{ MHz}$ |
| C_{rss} Reverse Transfer Capacitance | ALL | — | 29 | — | pF | See Fig. 10 |



Source-Drain Diode Ratings and Characteristics

| Parameter | Type | Min. | Typ. | Max. | Units | Test Conditions |
|---|------|--|------|------|---------------|--|
| I_S Continuous Source Current (Body Diode) | ALL | — | — | 8.2 | A | Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.  |
| I_{SM} Pulsed Source Current (Body Diode) ① | ALL | — | — | 33 | A | |
| V_{SD} Diode Forward Voltage ④ | ALL | — | — | 1.6 | V | $T_J = 25^\circ\text{C}$, $I_S = 8.2\text{A}$, $V_{GS} = 0\text{V}$ |
| t_{rr} Reverse Recovery Time | ALL | 41 | 86 | 190 | ns | $T_J = 25^\circ\text{C}$, $I_F = 7.3\text{A}$, $dI/dt = 100\text{ A}/\mu\text{s}$ |
| Q_{RR} Reverse Recovery Charge | ALL | 0.15 | 0.33 | 0.78 | μC | |
| t_{on} Forward Turn-On Time | ALL | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$. | | | | |

Thermal Resistance

| | | | | | | |
|--------------------------------|-----|---|-----|-----|-------|------------------------|
| R_{thJC} Junction-to-Case | ALL | — | — | 5.0 | K/W ⑤ | |
| R_{thCS} Case-to-Sink | ALL | — | 1.7 | — | K/W ⑤ | Typical solder mount ⑥ |
| R_{thJA} Junction-to-Ambient | ALL | — | — | 110 | K/W ⑤ | Typical socket mount |



- ① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5)
- ② @ $V_{DD} = 25\text{V}$, Starting $T_J = 25^\circ\text{C}$, $L = 100\mu\text{H}$, $R_G = 25\Omega$, single pulse.
- ③ $I_{SD} \leq 8.2\text{A}$, $dI/dt \leq 130\text{A}/\mu\text{s}$, $V_{DD} \leq 40\text{V}$, $T_J \leq 150^\circ\text{C}$, Suggested $R_G = 24\Omega$
- ④ Pulse width $\leq 300\mu\text{s}$; Duty Cycle $\leq 2\%$
- ⑤ $\text{K/W} = ^\circ\text{C/W}$, $\text{W/K} = \text{W}/^\circ\text{C}$
- ⑥ Mounting pad must cover heatsink surface area. See case style drawing on front page.

The information shown on the following graphs applies also to the IRFU devices.

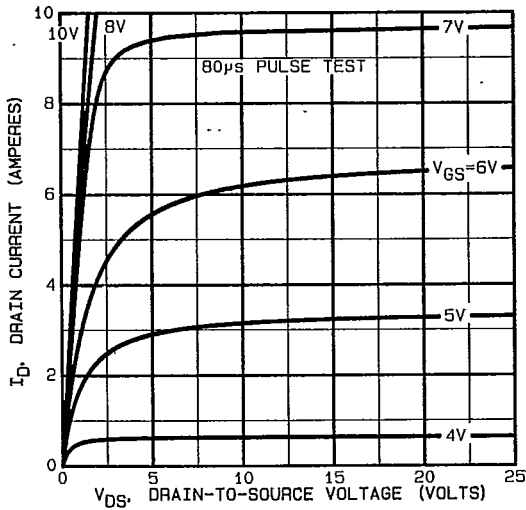


Fig. 1 — Typical Output Characteristics

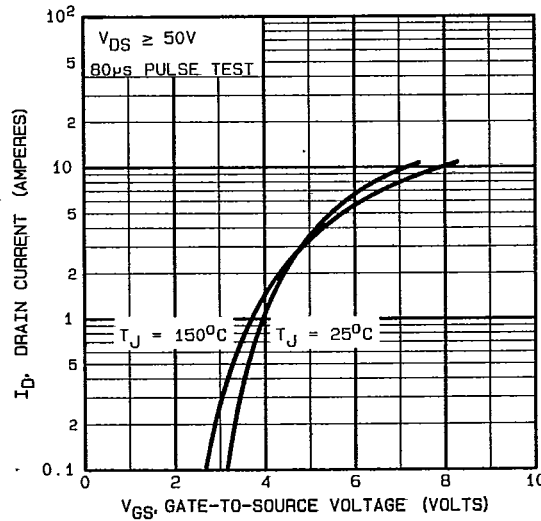


Fig. 2 — Typical Transfer Characteristics

IRFR010, IRFR012, IRFU010, IRFU012 Devices

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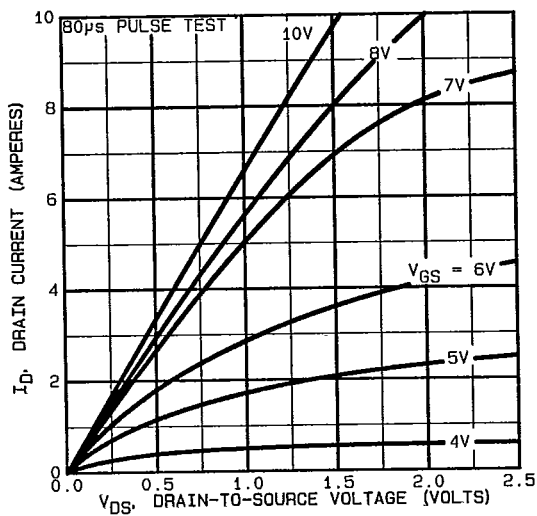


Fig. 3 - Typical Saturation Characteristics

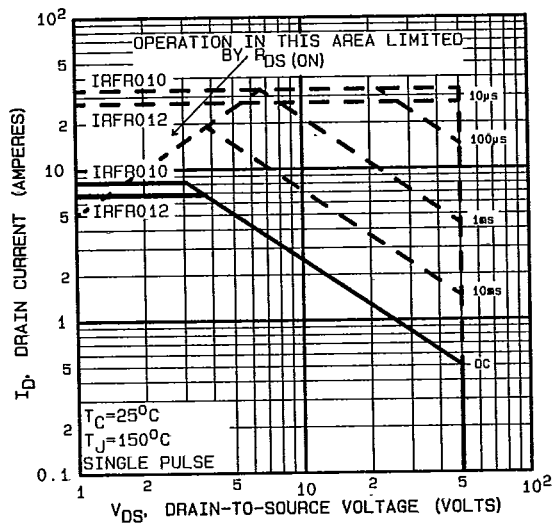


Fig. 4 - Maximum Safe Operating Area

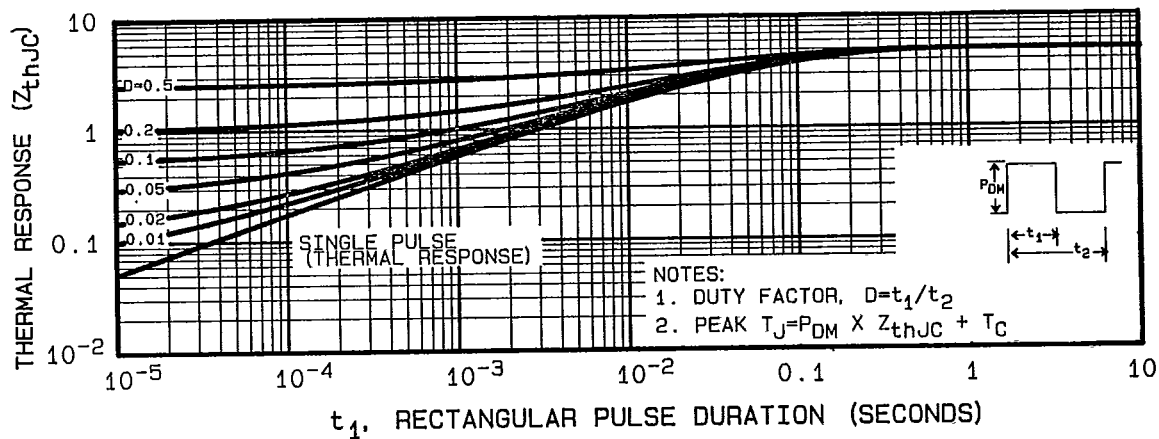


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

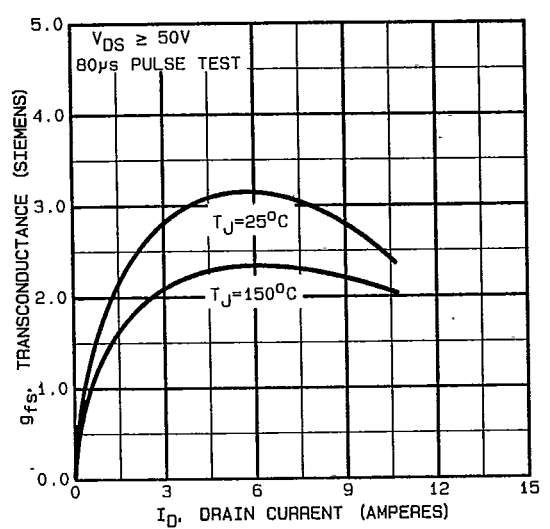


Fig. 6 — Typical Transconductance Vs. Drain Current

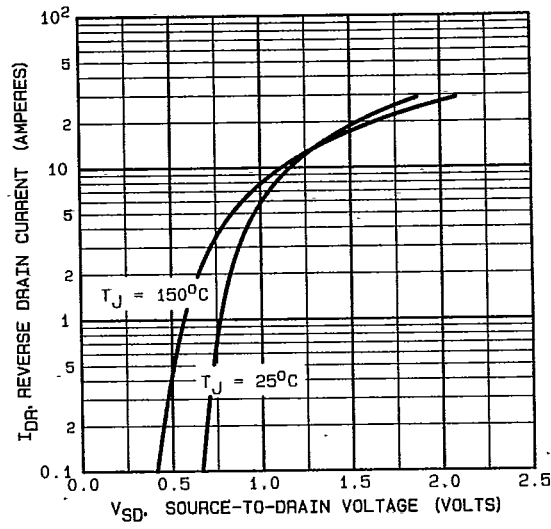


Fig. 7 — Typical Source-Drain Diode Forward Voltage

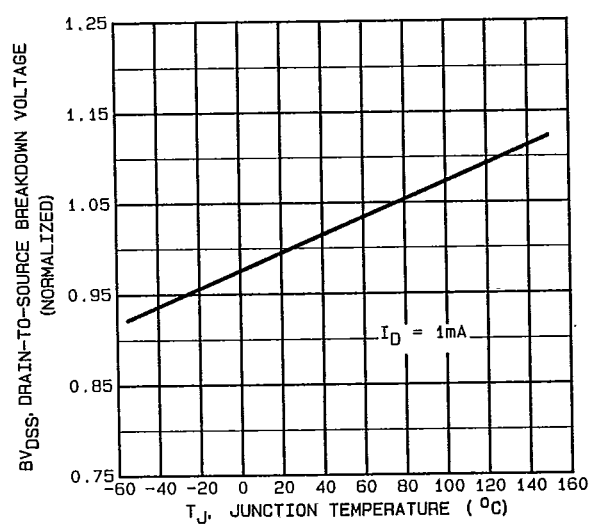


Fig. 8 — Breakdown Voltage Vs. Temperature

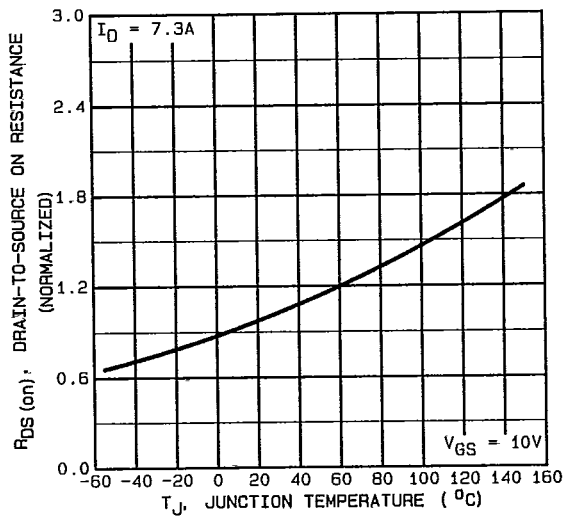


Fig 9 — Normalized On-Resistance Vs. Temperature

IRFR010, IRFR012, IRFU010, IRFU012 Devices

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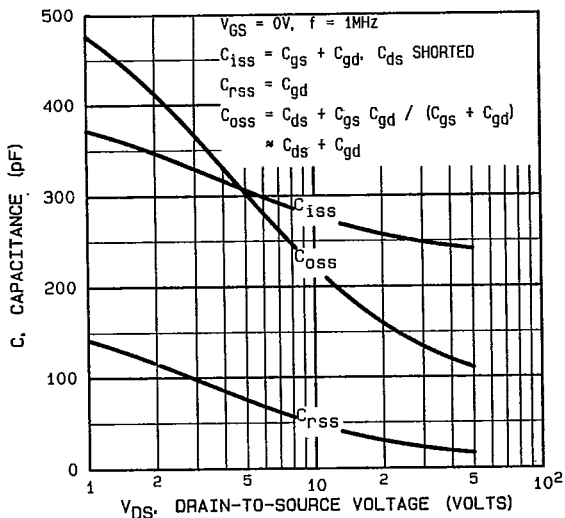


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

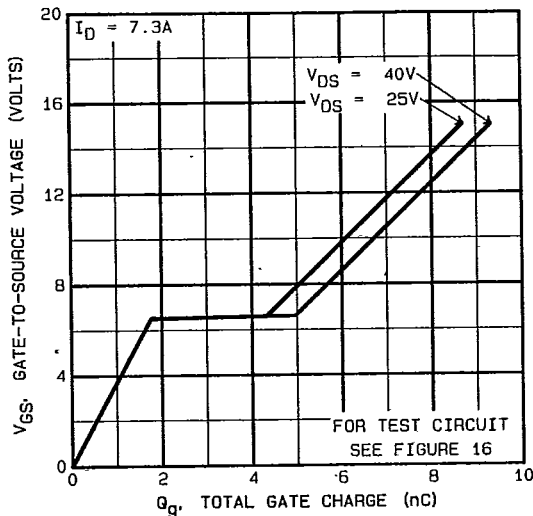


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

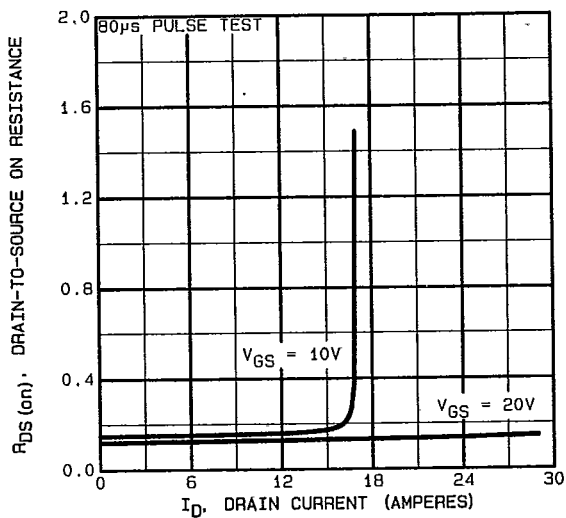


Fig. 12 — Typical On-Resistance Vs. Drain Current

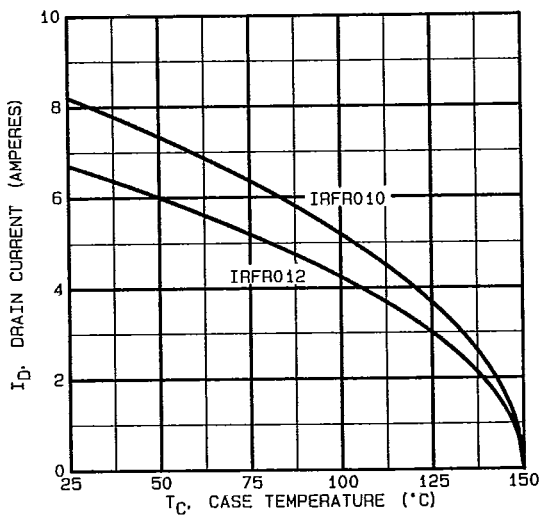


Fig. 13 — Maximum Drain Current Vs. Case Temperature

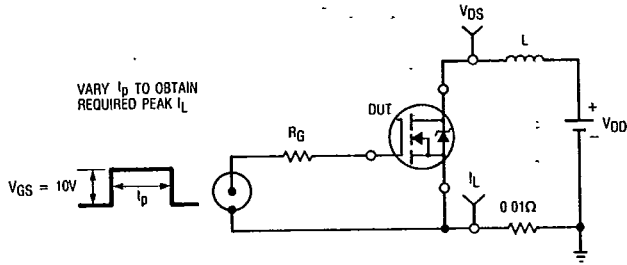


Fig. 14a — Unclamped Inductive Test Circuit

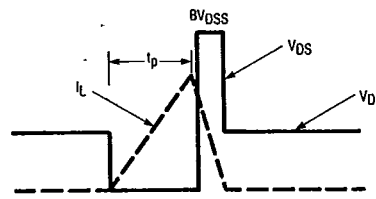


Fig. 14b — Unclamped Inductive Waveforms

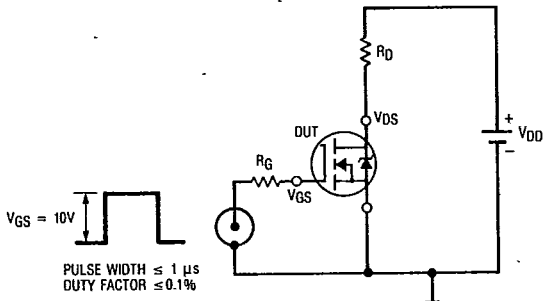


Fig. 15a — Switching Time Test Circuit

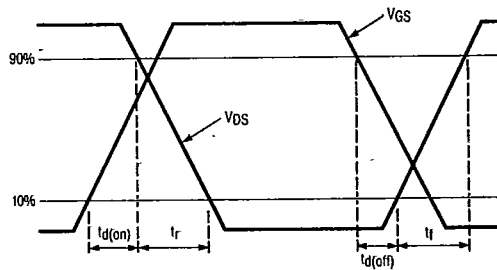


Fig. 15b — Switching Time Waveforms

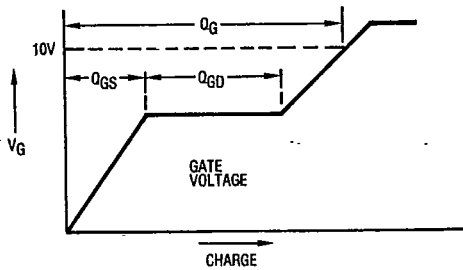


Fig. 16a — Basic Gate Charge Waveform

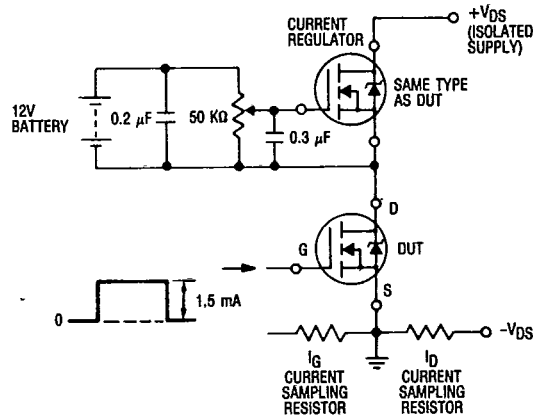


Fig. 16b — Gate Charge Test Circuit

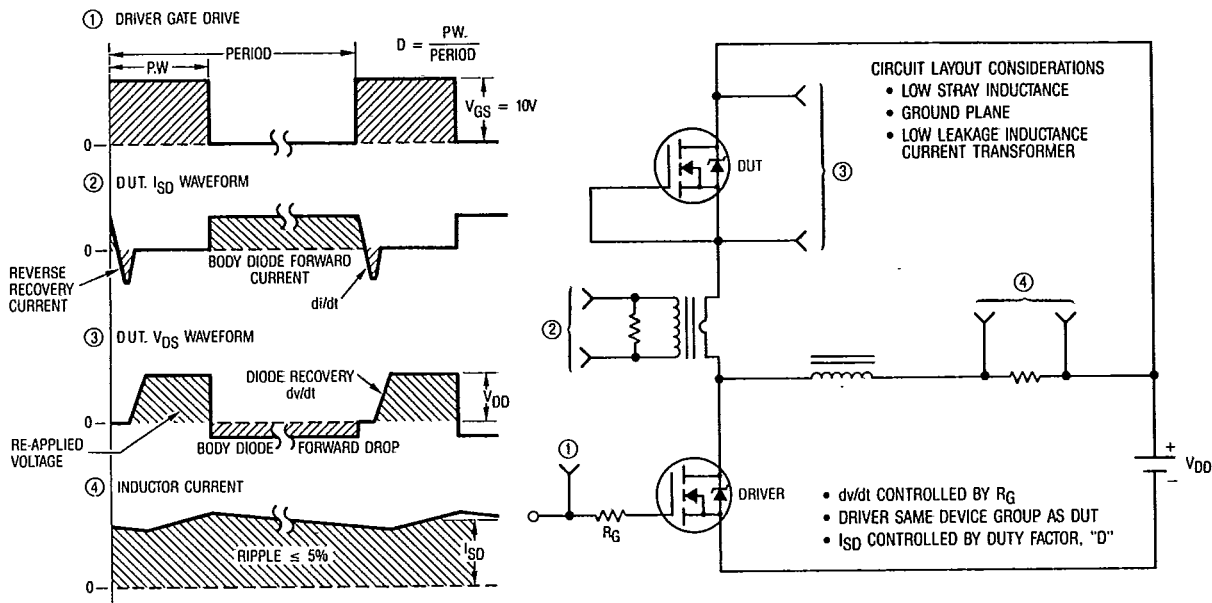


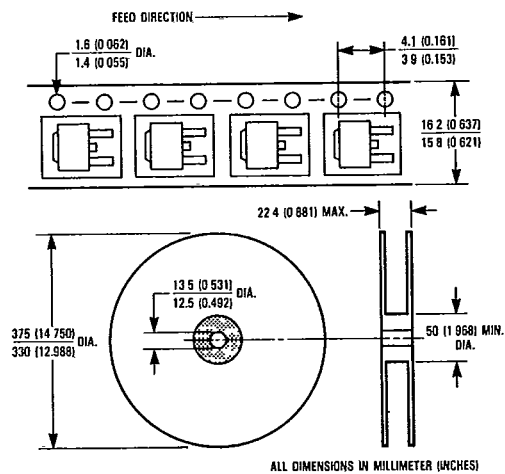
Fig. 17 — Peak Diode Recovery dv/dt Test Circuit

ORDERING INFORMATION

PACKAGING

IRFR Series — Tape and reel
 when ordering, add TR after the part number
 and the quantity
 (order in multiples of 3,000 pieces).

Example: IRFR010TR — 15,000 pieces.



单击下面可查看定价，库存，交付和生命周期等信息

[>>Vishay\(威世\)](#)