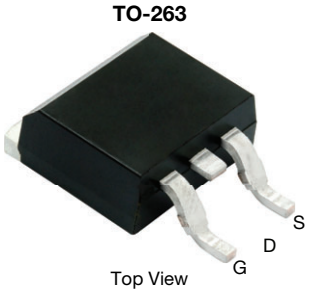
P-Channel 80 V (D-S) MOSFET



FEATURES

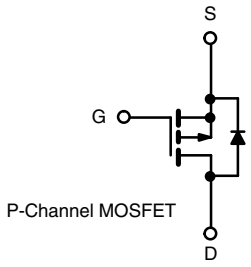
- TrenchFET® power MOSFET
- Package with low thermal resistance
- Maximum 175 °C junction temperature
- Low $R_{DS(on)}$ minimizes power loss from conduction
- Compatible with logic-level gate driving
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

PRODUCT SUMMARY	
V_{DS} (V)	-80
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0061
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4.5 V	0.0086
Q_g typ. (nC)	145
I_D (A)	-150
Configuration	Single

APPLICATIONS

- Battery protection
- Motor drive control
- Load switch



ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free and halogen-free	SUM60061EL-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-80	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current [d] (T_J = 175 °C)	T_C = 25 °C	I_D	-150 [d]	A
	T_C = 70 °C		-150 [d]	
Pulsed drain current (100 µs)		I_{DM}	-250	
Avalanche current	L = 0.1 mH	I_{AS}	-75	
Single pulse avalanche energy [a]		E_{AS}	281	mJ
Power dissipation	T_C = 25 °C [c]	P_D	375	W
	T_C = 125 °C [b]		125	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [b]	R_{thJA}	40	°C/W
Junction-to-case		R_{thJC}	0.4	

Notes

a. Duty cycle ≤ 1 %
b. When mounted on 1" square PCB (FR4 material)
c. See SOA curve for voltage derating
d. Limited by package

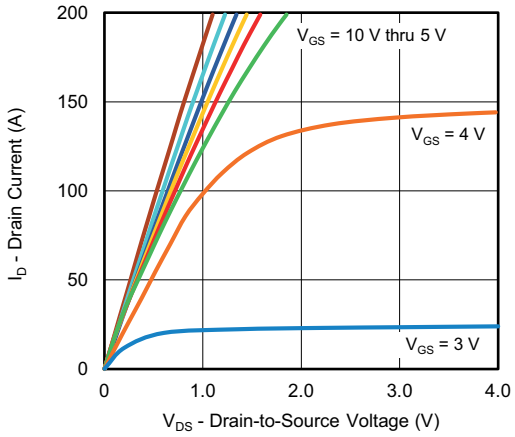
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -10 mA	-80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-1.5	-	-2.5	
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -80 V, V_{GS} = 0 V	-	-	-10	µA
		V_{DS} = -64 V, V_{GS} = 0 V, T_J = 125 °C	-	-	-50	
		V_{DS} = -64 V, V_{GS} = 0 V, T_J = 175 °C	-	-	-250	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≤ -5 V, V_{GS} = -10 V	-30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -20 A	-	0.0051	0.0061	Ω
		V_{GS} = -4.5 V, I_D = -15 A	-	0.0069	0.0086	
Forward transconductance [a]	g_{fs}	V_{DS} = -15 V, I_D = -15 A	-	80	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -40 V, f = 1 MHz	-	9600	-	pF
Output capacitance	C_{oss}		-	3300	-	
Reverse transfer capacitance	C_{rss}		-	110	-	
Total gate charge [c]	Q_g	V_{DS} = -40 V, V_{GS} = -10 V, I_D = -110 A	-	145	218	nC
Gate-source charge [c]	Q_{gs}		-	34	-	
Gate-drain charge [c]	Q_{gd}		-	16	-	
Gate resistance	R_g	f = 1 MHz	0.46	2.3	4.6	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = -40 V, R_L = 0.71 Ω I_D ≅ -20 A, V_{GEN} = -10 V, R_g = 1 Ω	-	25	35	ns
Rise time [c]	t_r		-	20	30	
Turn-off delay time [c]	$t_{d(off)}$		-	90	140	
Fall time [c]	t_f		-	20	30	
Drain-Source Body Diode Characteristics (T_C = 25 °C [b])						
Continuous current	I_S		-	-	-150	A
Pulsed current	I_{SM}		-	-	-250	
Forward voltage [a]	V_{SD}	I_F = -10 A, V_{GS} = 0 V	-	-0.8	-1.5	V
Reverse recovery time	t_{rr}	I_F = -20 A, dI/dt = 100 A/µs	-	90	135	ns
Peak reverse recovery charge	$I_{RM(REC)}$		-	-2.8	-4.2	A
Reverse recovery charge	Q_{rr}		-	145	218	nC

Notes

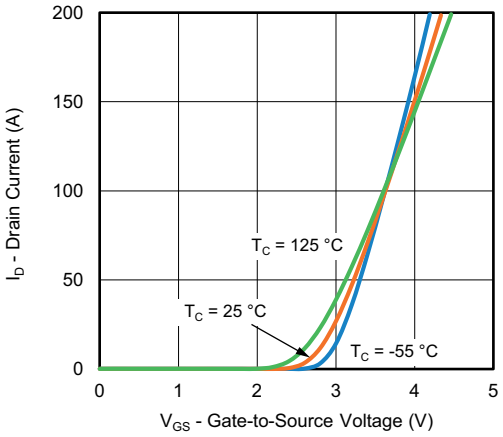
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

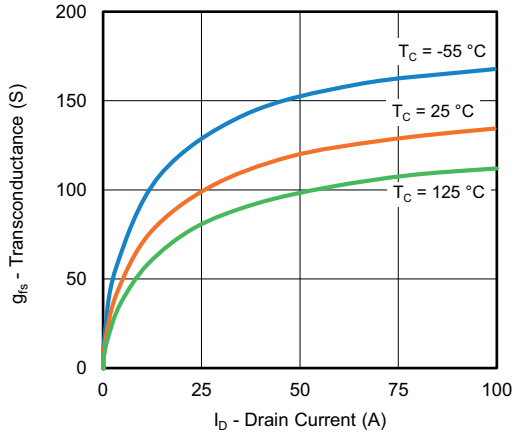
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



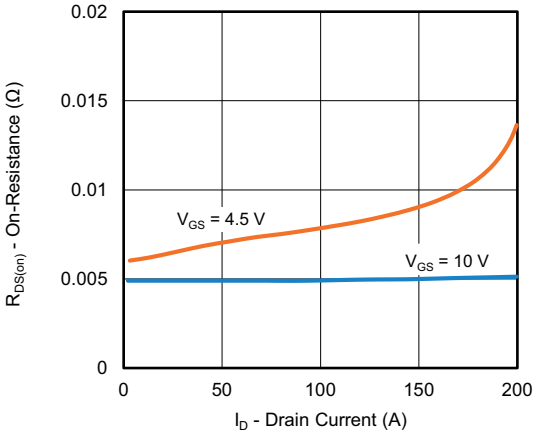
Output Characteristics



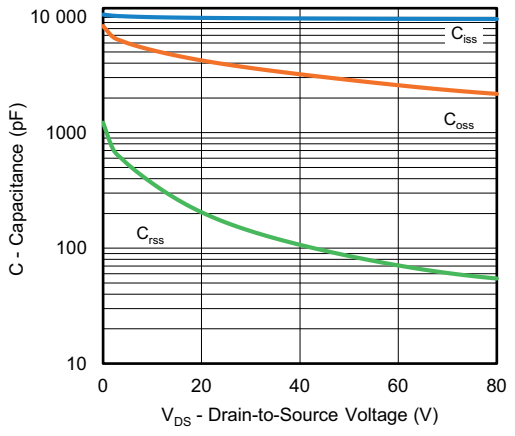
Transfer Characteristics



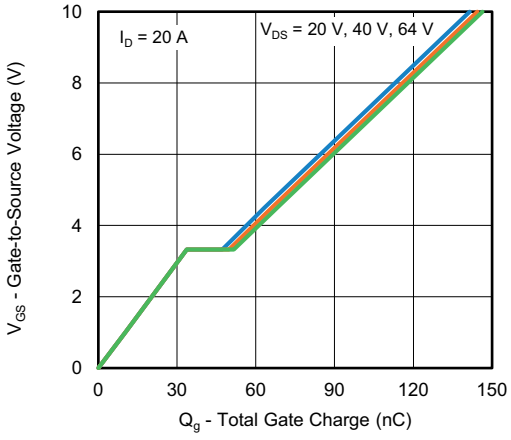
Transconductance



On-Resistance vs. Drain Current

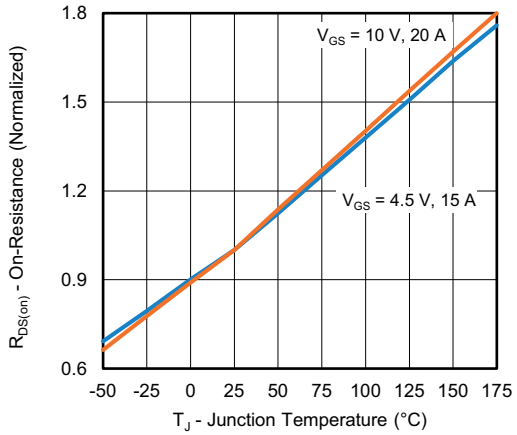


Capacitance

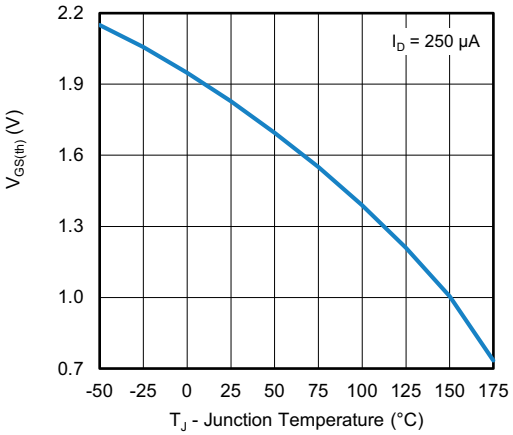


Gate Charge

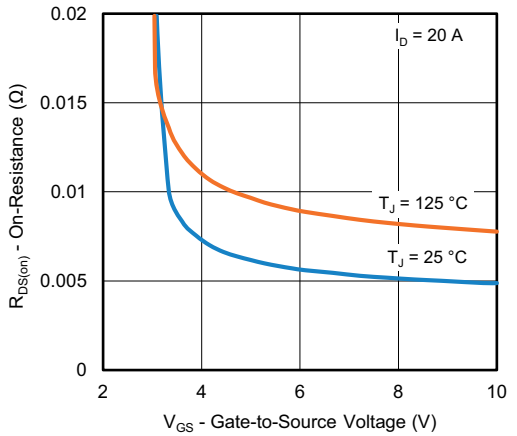
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



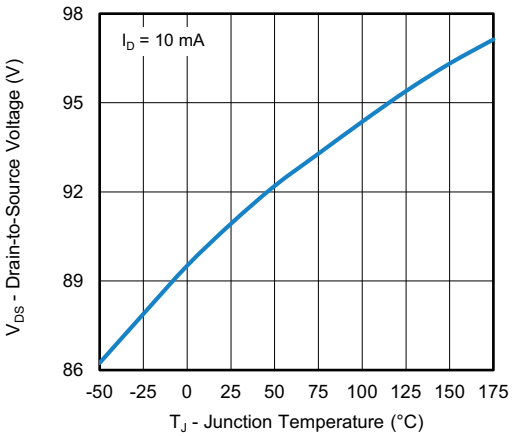
On-Resistance vs. Junction Temperature



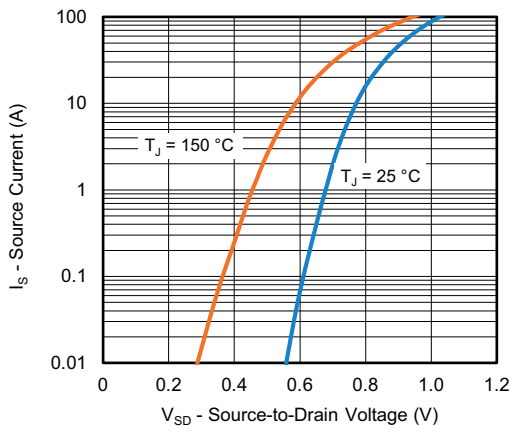
Threshold Voltage



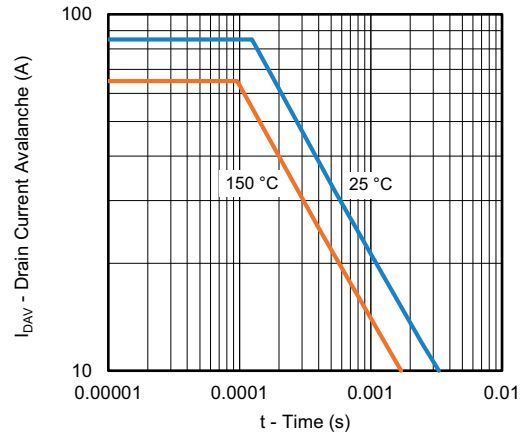
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature

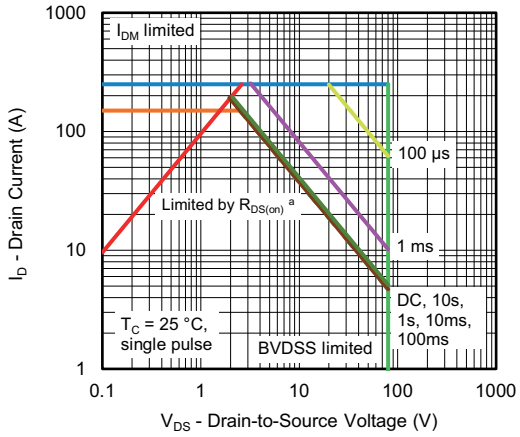


Source Drain Diode Forward Voltage



Avalanche Current vs. Time

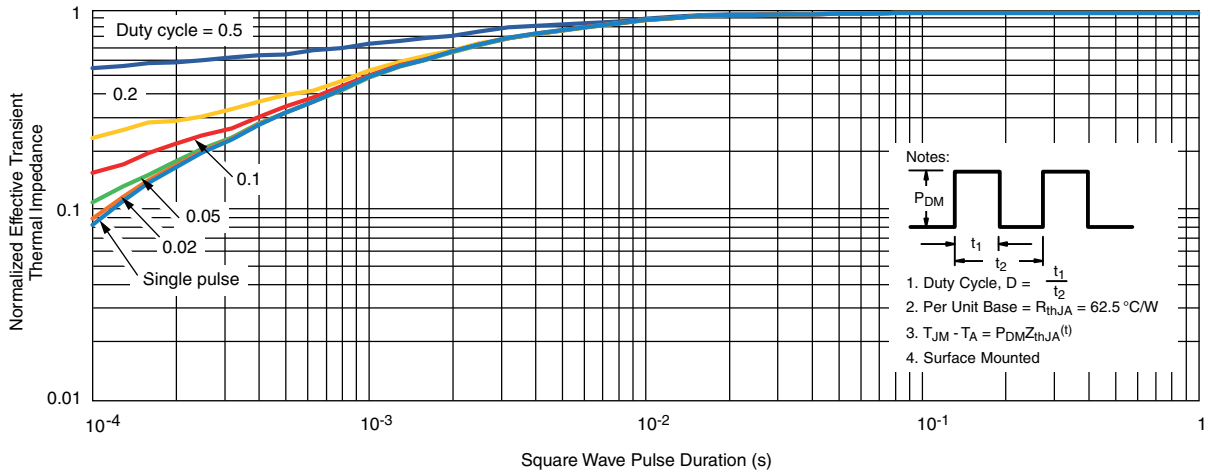
THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

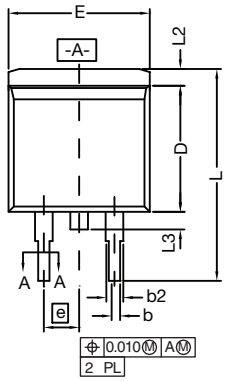


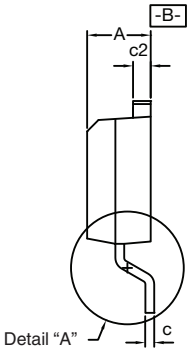
Normalized Thermal Transient Impedance, Junction-to-Case

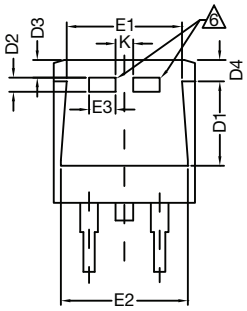
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63024.

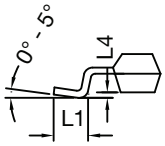
TO-263 (D^2PAK): 3-LEAD

VERSION 1: FACILITY CODE = T

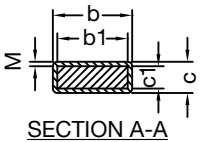








DETAIL A (ROTATED 90°)



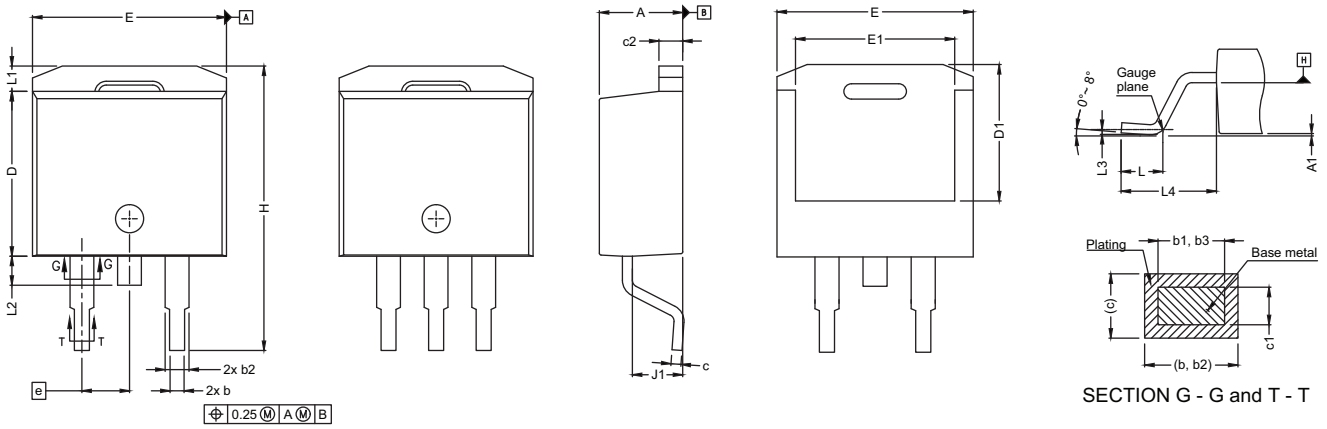
SECTION A-A

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050

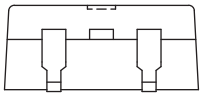
Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

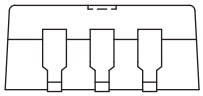
VERSION 2: FACILITY CODE = N



SECTION G - G and T - T



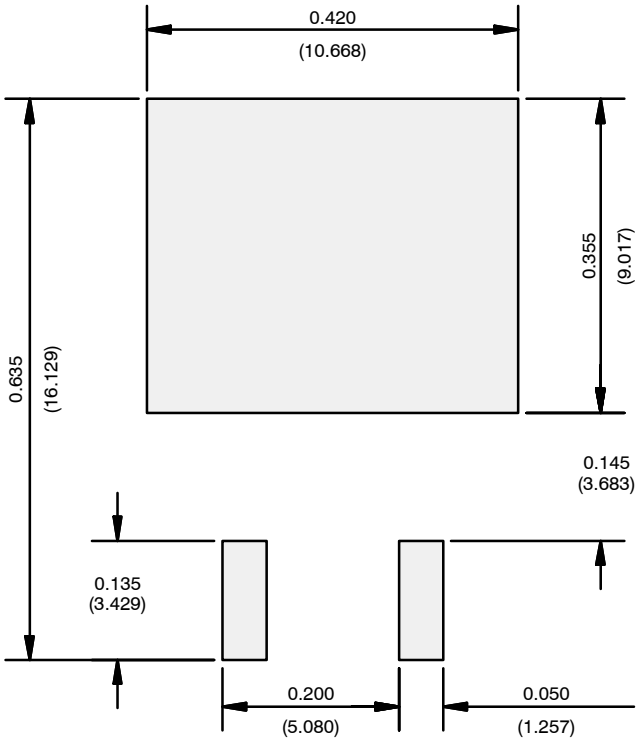
OPTION 1
2 leads



OPTION 2
3 leads

DIM.	MIN.	MAX.
A	4.36	4.56
A1	0	0.25
b	0.70	0.90
b1	0.51	0.89
b2	1.20	1.46
b3	1.17	1.37
c	0.38	0.694
c1	0.38	0.534
c2	1.19	1.34
D	8.60	9.00
D1	6.9	7.5
E	10.15	10.55
E1	8.1	8.7
e	2.54 BSC	
H	15.0	15.6
L	1.9	2.5
L1	-	1.65
L2	-	1.78
L3	0.25 typ.	
L4	4.78	5.28
J1	2.56	2.96
ECN: S24-1080-Rev. L, 28-Oct-2024 DWG: 5843		

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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