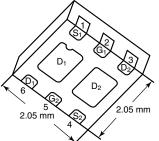


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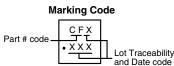
### Dual N-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$ $I_{D}\left(A\right)^{a}$ $Q_{g}$		Q <sub>g</sub> (Typ.)		
	0.028 at V <sub>GS</sub> = 4.5 V	4.5			
12	0.033 at V <sub>GS</sub> = 2.5 V	4.5	6.2 nC		
	0.042 at Vgs = 1.8 V	4.5			

#### PowerPAK SC-70-6 Dual



Ordering Information: SiA910EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

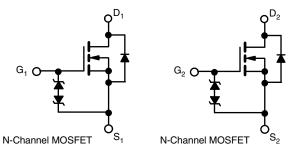


#### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Thermally Enhanced PowerPAK<sup>®</sup> SC-70 Package
  - Small Footprint Area
  - Low On-Resistance
- Typical ESD Protection: 2400 V
- 100 % R<sub>a</sub> Tested
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

#### APPLICATIONS

- Load Switch for Portable Applications
- High Frequency DC/DC Converter
- DC/DC Converter



ABSOLUTE MAXIMUM RATIN	<b>IGS</b> (T <sub>A</sub> = 25 °C	, unless oth	erwise noted)		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	12	V	
Gate-Source Voltage		V <sub>GS</sub>	± 8	v	
	T <sub>C</sub> = 25 °C		4.5 <sup>a</sup>		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	4.5 <sup>a</sup>		
	T <sub>A</sub> = 25 °C		4.5 <sup>a, b, c</sup>		
	T <sub>A</sub> = 70 °C		4.5 <sup>a, b, c</sup>	A	
Pulsed Drain Current		I <sub>DM</sub>	20		
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		4.5 <sup>a</sup>		
	T <sub>A</sub> = 25 °C	۱ <sub>S</sub>	1.6 <sup>b, c</sup>		
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		7.8		
	T <sub>C</sub> = 70 °C	P <sub>D</sub>	5	w	
	T <sub>A</sub> = 25 °C		1.9 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		1.2 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260		

#### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	R <sub>thJA</sub>	52	65	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	12.5	16	0/10	

Notes:

a. Package limited

b. Surface mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 110 °C/W.



ROHS COMPLIANT HALOGEN FREE

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	•						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$	12			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050 ··· A		8		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 2.5			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	0.4		1	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 8 V$			± 5	-	
		$V_{DS} = 0 V, V_{GS} = \pm 4.5 V$			± 0.5		
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 12 V, V <sub>GS</sub> = 0 V			1	μΑ	
	I <sub>DSS</sub>	$V_{DS} = 12 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$			10	1	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5$ V, $V_{GS}$ = 4.5 V	10			Α	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.2 A		0.023	0.028	Ω	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 4.8 A		0.027	0.033		
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 2.5 A		0.035	0.042		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.2 A		23		S	
Dynamic <sup>b</sup>			L		L	1	
Input Capacitance	C <sub>iss</sub>		1	455		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 0 V, f = 1 MHz		190			
Reverse Transfer Capacitance	C <sub>rss</sub>			150			
·		$V_{DS} = 6 V, V_{GS} = 8 V, I_D = 6.8 A$		10.5	16	- nC	
Total Gate Charge	Qg			6.2	9.5		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 6 V, V_{GS} = 4.5 V, I_{D} = 6.8 A$		0.8			
Gate-Drain Charge	Q <sub>gd</sub>			1.6			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.8	4	8	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			10	15		
Rise Time	t <sub>r</sub>			12	20	- ns 	
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{DD} = 6 \text{ V}, \text{ R}_{L} = 1.1 \Omega$ $I_{D} \cong 5.4 \text{ A}, \text{ V}_{\text{GEN}} = 4.5 \text{ V}, \text{ R}_{g} = 1 \Omega$		25	40		
Fall Time	t <sub>f</sub>	$ID = 3.4 \text{ A}, V_{GEN} = 4.3 \text{ V}, \Pi_g = 1.22$		12	20		
Turn-On Delay Time	t <sub>d(on)</sub>			5	10		
Rise Time	t <sub>r</sub>			10	15		
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{DD} = 6 \text{ V}, \text{ R}_{L} = 1.1 \Omega$ $I_{D} \approx 5.4 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		20	30		
Fall Time	t <sub>f</sub>	$D = 3.4 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ H}_{\text{g}} = 1.22$		10	15		
Drain-Source Body Diode Characteristic	s	l			1	1	
Continuous Source-Drain Diode Current	۱ <sub>S</sub>	T <sub>C</sub> = 25 °C			4.5	A	
Pulse Diode Forward Current	I <sub>SM</sub>			T	20		
Body Diode Voltage	V <sub>SD</sub>	$I_{\rm S} = 5.4 \text{ A}, V_{\rm GS} = 0 \text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			25	50	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1		10	20	nC	
Reverse Recovery Fall Time	ta	I <sub>F</sub> = 5.4 A, dl/dt = 100 A/ $\mu$ s, T <sub>J</sub> = 25 °C		13		- ns	
Reverse Recovery Rise Time	t <sub>b</sub>			12			

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing.

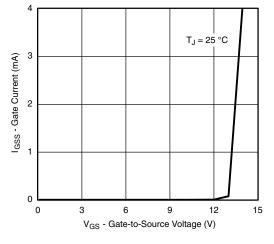
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For technical questions, contact: <a href="mailto:pmostechsupport@vishay.com">pmostechsupport@vishay.com</a>

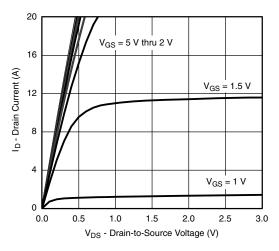


### SiA910EDJ Vishay Siliconix

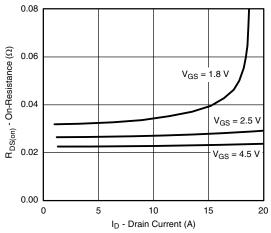
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Gate Current vs. Gate-Source Voltage



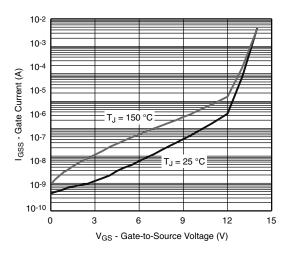
**Output Characteristics** 



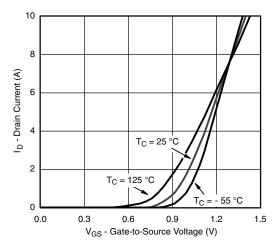
**On-Resistance vs. Drain Current and Gate Voltage** 

Document Number: 65535

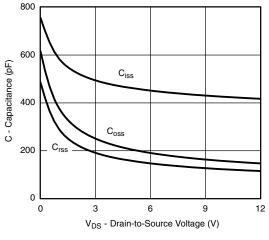
S13-0460-Rev. B, 04-Mar-13



Gate Current vs. Gate-Source Voltage



**Transfer Characteristics** 



Capacitance

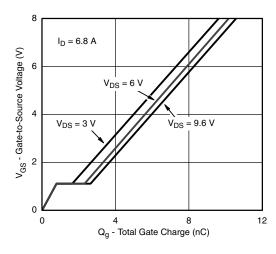
#### \_\_\_\_\_\_ 0 l 10 15 20 0 D - Drain Current (A)

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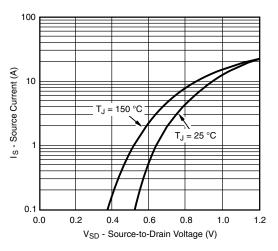




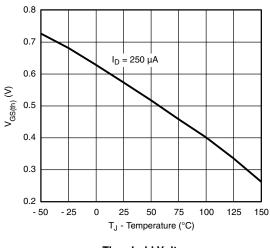
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



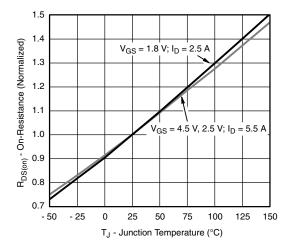
Gate Charge



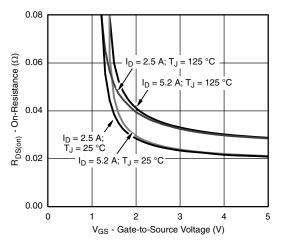
Source-Drain Diode Forward Voltage



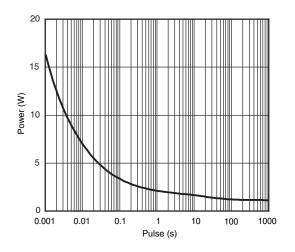
Threshold Voltage



**On-Resistance vs. Junction Temperature** 



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)

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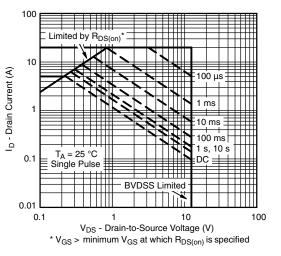
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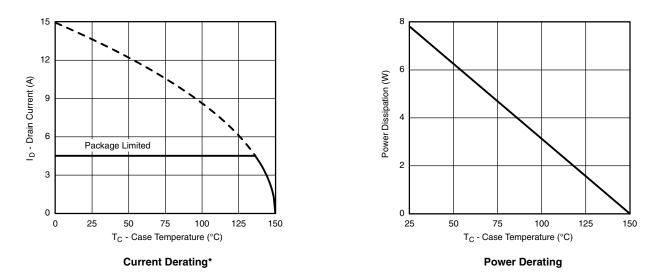


### SiA910EDJ Vishay Siliconix

### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient

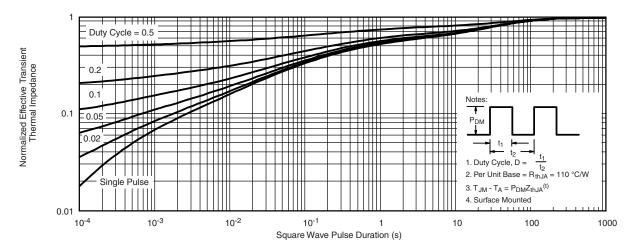


\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

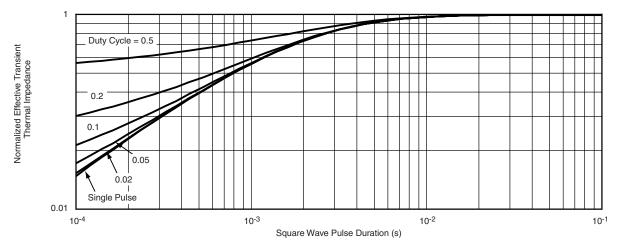


### **Vishay Siliconix**

### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

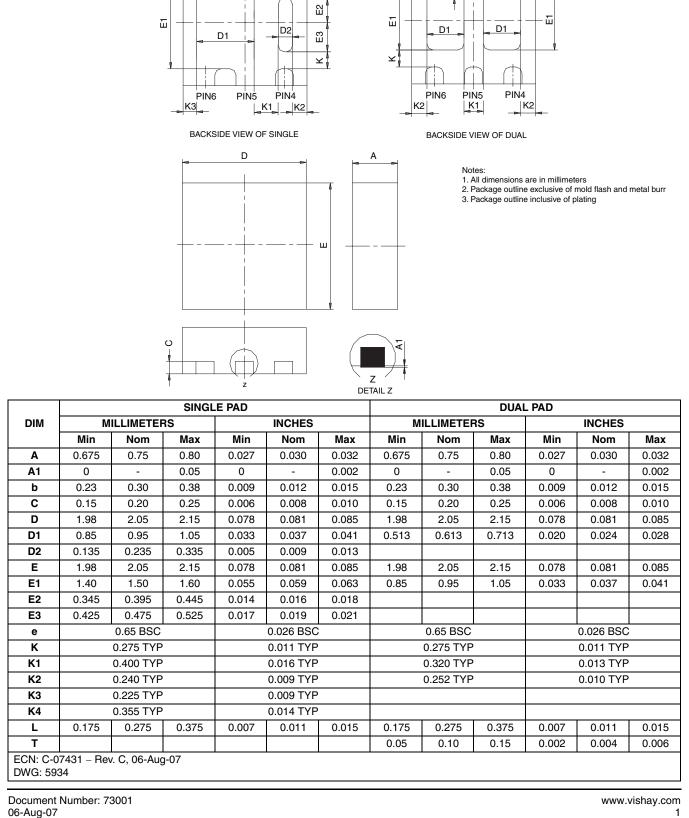


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?65535">www.vishay.com/ppg?65535</a>.



### PowerPAK<sup>®</sup> SC70-6L

# b PIN2 PIN1 PIN3 \_ ₹

# **Package Information**

b

PIN3

\_\_ ₿

PIN2

PIN1

¥

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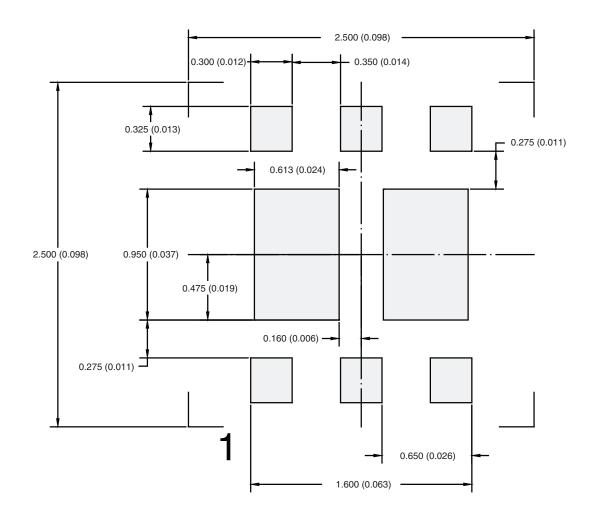


# **Application Note 826**

Vishay Siliconix



### **RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual**



Dimensions in mm (inches)

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