8-Channel, Dual 4-Channel, Triple 2-Channel Multiplexers

DESCRIPTION

The DG9251, DG9252, and DG9253 are high precision single and dual supply CMOS analog multiplexers. DG9251 is an 8-channel multiplexer, the DG9252 is a dual 4-channel multiplexer, and the DG9253 is a triple 2-channel multiplexer or triple SPDT.

Designed to operate from a + 2.7 V to + 16 V single supply or from a ± 2.7 V to ± 5 V dual supplies, the DG9251, DG9252, and DG9253 are fully specified at + 16 V, + 5 V and ± 5 V. All control logic inputs have guaranteed 1.4 V high limit when operating from + 5 V or ± 5 V supplies and 1.65 V when operating from a + 16 V supply.

The DG9251, DG9252, and DG9253 are precision multiplexers of low leakage, low charge injection, and lowparasitic capacitance. They conduct equally well in bothdirections, offer rail to rail analog signal handling and can beused both as multiplexers as well as de-multiplexers.The DG9251, DG9252, and DG9253 operating temperature is specified from - 40 °C to + 85 °C and are available in ultra compact 1.8 mm x 2.6 mm miniQFN16 packages.

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- + 2.7 V to + 16 V single supply operation
  ± 2.7 V to ± 5 V dual supply operation
- Fully specified at + 16 V, + 5 V, ± 5 V
- Low charge injection (< 4.1 pC typ.)
- High bandwidth: 314 MHz (DG9251)
  449 MHz (DG9252)
  480 MHz (DG9253)
- Low switch capacitance ($C_{s(off)}$ 2.7 pF typ.)
- Good isolation and crosstalk performance (typ. - 45 dB at 100 MHz)
- MiniQFN16 package (1.8 mm x 2.6 mm)
- **Compliant to RoHS Directive 2002/95/EC**

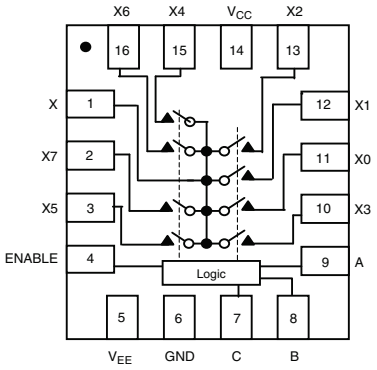
Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Data acquisition
- Medical and healthcare devices
- Control and automation equipments
- Test instruments
- Touch panels
- Consumer

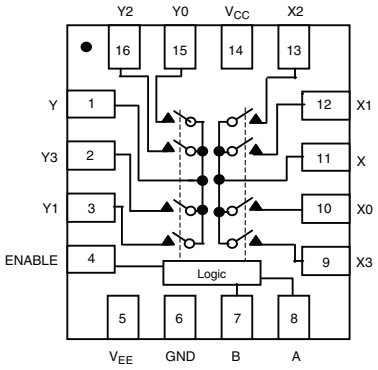
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG9251
mQFN-16



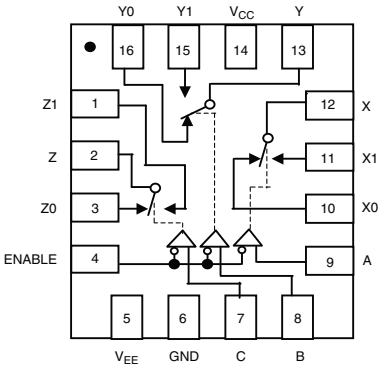
Top View

DG9252
mQFN-16

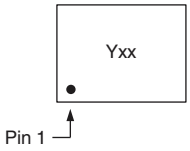


Top View

DG9253
mQFN-16



Top View



Device Marking: 8xx for DG9251
(miniQFN16) Hxx for DG9252
Jxx for DG9253
xx = Date/Lot Traceability Code

TRUTH TABLE

Enable Input	Select Inputs			On Switches		
	C	B	A	DG9251	DG9252	DG9253
H	X	X	X	All Switches Open	All Switches Open	All Switches Open
L	L	L	L	X to X0	X to X0, Y to Y0	X to X0, Y to Y0, Z to Z0
L	L	L	H	X to X1	X to X1, Y to Y1	X to X1, Y to Y0, Z to Z0
L	L	H	L	X to X2	X to X2, Y to Y2	X to X0, Y to Y1, Z to Z0
L	L	H	H	X to X3	X to X3, Y to Y3	X to X1, Y to Y1, Z to Z0
L	H	L	L	X to X4	X to X0, Y to Y0	X to X0, Y to Y0, Z to Z1
L	H	L	H	X to X5	X to X1, Y to Y1	X to X1, Y to Y0, Z to Z1
L	H	H	L	X to X6	X to X2, Y to Y2	X to X0, Y to Y1, Z to Z1
L	H	H	H	X to X7	X to X3, Y to Y3	X to X1, Y to Y1, Z to Z1

ORDERING INFORMATION

Temp. Range	Package	Part Number
DG9251, DG9252, DG9253		
- 40 °C to 125 °C[a]	16-Pin miniQFN	DG9251EN-T1-E4
		DG9252EN-T1-E4
		DG9253EN-T1-E4

Notes:
a. - 40 °C to 85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Limit	Unit
V_{CC} to V_{EE}		18	V
GND to V-		9	
Digital Inputs[a], V_S, V_D		(V-) - 0.3 to (V+) + 0.3 or 30 mA, whichever occurs first	
Continuous Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed 1 ms, 10 % duty cycle)		100	
Storage Temperature		- 65 to 150	°C
Power Dissipation[b]	16-Pin miniQFN[c, d]	525	mW
Thermal Resistance[b]	16-Pin miniQFN[d]	152	°C/W
Latch-up (per JESD78)		> 300	mA

Notes:
a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.6 mW/°C above 70 °C.
d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (for Dual Supplies)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{CC} = + 5 V, V_{EE} = - 5 V, $V_{IN(A, B, C and ENABLE)}$ = 1.4 V, 0.3 V[a]		Temp.[b]	Typ.[c]	- 40 °C to 125 °C Min.[d]	- 40 °C to 125 °C Max.[d]	- 40 °C to 85 °C Min.[d]	- 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		- 5	5	- 5	5	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = - 3 V, 0 V, + 3 V		Room Full	90		182 252		182 223	Ω
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = ± 3 V		Room Full	3.1		6 10		6 8	Ω
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = - 3 V, 0 V, + 3 V		Room Full	32.4		44 64		44 61	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_{CC} = 5.5 V, V_{EE} = - 5.5 V, V_D = ± 4.5 V, V_S = ± 4.5 V		Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	nA
	$I_{D(off)}$			Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	nA
Channel On Leakage Current	$I_{D(on)}$	V_{CC} = 5.5 V, V_{EE} = - 5.5 V, V_S = V_D = ± 4.5 V		Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	nA
Digital Control										
$V_{IN(A, B, C and ENABLE)}$ Low	V_{IL}			Full			0.3		0.3	V
$V_{IN(A, B, C and ENABLE)}$ High	V_{IH}			Full		1.4		1.4		V
Input Current, V_{IN} Low	I_{IL}	$V_{IN(A, B, C and ENABLE)}$ under test = 0.3 V		Full	0.01	- 1	1	- 1	1	µA
Input Current, V_{IN} High	I_{IH}	$V_{IN(A, B, C and ENABLE)}$ under test = 1.4 V		Full	0.01	- 1	1	- 1	1	µA
Input Capacitance[e]	C_{IN}	f = 1 MHz		Room	2.4					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see figure 1, 2, 3		Room Full	88		236 281		236 251	ns
Enable Turn-On Time	t_{ON}			Room Full	158		250 455		250 369	ns
Enable Turn-Off Time	t_{OFF}			Room Full	40		125 136		125 131	ns
Break-Before-Make Time Delay	t_D			Room Full	32	13		13		ns
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 15 pF	f = 100 kHz	Room	< - 90					dB
			f = 10 MHz	Room	- 64					dB
			f = 100 MHz	Room	- 45					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		f = 100 kHz	Room	< - 90					dB
			f = 10 MHz	Room	- 67					dB
			f = 100 MHz	Room	- 48					dB
Bandwith, 3 dB	BW	R_L = 50 Ω	DG9251	Room	314					MHz
			DG9252	Room	449					MHz
			DG9253	Room	480					MHz
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Room	4.1					pC
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	DG9251	Room	2.7					pF
			DG9252	Room	2.2					pF
			DG9253	Room	2.0					pF
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz	DG9251	Room	10.7					pF
			DG9252	Room	6.6					pF
			DG9253	Room	4.6					pF
Channel On Capacitance[e]	$C_{D(on)}$	f = 1 MHz	DG9251	Room	14.6					pF
			DG9252	Room	9.8					pF
			DG9253	Room	8.6					pF
Total Harmonic Distortion[e]	THD	Signal = 1 V_{RMS}, 20 Hz to 20 kHz, R_L = 600 Ω		Room	0.2					%

SPECIFICATIONS (for Dual Supplies)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{CC} = + 5 V, V_{EE} = - 5 V $V_{IN(A, B, C \text{ and ENABLE})}$ = 1.4 V, 0.3 V[a]	Temp.[b]	Typ.[c]	- 40 °C to 125 °C Min.[d]	- 40 °C to 125 °C Max.[d]	- 40 °C to 85 °C Min.[d]	- 40 °C to 85 °C Max.[d]	Unit
Power Supplies									
Power Supply Current	I_{CC}	V_{CC} = + 5 V, V_{EE} = - 5 V $V_{IN(A, B, C \text{ and ENABLE})}$ = 0 or 5 V	Room Full	0.05		1 10		1 10	µA
Negative Supply Current	I_{EE}		Room Full	- 0.05	- 1 - 10		- 1 - 10		
Ground Current	I_{GND}		Room Full	- 0.05	- 1 - 10		- 1 - 10		

SPECIFICATIONS (for Unipolar Supplies)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{CC} = + 5 V, V_{EE} = 0 V $V_{IN(A, B, C \text{ and ENABLE})}$ = 1.4 V, 0.3 V[a]	Temp.[b]	Typ.[c]	- 40 °C to 125 °C Min.[d]	- 40 °C to 125 °C Max.[d]	- 40 °C to 85 °C Min.[d]	- 40 °C to 85 °C Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	5	0	5	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 0 V, + 3.5 V	Room Full	145		482 565		482 513	Ω
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = + 3.5 V	Room Full	3.6		20 22		20 21	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = 0 V, + 3 V	Room Full	113		151 254		151 231	
Switch Off Leakage Current	$I_{S(off)}$	V_{CC} = + 5.5 V, V_{EE} = 0 V V_D = 1 V/4.5 V, V_S = 4.5 V/1 V	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	nA
	$I_{D(off)}$		Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Channel On Leakage Current	$I_{D(on)}$	V_{CC} = + 5.5 V, V_{EE} = 0 V V_D = V_S = 1 V/4.5 V	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Digital Control									
$V_{IN(A, B, C \text{ and ENABLE})}$ Low	V_{IL}		Full			0.3		0.3	V
$V_{IN(A, B, C \text{ and ENABLE})}$ High	V_{IH}		Full		1.4		1.4		
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C \text{ and ENABLE})}$ under test = 0.3 V	Full	0.01	- 1	1	- 1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C \text{ and ENABLE})}$ under test = 1.4 V	Full	0.01	- 1	1	- 1	1	
Dynamic Characteristics									
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see figure 1, 2, 3	Room Full	97		230 305		230 266	ns
Enable Turn-On Time	t_{ON}		Room Full	229		335 652		335 545	
Enable Turn-Off Time	t_{OFF}		Room Full	64		150 173		150 163	
Break-Before-Make Time Delay	t_D		Room Full	36	20		20		
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Full	0.44					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 15 pF f = 100 kHz	Room	< - 90					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	< - 90					

SPECIFICATIONS (for Unipolar Supplies)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{CC} = + 5 V, V_{EE} = 0 V $V_{IN(A, B, C and ENABLE)}$ = 1.4 V, 0.3 V[a]		Temp.[b]	Typ.[c]	- 40 °C to 125 °C Min.[d]	- 40 °C to 125 °C Max.[d]	- 40 °C to 85 °C Min.[d]	- 40 °C to 85 °C Max.[d]	Unit
Dynamic Characteristics										
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	DG9251	Room	2.9					pF
			DG9252	Room	2.2					
			DG9253	Room	2.1					
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz	DG9251	Room	12.4					
			DG9252	Room	6.8					
			DG9253	Room	4.6					
Channel On Capacitance[e]	$C_{D(on)}$	f = 1 MHz	DG9251	Room	16					
			DG9252	Room	10.6					
			DG9253	Room	8.8					
Power Supplies										
Power Supply Current	I_{CC}	$V_{IN(A, B, C and ENABLE)}$ = 0 V or 5 V		Room Full	0.05		1 10		1 10	µA
Negative Supply Current	I_{EE}			Room Full	- 0.05	- 1 - 10		- 1 - 10		
Ground Current	I_{GND}			Room Full	- 0.05	- 1 - 10		- 1 - 10		

SPECIFICATIONS (for Unipolar Supplies)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{CC} = + 16 V, V_{EE} = 0 V $V_{IN(A, B, C and ENABLE)}$ = 1.6 V, 0.5 V[a]	Temp.[b]	Typ.[c]	- 40 °C to 125 °C Min.[d]	- 40 °C to 125 °C Max.[d]	- 40 °C to 85 °C Min.[d]	- 40 °C to 85 °C Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	16	0	16	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 0.7 V, 8 V, 15.3 V	Room Full	69		152 171		152 158	Ω
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = + 0.7 V	Room Full	2		7 10		7 8	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = 0.7 V, + 15.3 V	Room Full	32		45 53		45 49	
Switch Off Leakage Current	$I_{S(off)}$	V_{CC} = + 16 V, V_{EE} = 0 V V_D = 1 V/15 V, V_S = 15 V/1 V	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	nA
	$I_{D(off)}$		Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Channel On Leakage Current	$I_{D(on)}$	V_{CC} = + 16 V, V_{EE} = 0 V V_D = V_S = 1 V/15 V	Room Full	± 0.02	- 1 - 50	1 50	- 1 - 5	1 5	
Digital Control									
$V_{IN(A, B, C and ENABLE)}$ Low	V_{IL}		Full			0.5		0.5	V
$V_{IN(A, B, C and ENABLE)}$ High	V_{IH}		Full		1.6		1.6		
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C and ENABLE)}$ under test = 0.5 V	Full	0.01	- 1	1	- 1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C and ENABLE)}$ under test = 1.6 V	Full	0.01	- 1	1	- 1	1	
Dynamic Characteristics									
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see figure 1, 2, 3	Room Full	56		130 160		130 150	ns
Enable Turn-On Time	t_{ON}		Room Full	98		175 256		175 221	
Enable Turn-Off Time	t_{OFF}		Room Full	37		120 134		120 127	
Break-Before-Make Time Delay	t_D		Room Full	31	12		12		

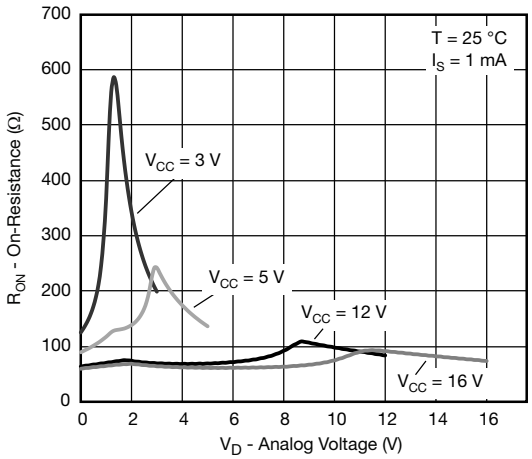
SPECIFICATIONS (for Unipolar Supplies)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{CC} = + 16 V, V_{EE} = 0 V $V_{IN(A, B, C \text{ and ENABLE})}$ = 1.6 V, 0.5 V[a]		Temp.[b]	Typ.[c]	- 40 °C to 125 °C Min.[d]	- 40 °C to 125 °C Max.[d]	- 40 °C to 85 °C Min.[d]	- 40 °C to 85 °C Max.[d]	Unit
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF		Room	4.5					pC
Dynamic Characteristics										
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 15 pF f = 100 kHz		Room	< - 90					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}			Room	< - 90					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	DG9251	Room	2.6					pF
			DG9252	Room	2.1					
			DG9253	Room	1.8					
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz	DG9251	Room	10.4					
			DG9252	Room	5.8					
			DG9253	Room	4.2					
Channel On Capacitance[e]	$C_{D(on)}$	f = 1 MHz	DG9251	Room	15					
			DG9252	Room	9.5					
			DG9253	Room	8.2					
Power Supplies										
Power Supply Current	I_{CC}	$V_{IN(A, B, C \text{ and ENABLE})}$ = 0 V or 16 V		Room Full	0.05		1 10		1 10	µA
Negative Supply Current	I_{EE}			Room Full	- 0.05	- 1 - 10		- 1 - 10		
Ground Current	I_{GND}			Room Full	- 0.05	- 1 - 10		- 1 - 10		

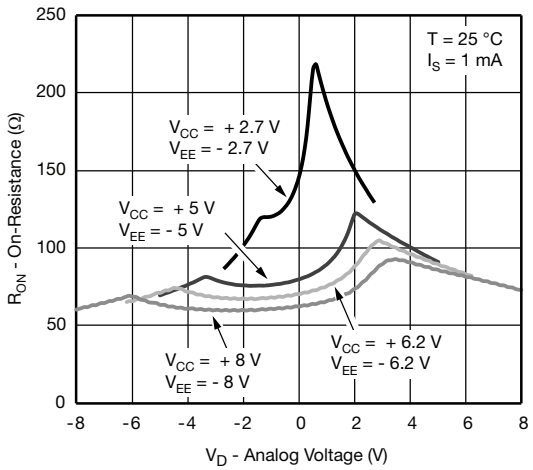
Notes:
a. V_{IN} = input voltage to perform proper function.
b. Room - 25 °C, full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

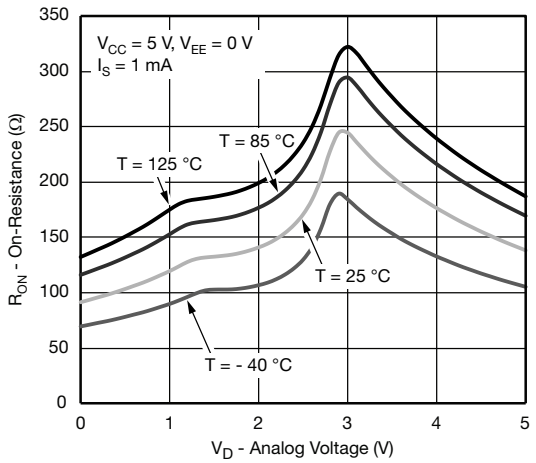


R_{ON} vs. V_D and Single Supply Voltage

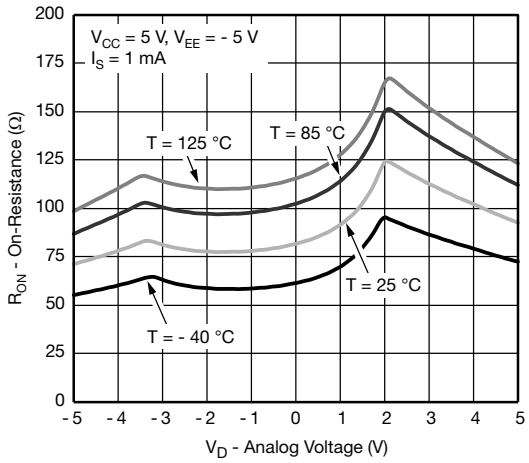


R_{ON} vs. V_D and Dual Supply Voltage

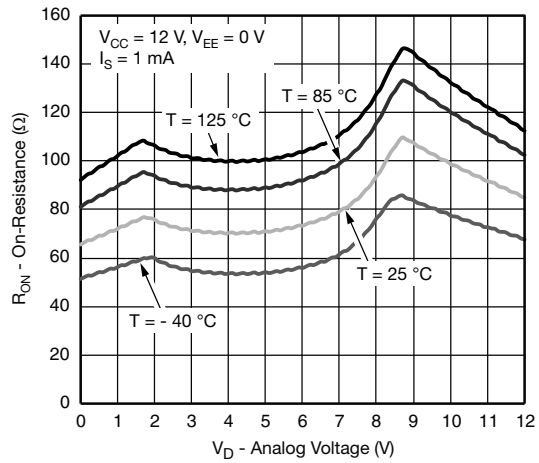
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



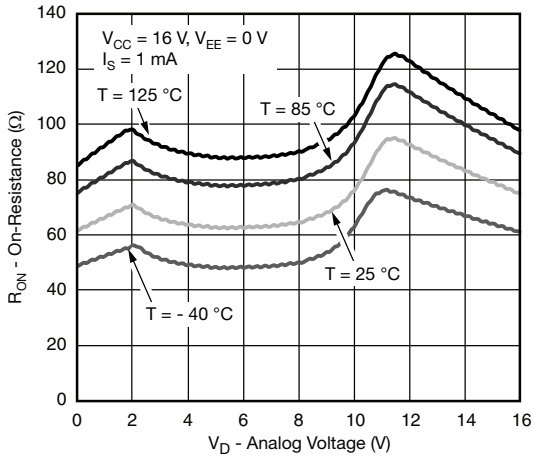
R_{ON} vs. Analog Voltage and Temperature



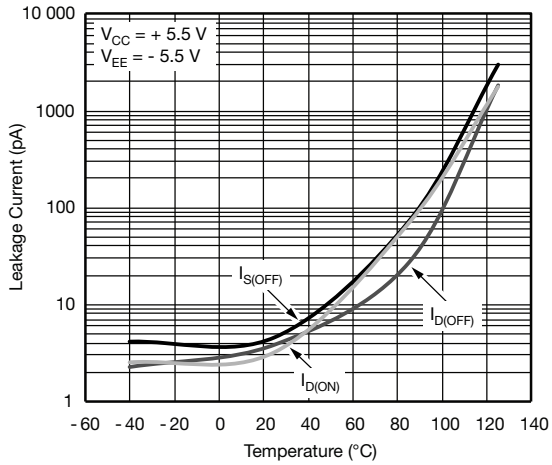
R_{ON} vs. Analog Voltage and Temperature



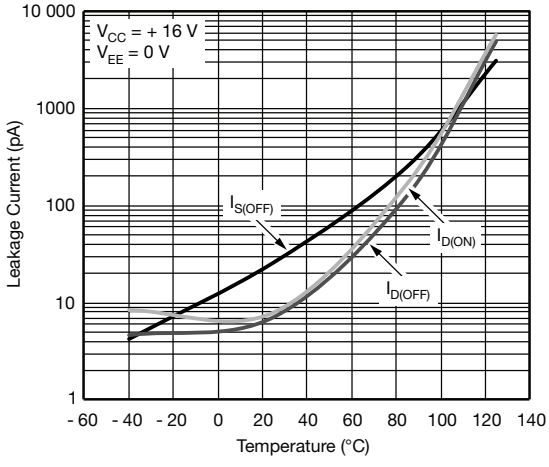
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature

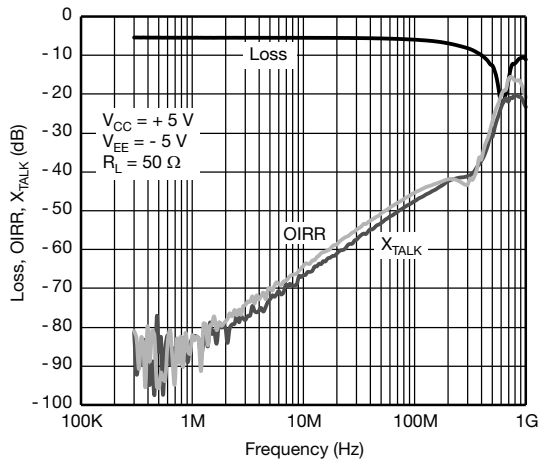


Leakage Current vs. Temperature

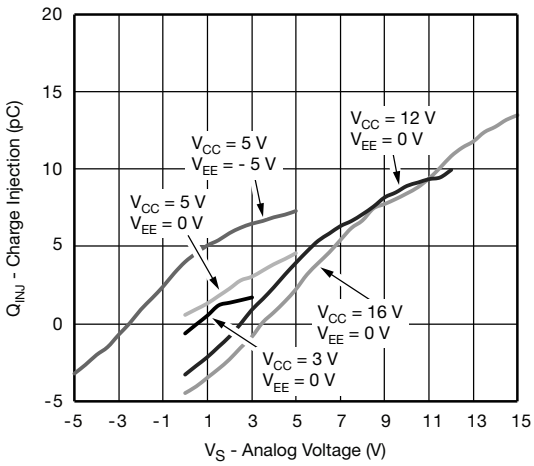


Leakage Current vs. Temperature

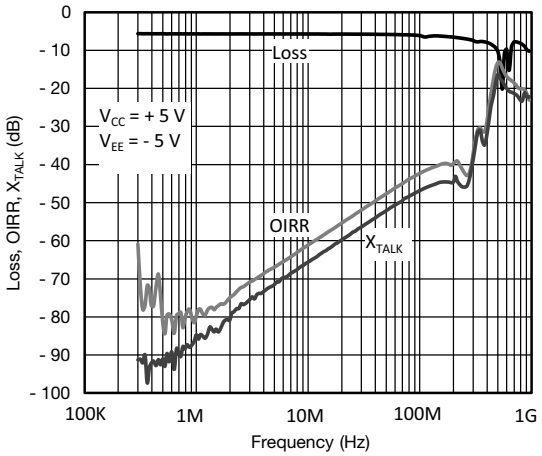
TYPICAL CHARACTERISTICS



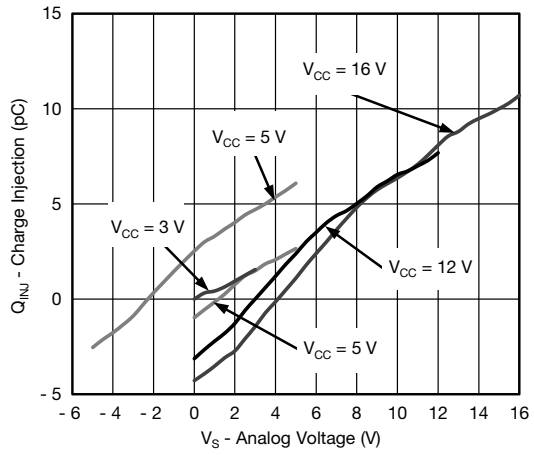
DG9251 Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



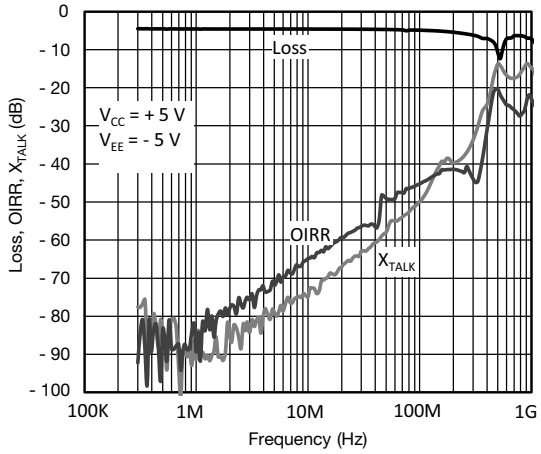
DG9251 Charge Injection vs. Analog Voltage



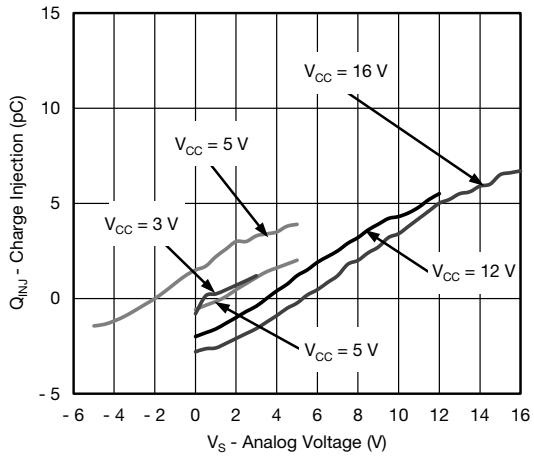
DG9252 Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



DG9252 Charge Injection vs. Analog Voltage

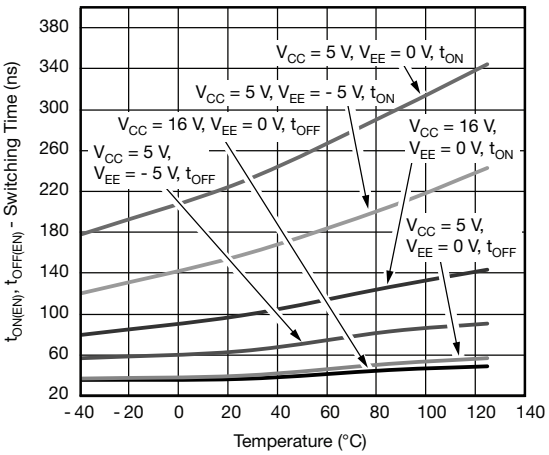


DG9253 Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

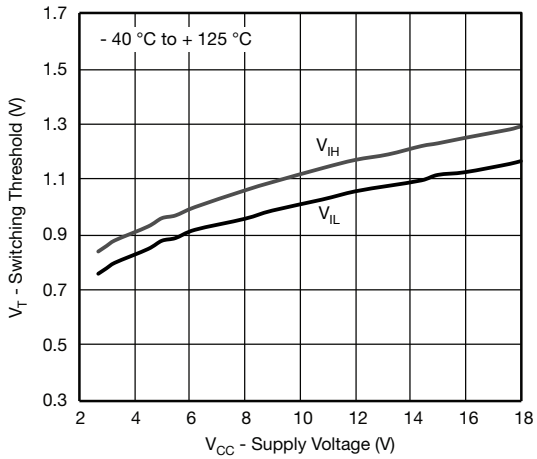


DG9253 Charge Injection vs. Analog Voltage

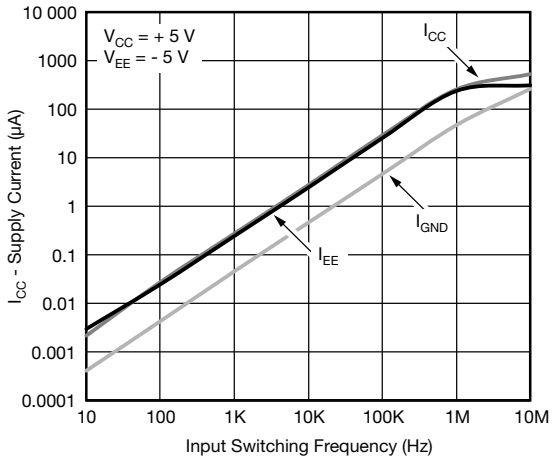
TYPICAL CHARACTERISTICS



Switching Time vs. Temperature



Switching Threshold vs. Supply Voltage



Supply Current vs. Input Switching Frequency

TEST CIRCUITS

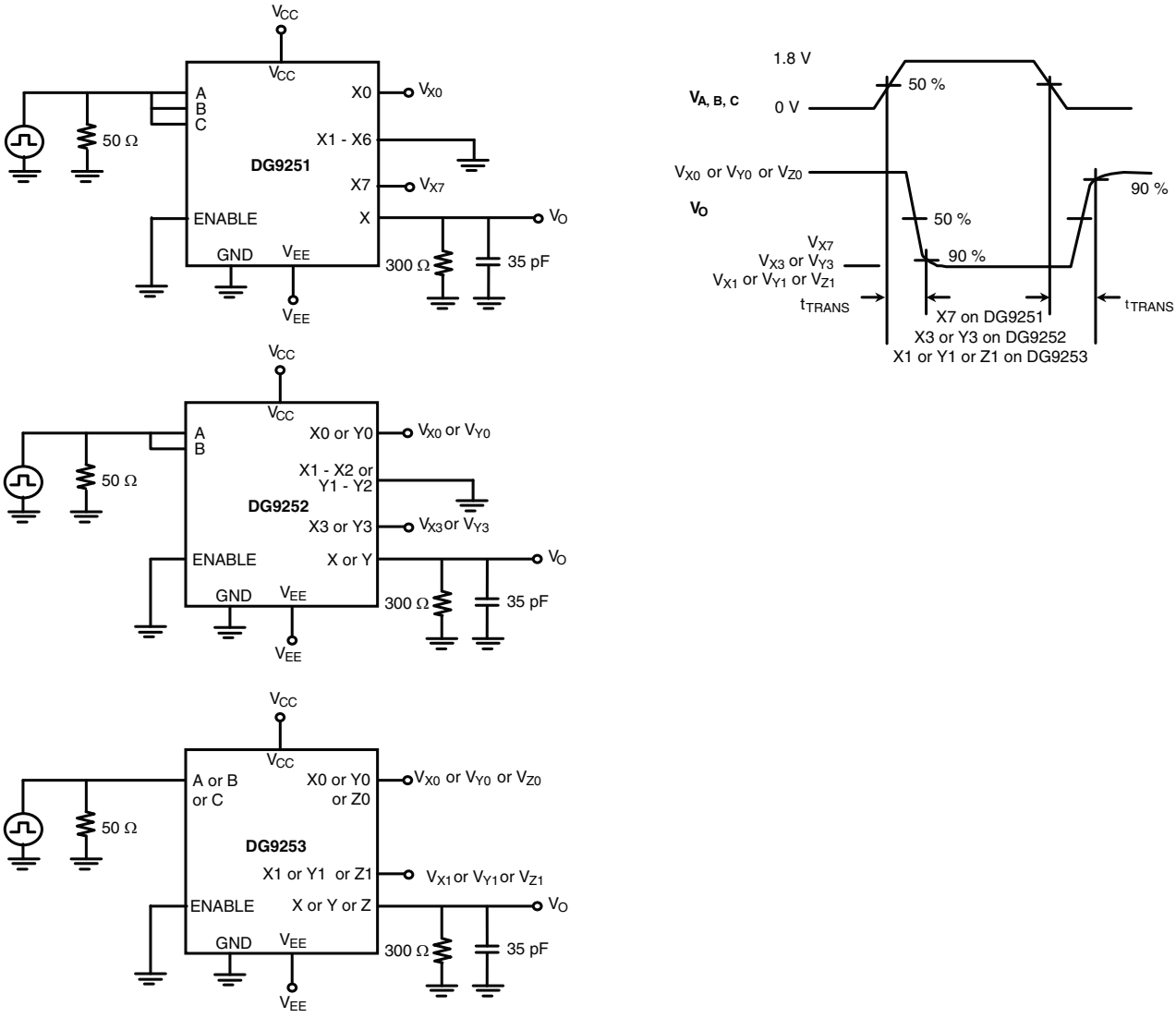
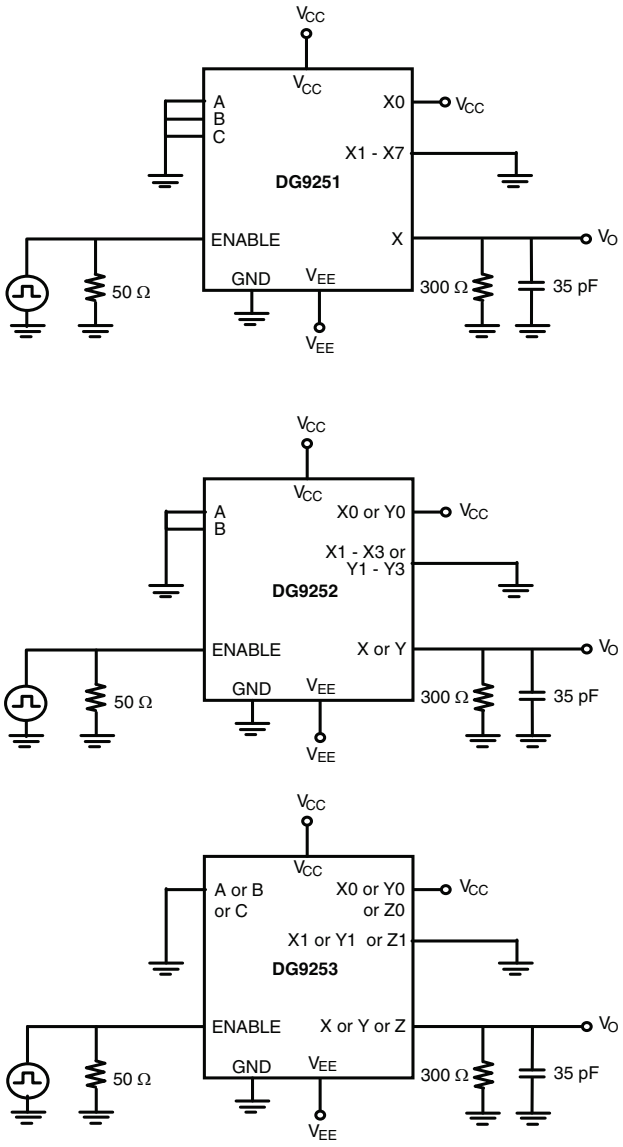


Figure 1. Transition Time

TEST CIRCUITS



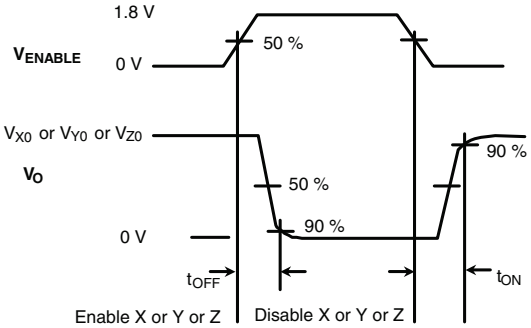


Figure 2. Enable Switching Time

TEST CIRCUITS

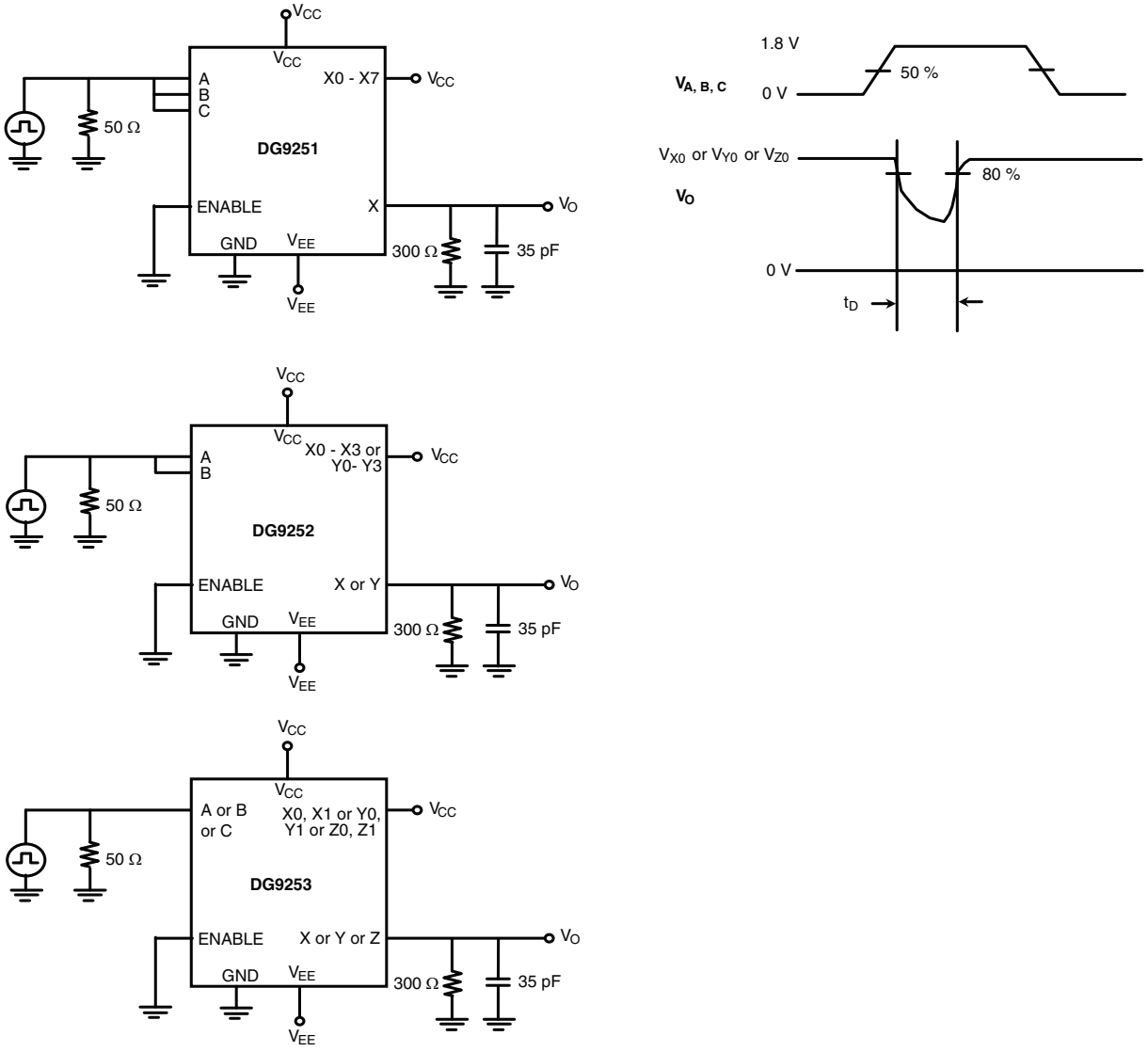
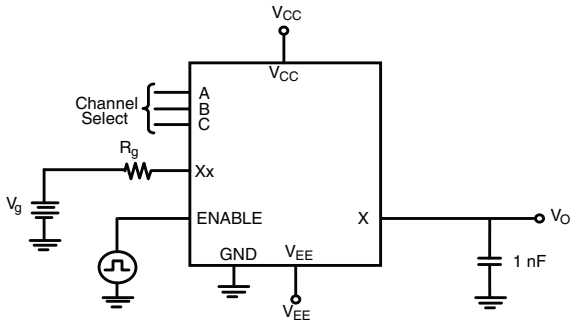


Figure 3. Break-Before-Make

TEST CIRCUITS



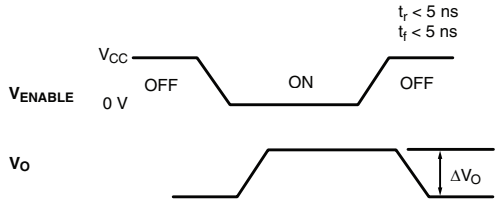


Figure 4. Charge Injection

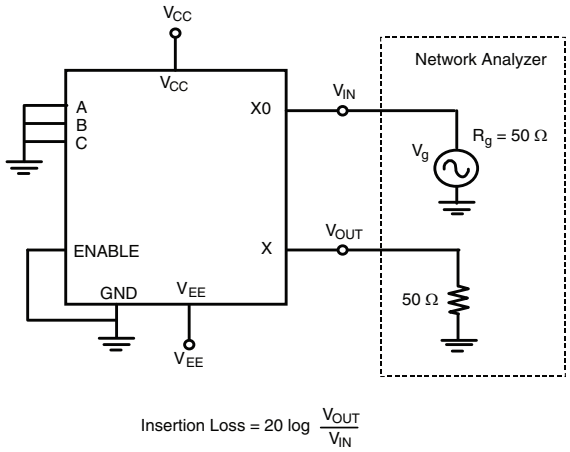


Figure 5. Insertion Loss

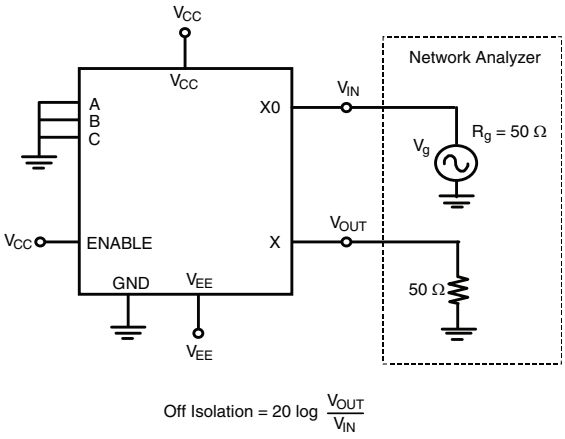


Figure 6. Off Isolation

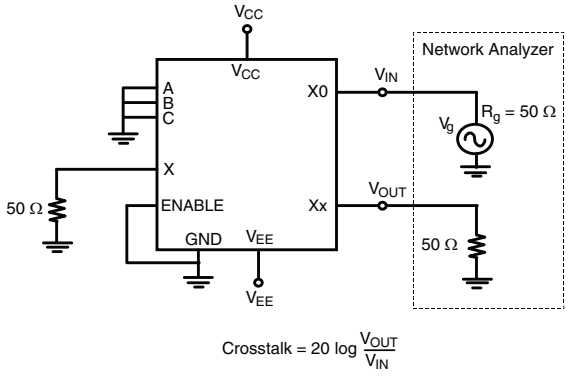


Figure 7. Crosstalk

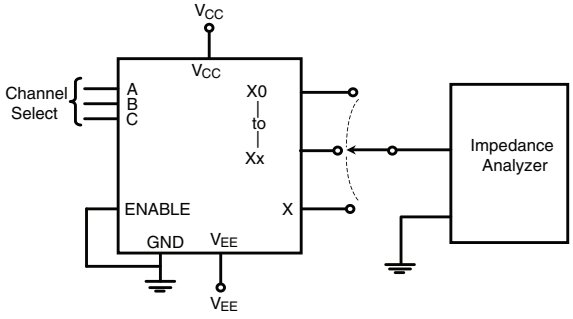
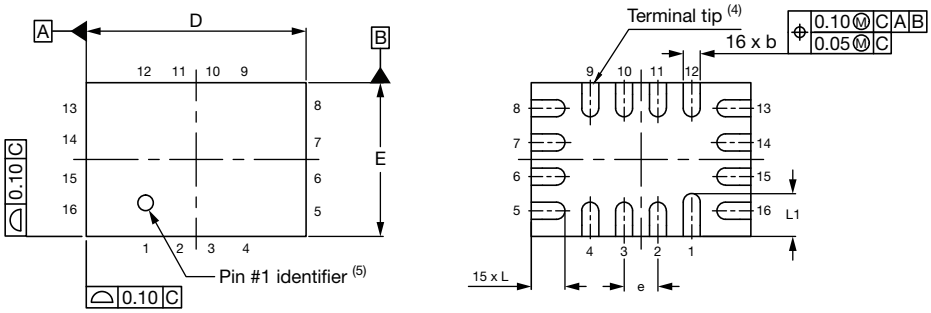


Figure 8. Source, Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67075.

Thin miniQFN16 Case Outline



Top view

Bottom view

Side view

DIMENSIONS	MILLIMETERS (1)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N (3)	16			16		
Nd (3)	4			4		
Ne (3)	4			4		

Notes

(1) Use millimeters as the primary measurement.

(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.

(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.

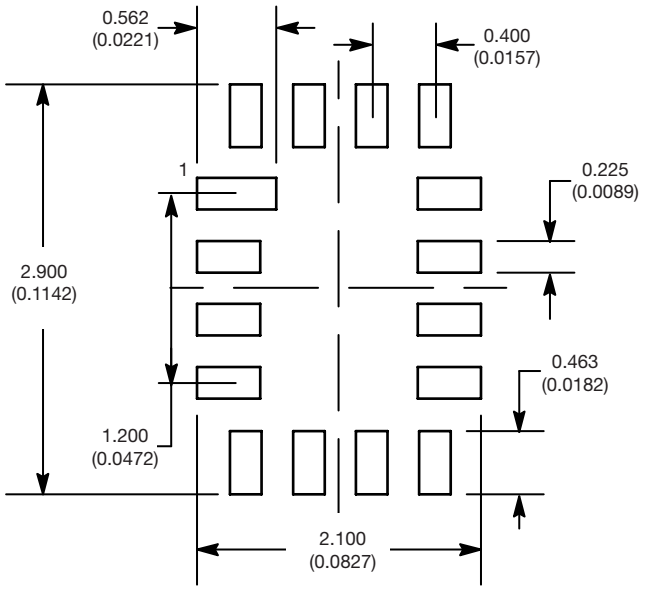
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.

(6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

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