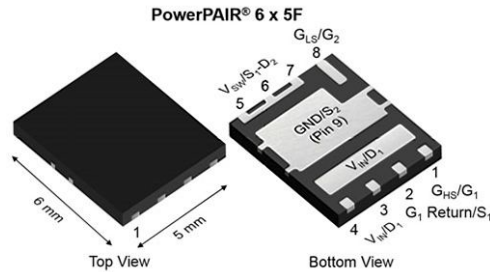


Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode



FEATURES

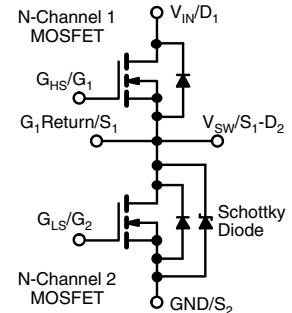
- TrenchFET® Gen IV power MOSFET
- SkyFET® low-side MOSFET with integrated Schottky
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V _{DS} (V)	30	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.00307	0.00105
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.00530	0.00145
Q _g typ. (nC)	9	38.6
I _D (A) ^a	76	197
Configuration	Dual	

ORDERING INFORMATION

Package	PowerPAIR 6 x 5F
Lead (Pb)-free and halogen-free	SiZF920DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage	V _{DS}	30	30	V	
Gate-source voltage	V _{GS}	+20, -16	+16, -12	V	
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	76	197	A
		T _C = 70 °C	61	158	
		T _A = 25 °C	28 ^{b, c}	49 ^{b, c}	
		T _A = 70 °C	23 ^{b, c}	39 ^{b, c}	
Pulsed drain current (t = 100 μs)	I _{DM}	130	130	A	
Continuous source-drain diode current	I _S	T _C = 25 °C	26	122	A
		T _A = 25 °C	3.6 ^{b, c}	7.4 ^{b, c}	
Single pulse avalanche current	I _{AS}	16	28	mJ	
Single pulse avalanche energy	E _{AS}	13	39		
Maximum power dissipation	P _D	T _C = 25 °C	28	74	W
		T _C = 70 °C	18	47	
		T _A = 25 °C	3.9 ^{b, c}	4.5 ^{b, c}	
		T _A = 70 °C	2.5 ^{b, c}	2.9 ^{b, c}	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) ^{d, e}		260		°C	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	CHANNEL-1		CHANNEL-2		UNIT	
		TYP.	MAX.	TYP.	MAX.		
Maximum junction-to-ambient ^{b, f}	t ≤ 10 s	R _{thJA}	25	32	22	28	°C/W
Maximum junction-to-case (source)	Steady state	R _{thJC}	3.5	4.4	1.3	1.7	°C/W

Notes

- T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 65 °C/W for channel-1 and 65 °C/W for channel-2



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT			
Static									
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	30	-	-	V		
			Ch-2	30	-	-			
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.1	-	2.4			
			Ch-2	1.1	-	2.2			
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}, -16\text{ V}$	Ch-1	-	-	± 100	nA		
		$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V}, -12\text{ V}$	Ch-2	-	-	± 100			
Zero Gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	-	1	μA		
			Ch-2	-	60	400			
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1	-	-	5			
			Ch-2	-	350	4000			
On-state drain current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20	-	-	A		
			Ch-2	20	-	-			
Drain-source on-state resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-1	-	0.00230	0.00307	Ω		
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-2	-	0.00070	0.00105			
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-1	-	0.00380	0.00530			
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-2	-	0.00095	0.00145			
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$	Ch-1	-	65	-	S		
		$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$	Ch-2	-	135	-			
Dynamic ^a									
Input capacitance	C_{iss}	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	1300	-	pF		
			Ch-2	-	5230	-			
Output capacitance	C_{oss}		Ch-1	-	700	-			
			Ch-2	-	2920	-			
Reverse transfer capacitance	C_{rss}		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	35		-	
				Ch-2	-	360		-	
C_{rss}/C_{iss} ratio				Ch-1	-	0.027		0.054	
				Ch-2	-	0.069		0.140	
Total gate charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		Ch-1	-	19	29	nC	
		$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		Ch-2	-	83	125		
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		Ch-1	-	9	14		
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		Ch-2	-	38.6	58		
Gate-source charge	Q_{gs}	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	-	4.4	-			
			Ch-2	-	17	-			
Gate-drain charge	Q_{gd}		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	-	2	-		
				Ch-2	-	9.2	-		
Output charge	Q_{oss}			$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	17	-	
					Ch-2	-	46	-	
Gate resistance	R_g			$f = 1\text{ MHz}$	Ch-1	0.2	1	2	Ω
					Ch-2	0.1	0.4	0.8	



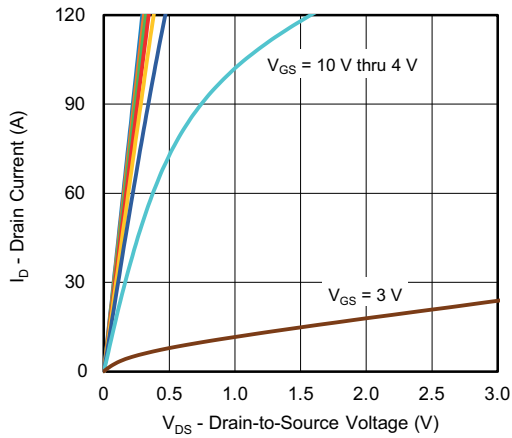
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Dynamic ^a							
Turn-on delay time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	18	35	ns
Rise time	t _r		Ch-2	-	34	70	
Turn-off delay time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	95	190	
			Ch-2	-	116	230	
Fall time	t _f		Ch-1	-	17	35	
			Ch-2	-	45	90	
Turn-on delay time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	10	20	
			Ch-2	-	27	50	
Rise time	t _r		Ch-1	-	11	20	
			Ch-2	-	17	35	
Turn-off delay time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	5	10	
			Ch-2	-	70	150	
Fall time	t _f		Ch-1	-	20	40	
			Ch-2	-	43	85	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	Ch-1	-	-	26	A
			Ch-2	-	-	122	
Pulse diode forward current ^a	I _{SM}		Ch-1	-	-	130	
			Ch-2	-	-	130	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	Ch-1	-	0.77	1.1	V
		I _S = 3 A, V _{GS} = 0 V	Ch-2	-	0.36	0.60	
Body diode reverse recovery time	t _{rr}	Channel-1 I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	27	50	ns
			Ch-2	-	55	110	
Body diode reverse recovery charge	Q _{rr}		Ch-1	-	15	30	nC
			Ch-2	-	66	130	
Reverse recovery fall time	t _a	Channel-2 I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	16	-	ns
			Ch-2	-	30	-	
Reverse recovery rise time	t _b		Ch-1	-	11	-	
			Ch-2	-	25	-	

Notes

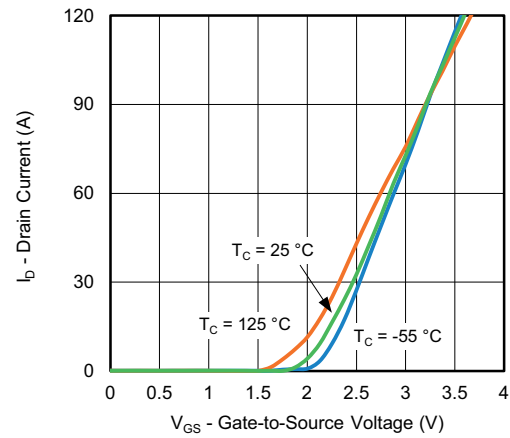
- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

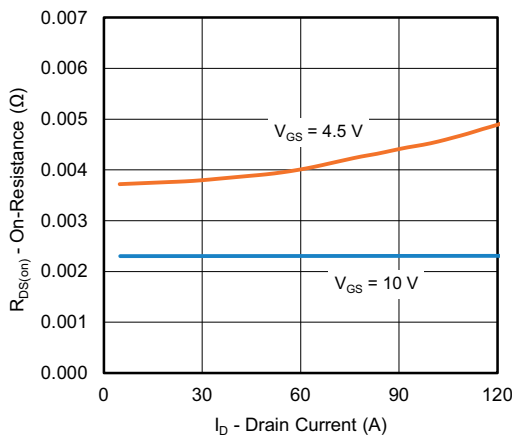
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



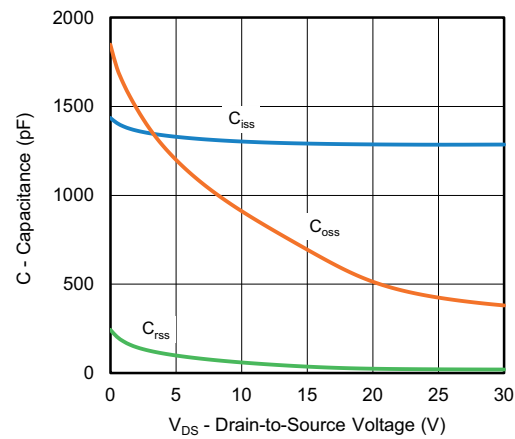
Output Characteristics



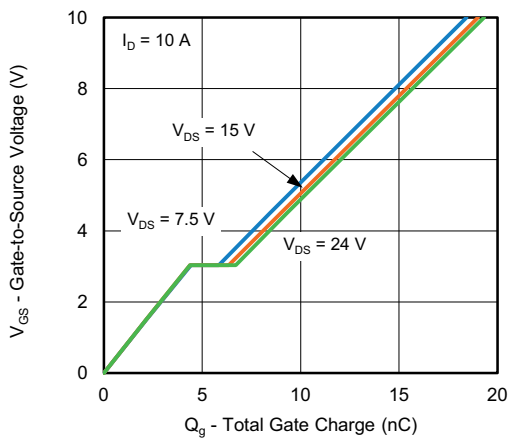
Transfer Characteristics



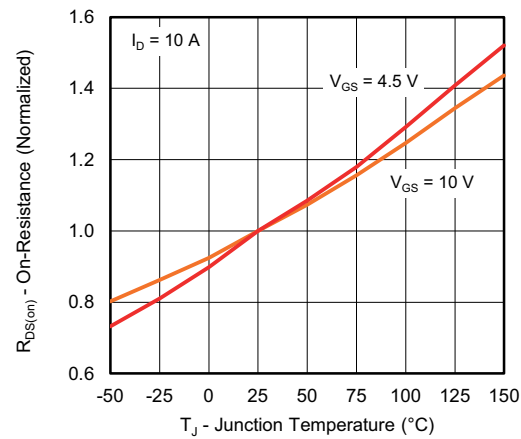
On-Resistance vs. Drain Current



Capacitance



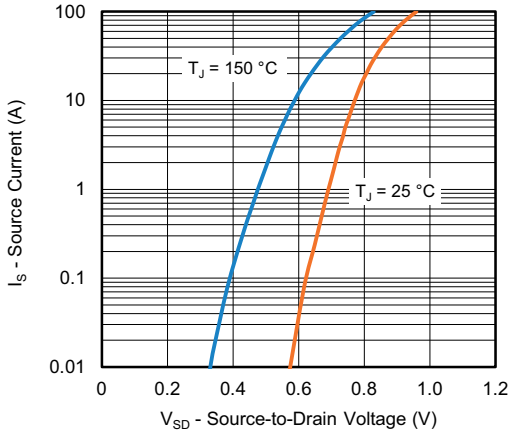
Gate Charge



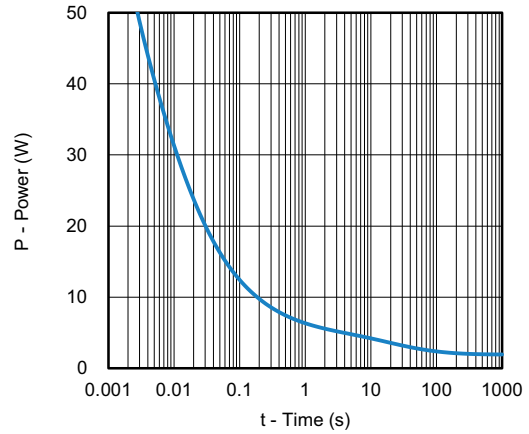
On-Resistance vs. Junction Temperature



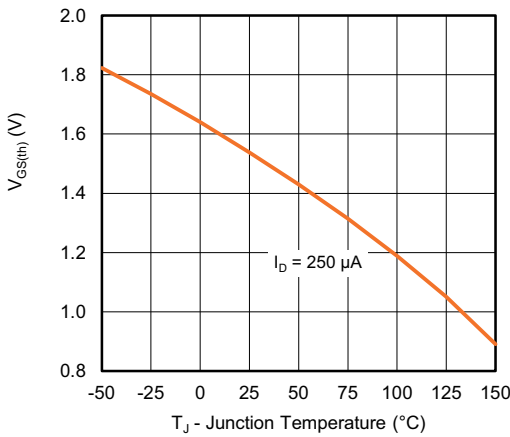
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



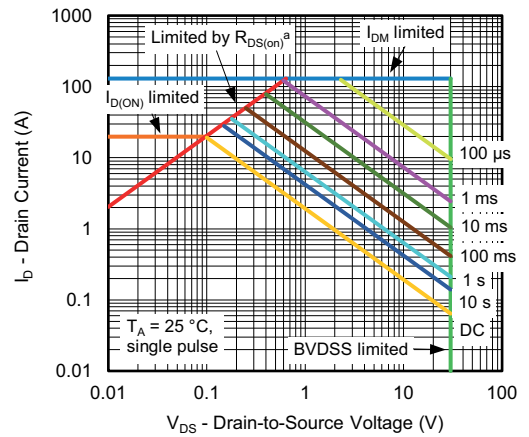
Source-Drain Diode Forward Voltage



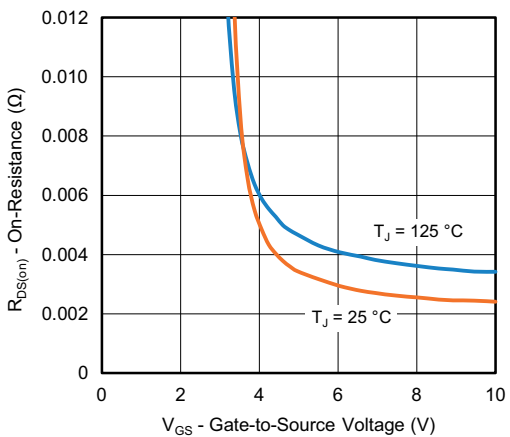
Single Pulse Power, Junction-to-Ambient



Threshold Voltage



Safe Operating Area, Junction-to-Ambient



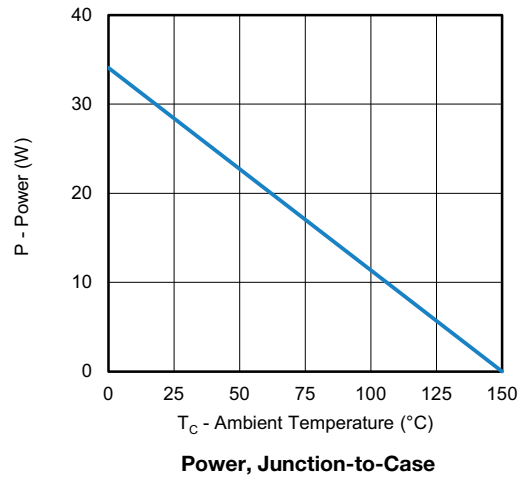
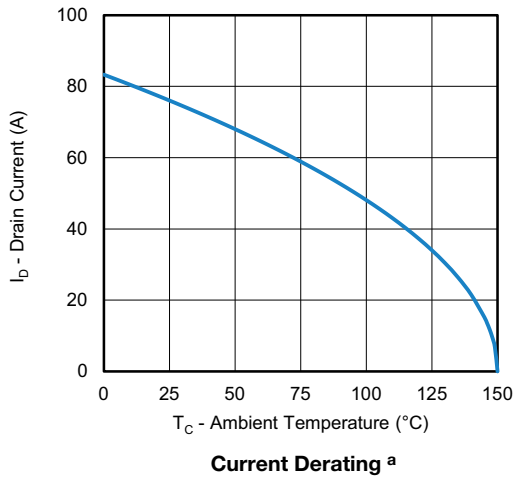
On-Resistance vs. Gate-to-Source Voltage

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

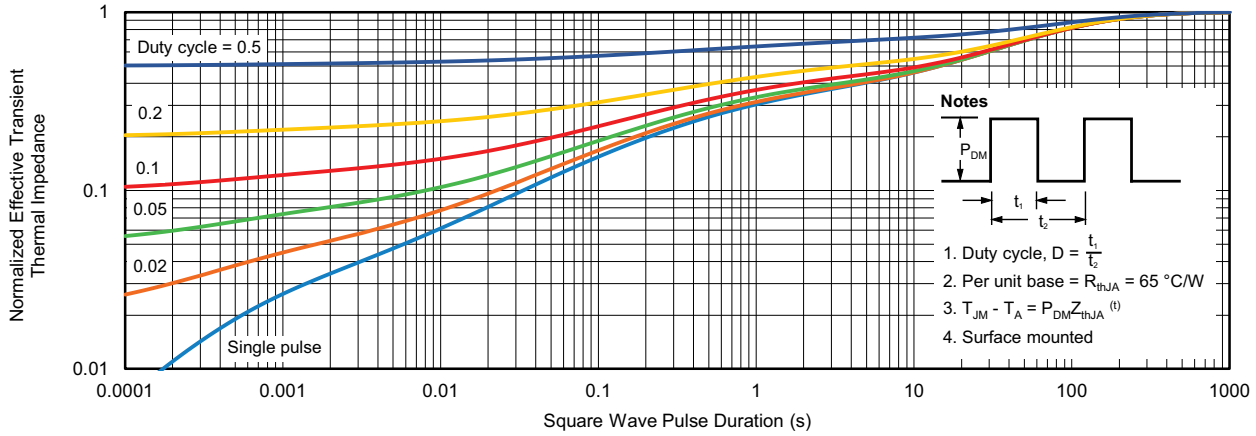


Note

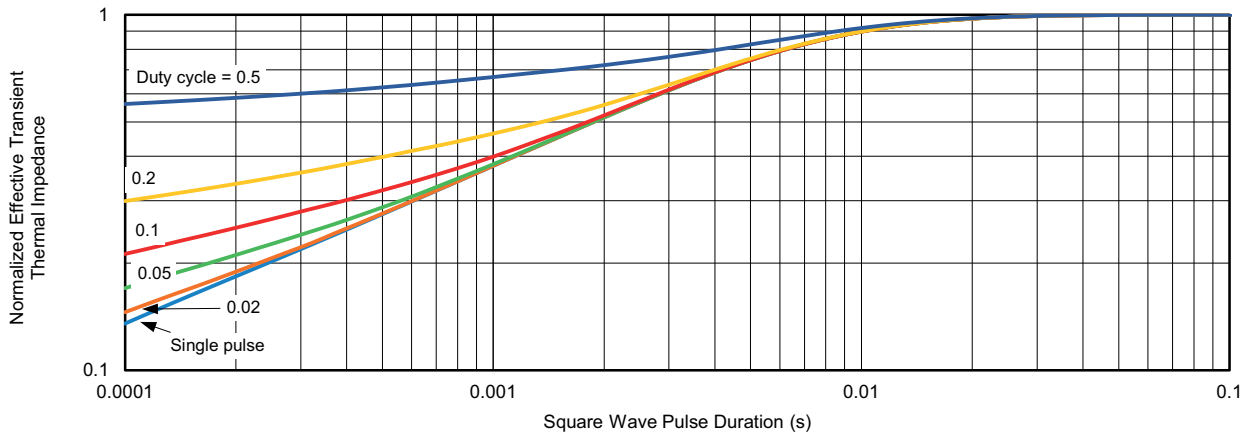
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

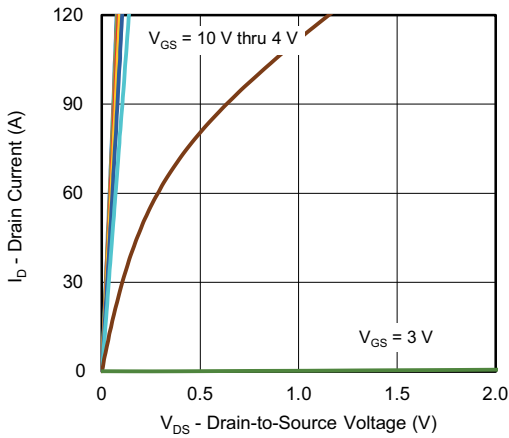


Normalized Thermal Transient Impedance, Junction-to-Ambient

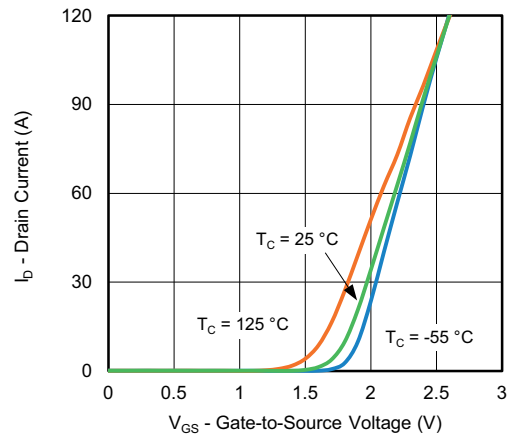


Normalized Thermal Transient Impedance, Junction-to-Case

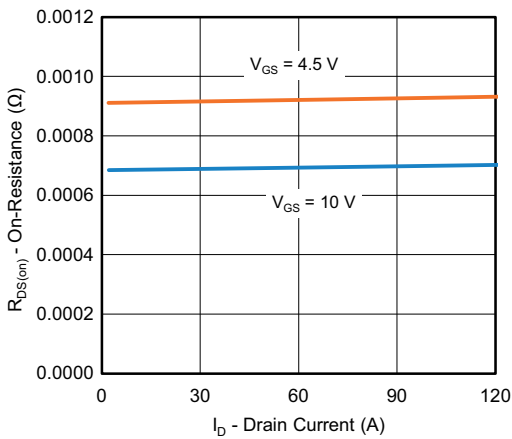
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



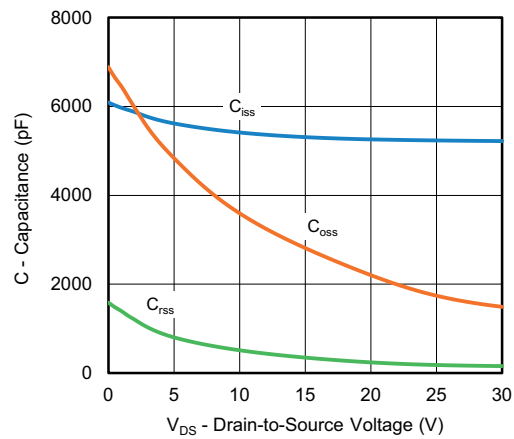
Output Characteristics



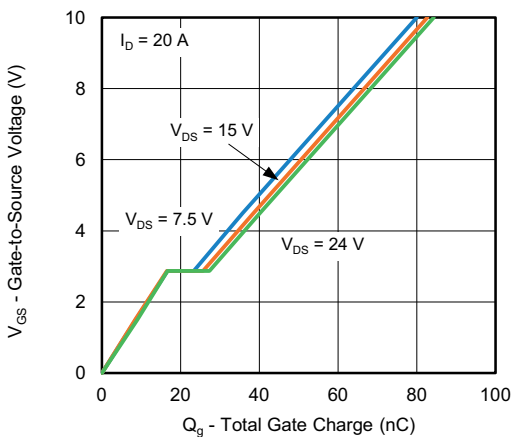
Transfer Characteristics



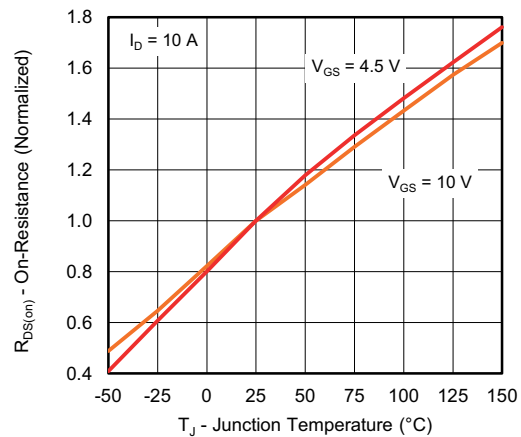
On-Resistance vs. Drain Current



Capacitance



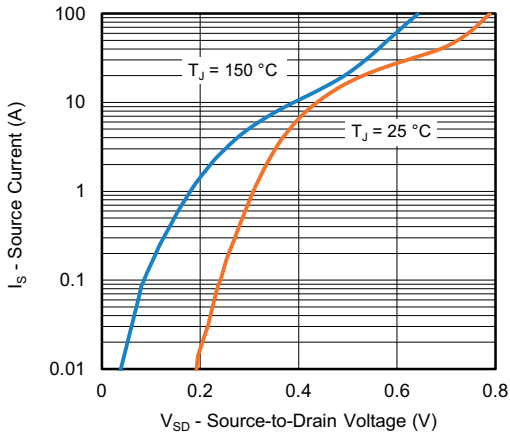
Gate Charge



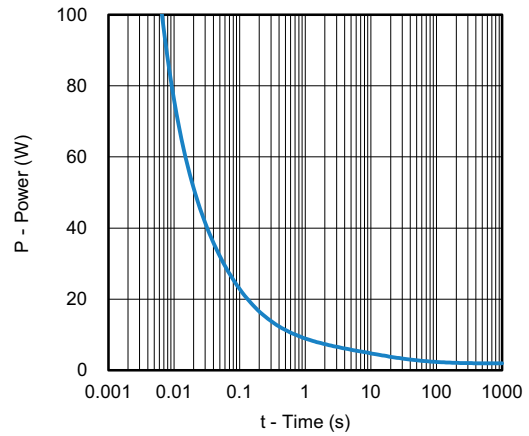
On-Resistance vs. Junction Temperature



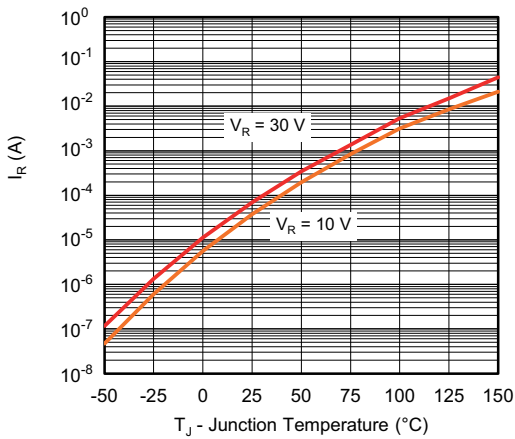
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



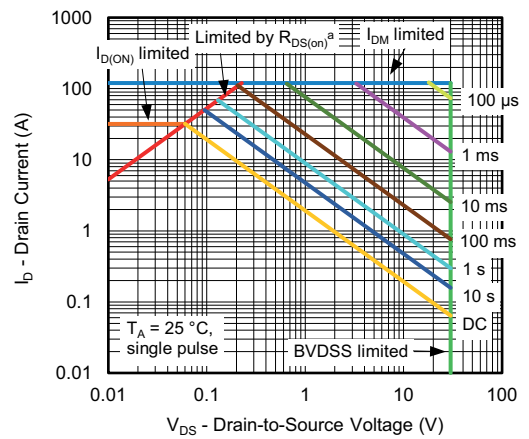
Source-Drain Diode Forward Voltage



Single Pulse Power, Junction-to-Ambient



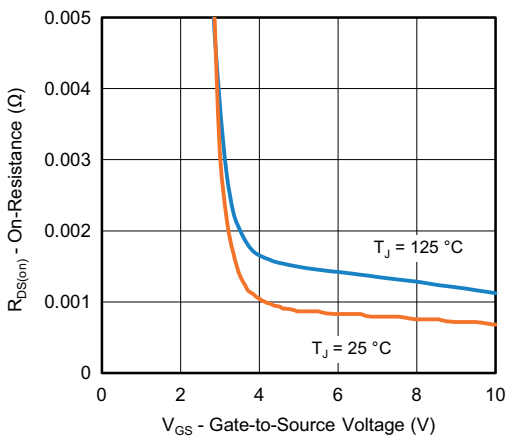
Reverse Current (Schottky)



Safe Operating Area, Junction-to-Ambient

Note

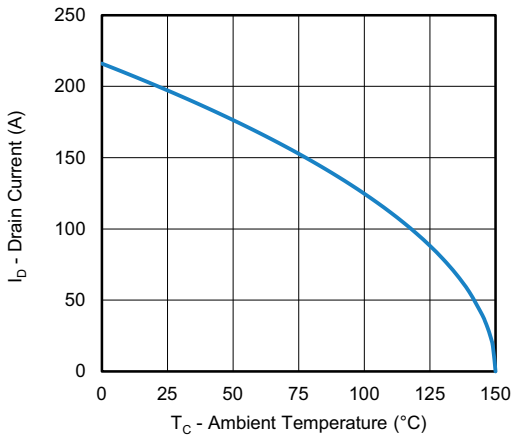
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



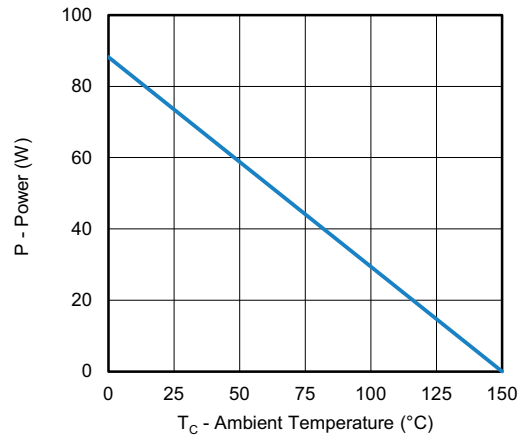
On-Resistance vs. Gate-to-Source Voltage



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



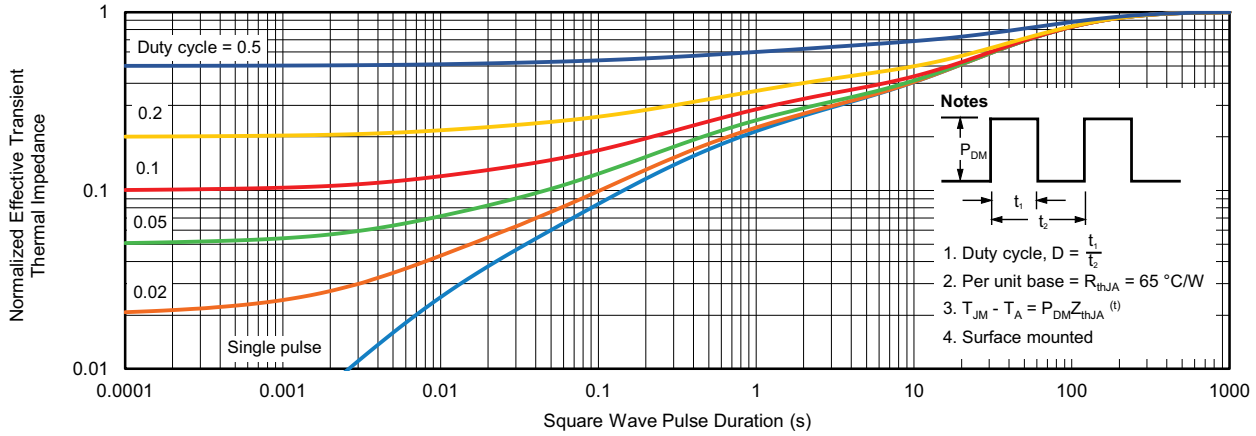
Power, Junction-to-Case

Note

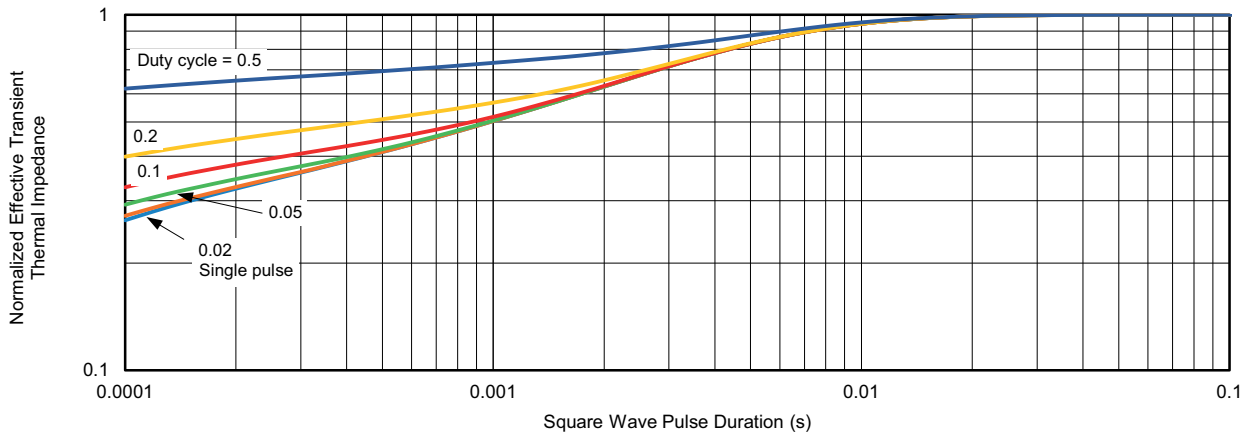
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?79595.

PowerPAIR® 6 x 5 F Case Outline



DIMENSION	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.10	0.000	-	0.004
b	0.35	0.41	0.46	0.014	0.016	0.018
b1	0.38 ref.			0.015 ref.		
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.26	3.31	3.36	0.128	0.130	0.132
D2	4.20	4.30	4.40	0.165	0.169	0.173
D3	4.15	4.20	4.25	0.163	0.165	0.167
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	2.50	2.55	2.60	0.098	0.100	0.102
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.050 BSC		
e1	3.81 BSC			0.150 BSC		
K	0.52	0.57	0.62	0.020	0.022	0.024
K1	0.69	0.74	0.79	0.027	0.029	0.031
K2	0.60	0.65	0.70	0.024	0.026	0.028
K3	0.39 BSC			0.015 BSC		
K4	0.50	0.55	0.60	0.020	0.022	0.024
K5	0.25	0.30	0.35	0.010	0.012	0.014
K6	0.40	0.45	0.50	0.016	0.018	0.020
K7	0.35	0.40	0.45	0.014	0.016	0.018
K8	0.30	0.35	0.40	0.012	0.014	0.016
L	0.33	0.43	0.53	0.013	0.017	0.021
L1	1.31	1.36	1.41	0.052	0.054	0.056
L2	0.20 ref.			0.008 ref.		
ECN: T20-0097-Rev. C, 25-Feb-2020						
DWG: 6043						

Note

- Millimeters will govern

Recommended Minimum PAD for PowerPAIR® 6 x 5



Dimensions in millimeters (inch)

Note

- Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



Disclaimer

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