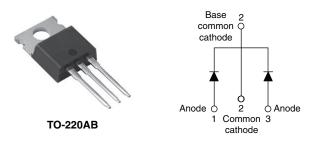


**Vishay Semiconductors** 

# Schottky Rectifier, 2 x 8 A



PRODUCT SUMMARY					
Package	TO-220AB				
I <sub>F(AV)</sub>	2 x 8 A				
V <sub>R</sub>	60 V, 80 V, 100 V				
V <sub>F</sub> at I <sub>F</sub>	0.58 V				
I <sub>RM</sub> max.	7 mA at 125 °C				
T <sub>J</sub> max.	175 °C				
Diode variation	Common cathode				
E <sub>AS</sub>	7.5 mJ				

### **FEATURES**

- 175 °C T<sub>J</sub> operation
- Low forward voltage drop
- · High frequency operation



• High purity, high temperature epoxy encapsulation for enhanced mechanical strength RoHS and moisture resistance



- Guard ring for enhanced ruggedness and long FREE term reliability
- Compliant to RoHS Directive 2002/95/EC
- Designed and qualified according to JEDEC-JESD47
- Halogen-free according to IEC 61249-2-21 definition (-N3 only)

### DESCRIPTION

This center tap Schottky rectifier series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in switching power supplies, converters, freewheeling diodes, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS						
SYMBOL	CHARACTERISTICS	VALUES	UNITS			
I <sub>F(AV)</sub>	Rectangular waveform	16	A			
V <sub>RRM</sub>		60 to 100	V			
I <sub>FSM</sub>	t <sub>p</sub> = 5 μs sine	850	A			
V <sub>F</sub>	8 A <sub>pk</sub> , T <sub>J</sub> = 125 °C (per leg)	0.58	V			
TJ	Range	- 55 to 175	°C			

VOLTAGE RATINGS									
PARAMETER	SYMBOL	VS- 16CTQ060PbF	VS- 16CTQ060-N3	VS- 16CTQ080PbF	VS- 16CTQ080-N3	VS- 16CTQ100PbF	VS- 16CTQ100-N3	UNITS	
Maximum DC reverse voltage	V <sub>R</sub>								
Maximum working peak reverse voltage	V <sub>RWM</sub>	60	60	80	80	100	100	V	

ABSOLUTE MAXIMUM RATINGS							
PARAMETER		SYMBOL	TEST COND	DITIONS	VALUES	UNITS	
Maximum average forward current	per leg		50 % duty cycle at $T_{C}$ = 148 °C, rectangular waveform		8	•	
See fig. 5	per device	IF(AV)			16	A	
Maximum peak one cycle non-repetitive surge current per leg See fig. 7			5 $\mu s$ sine or 3 $\mu s$ rect. pulse	Following any rated load condition and with rated	850	А	
		IFSM	10 ms sine or 6 ms rect. pulse	V <sub>RRM</sub> applied	275	A	
Non-repetitive avalanche energy per leg		E <sub>AS</sub>	$T_J = 25 \text{ °C}, I_{AS} = 0.50 \text{ A}, L = 60$	) mH	7.50	mJ	

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VS-16CTQ...PbF Series, VS-16CTQ...-N3 Series

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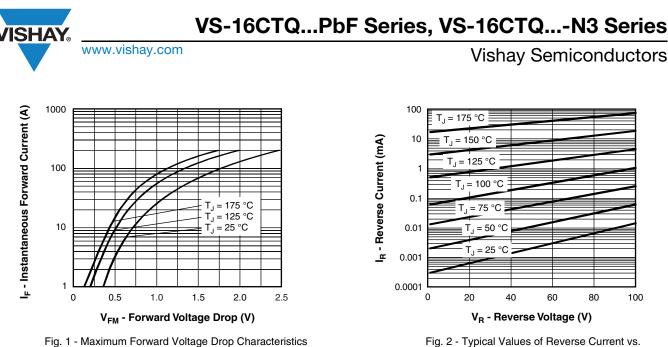
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<b>ABSOLUTE MAXIMUM RATIN</b>	GS				
Repetitive avalanche current per leg		Current decaying linearly to zero in 1 $\mu$ s Frequency limited by T <sub>J</sub> maximum V <sub>A</sub> = 1.5 x V <sub>R</sub> typic		al 0.50	А
ELECTRICAL SPECIFICATIO	ONS				
PARAMETER	SYMBOL	TEST CO	NDITIONS	VALUES	UNITS
		8 A	т ос «о	0.72	
Maximum forward voltage drop per leg See fig. 1	V <sub>FM</sub> <sup>(1)</sup>	16 A	T <sub>J</sub> = 25 °C	0.88	v
		8 A	T 405.00	0.58	
		16 A	T <sub>J</sub> = 125 °C	0.69	
Maximum reverse leakage current per leg	I <sub>RM</sub> <sup>(1)</sup>	T <sub>J</sub> = 25 °C	\/	0.55	mA
See fig. 2		T <sub>J</sub> = 125 °C	$V_R = rated V_R$	7.0	
Threshold voltage	V <sub>F(TO)</sub>	T T maximum		0.415	V
Forward slope resistance	r <sub>t</sub>	$T_J = T_J maximum$		11.07	mΩ
Maximum junction capacitance per leg	CT	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz) 25 °C		500	pF
Typical series inductance per leg	L <sub>S</sub>	Measured lead to lead 5 mm from package body		8.0	nH
Maximum voltage rate of change	dV/dt	Rated V <sub>R</sub>		10 000	V/µs

#### Note

 $^{(1)}\,$  Pulse width < 300  $\mu s,$  duty cycle < 2 %

THERMAL - MECHANIC	AL SPECIFICA	TIONS			
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction and storage temperature range	T <sub>J</sub> , T <sub>Stg</sub>		- 55 to 175	°C	
Maximum thermal resistance, junction to case per leg	R <sub>thJC</sub>			°C ///	
Maximum thermal resistance junction to case per package	R <sub>thJC</sub>	DC operation	1.63	°C/W	
Typical thermal resistance, case to heatsink	R <sub>thCS</sub>	Mounting surface, smooth and greased	0.50		
Approvimate weight			2	g	
Approximate weight			0.07	oz.	
	nimum		6 (5)	kgf ⋅ cm	
Mounting torque ma	ximum		12 (10)	(lb̃f · in)	
			16CT	Q060	
Marking device		Case style TO-220AB	16CT	Q080	
			16CT	Q100	



(Per Leg)

Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

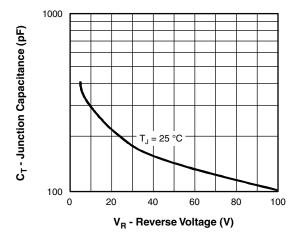


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

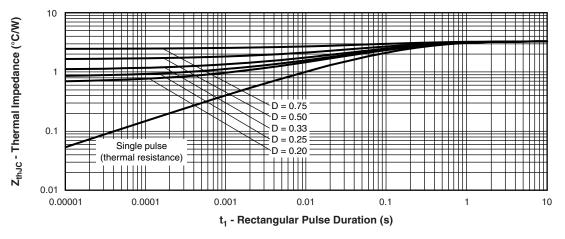


Fig. 4 - Maximum Thermal Impedance Z<sub>thJC</sub> Characteristics (Per Leg)

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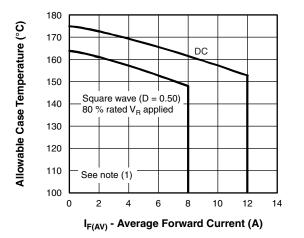
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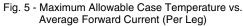
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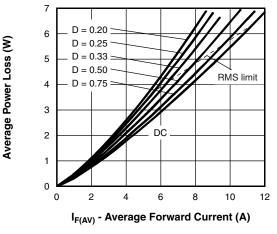


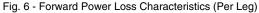
## VS-16CTQ...PbF Series, VS-16CTQ...-N3 Series

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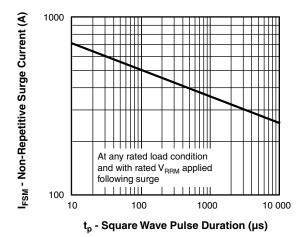


Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

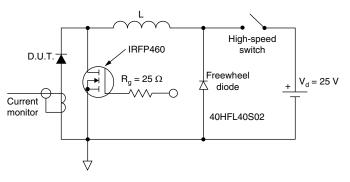


Fig. 8 - Unclamped Inductive Test Circuit

### Note

<sup>(1)</sup> Formula used:  $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$ ;

Pd = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);

 $Pd_{REV}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R \text{ at } V_{R1}$  = 80 % rated  $V_R$  applied

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## Vishay Semiconductors

### **ORDERING INFORMATION TABLE**

Dev

vice code	vs-	16	С	т	Q	100	PbF	
	1	2	3	4	5	6	7	
	1 - 2 - 3 - 4 -	Cur Circ C =	Vishay Semiconductors product Current rating (16 = 16 A) Circuit configuration C = Common cathode Package					
	5 - 6 - 7 -	Volt	Schottky "Q" series060 = 60Voltage rating080 = 80100 = 100Environmental digit					V

• -N3 = Halogen-free, RoHS compliant, and totally lead (Pb)-free

ORDERING INFORMATION (Example)							
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION				
VS-16CTQ060PbF	50	1000	Antistatic plastic tube				
VS-16CTQ060-N3	50	1000	Antistatic plastic tube				
VS-16CTQ080PbF	50	1000	Antistatic plastic tube				
VS-16CTQ080-N3	50	1000	Antistatic plastic tube				
VS-16CTQ100PbF	50	1000	Antistatic plastic tube				
VS-16CTQ100-N3	50	1000	Antistatic plastic tube				

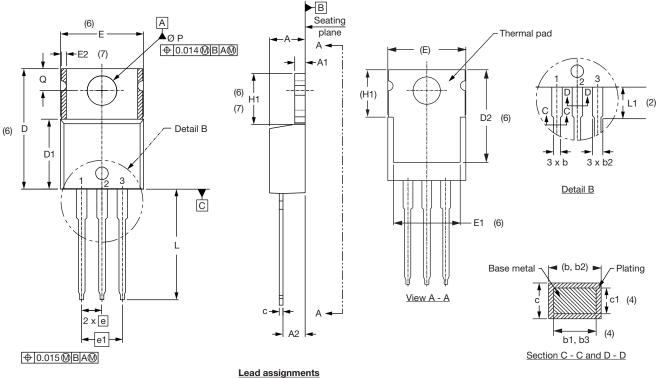
LINKS TO RELATED DOCUMENTS					
Dimensions www.vishay.com/doc?95222					
Part marking information	TO-220AB PbF	www.vishay.com/doc?95225			
	TO-220AB -N3	www.vishay.com/doc?95028			
SPICE model		www.vishay.com/doc?95279			

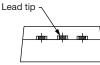


**Vishay Semiconductors** 

**TO-220AB** 

### **DIMENSIONS** in millimeters and inches





_ead	assi	gni	ne	nts
		-		

**Diodes** 

3. - Anode

1. - Anode/open 2. - Cathode

SYMBOL	MILLIN	IETERS	INC	NOTES	
STMBOL	MIN.	MAX.	MIN.	MAX.	NOTES
А	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
с	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6

#### Notes

- <sup>(1)</sup> Dimensioning and tolerancing as per ASME Y14.5M-1994
- <sup>(2)</sup> Lead dimension and finish uncontrolled in L1
- <sup>(3)</sup> Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed  $0.127 \text{ mm} (0.005^{\circ})$  per side. These dimensions are measured at the outermost extremes of the plastic body
- $^{\left( 4\right) }$  Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimensions: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1

SYMBOL	MILLIN	MILLIMETERS		INCHES		
STIVIDOL	MIN.	MAX.	MIN.	MAX.	NOTES	
E	10.11	10.51	0.398	0.414	3, 6	
E1	6.86	8.89	0.270	0.350	6	
E2	-	0.76	-	0.030	7	
е	2.41	2.67	0.095	0.105		
e1	4.88	5.28	0.192	0.208		
H1	6.09	6.48	0.240	0.255	6, 7	
L	13.52	14.02	0.532	0.552		
L1	3.32	3.82	0.131	0.150	2	
ØР	3.54	3.73	0.139	0.147		
Q	2.60	3.00	0.102	0.118		
θ	90° to 93°		90° to 93°			

Conforms to JEDEC outline TO-220AB

- $^{(7)}$  Dimensions E2 x H1 define a zone where stamping and singulation irregularities are allowed
- Outline conforms to JEDEC TO-220, except A2 (maximum) and (8) D2 (minimum) where dimensions are derived from the actual package outline

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