

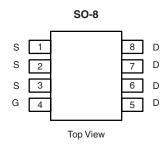
P-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)		
	0.011 at V _{GS} = - 10 V	- 13.7		
- 20	0.014 at V _{GS} = - 4.5 V	- 12.3		
	0.020 at V _{GS} = - 2.5 V	- 10.3		

FEATURES

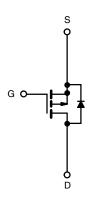
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs





Ordering Information: Si4463BDY-T1-E3 (Lead (Pb)-free)

Si4463BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T	A = 25 °C, unle	ss otherwise r	noted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 20		V
Gate-Source Voltage		V _{GS}	± 12		
Continuous Dunin Comment /T 150 90\8	T _A = 25 °C	- I _D	- 13.7	- 9.8	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		- 11.1	- 7.9	•
Pulsed Drain Current		I _{DM}	- 50		Α
Continuous Source Current (Diode Conduction) ^a		I _S	- 2.7	- 1.36	
	T _A = 25 °C	P_{D}	3.0	1.5	W
Maximum Power Dissipation ^a	T _A = 70 °C] rD	1.9	0.95	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum boration to Ambienta	t ≤ 10 s	R_{thJA}	35	42	
Maximum Junction-to-Ambient ^a	Steady State	□thJA	70	84	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

Vishay Siliconix



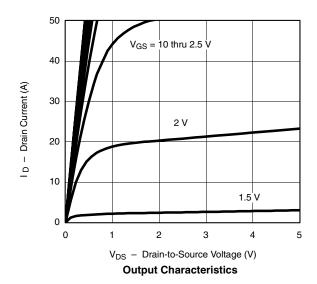
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions		Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.6		- 1.4	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 70 °C			- 1	μΑ	
Zero Gate Voltage Drain Current					- 10		
On-State Drain Current ^a	n Current ^a $I_{D(on)}$ $V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$		- 30			Α	
		V _{GS} = - 10 V, I _D = - 13.7 A	0.0085 0.01		0.011		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 12.3 A		0.010	0 0.014 Ω		
		V _{GS} = - 2.5 V, I _D = - 5 A		0.015	0.020	1	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 13.7 A		44		S	
Diode Forward Voltage ^a	V_{SD}	I _S = - 2.7 A, V _{GS} = 0 V		- 0.7	- 1.1	V	
Dynamic ^b							
Total Gate Charge	Q_g			37	56		
Gate-Source Charge	Q_{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -13.7 \text{ A}$		8.7		nC	
Gate-Drain Charge	Q_{gd}			11			
Gate Resistance	R_g	f = 1 MHz		2.7		Ω	
Turn-On Delay Time	t _{d(on)}			35	55		
Rise Time	t _r	V_{DD} = - 10 V, R_L = 10 Ω		60	90		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		115	170	ns	
Fall Time	t _f			75	115		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 2.3 A, dl/dt = 100 A/μs		50	75		

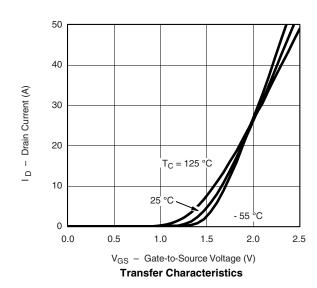
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

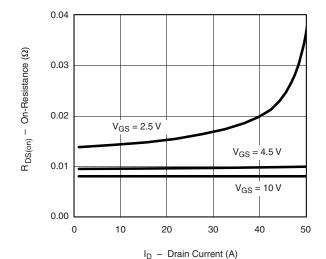
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



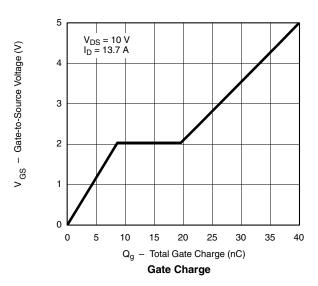




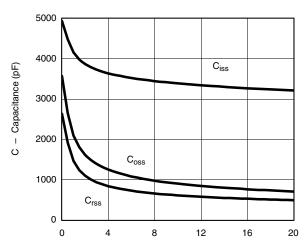
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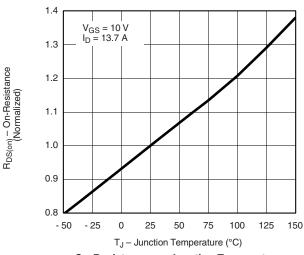
On-Resistance vs. Drain Current



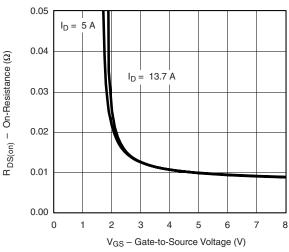
Source-Drain Diode Forward Voltage



V_{DS} - Drain-to-Source Voltage (V) **Capacitance**



On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

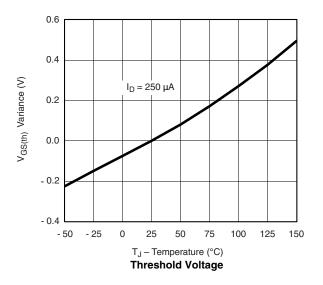
50

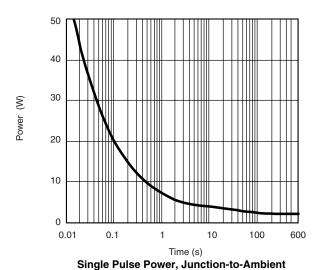
Source Current (A)

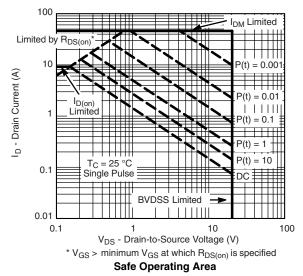
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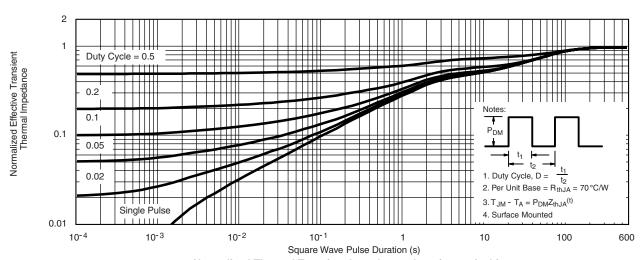
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





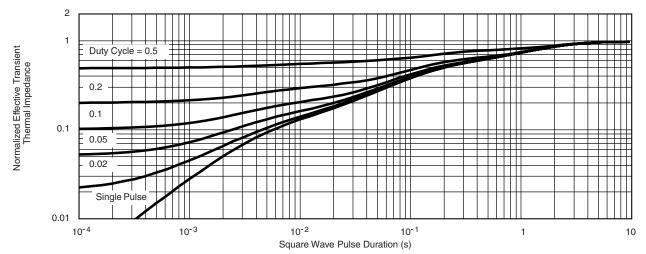




Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

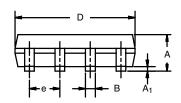
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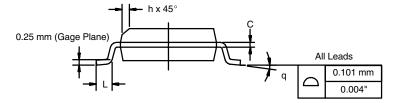
Document Number: 72789 S09-0393-Rev. C, 09-Mar-09



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I. 11-Sep-06					

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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