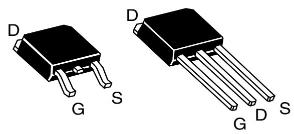
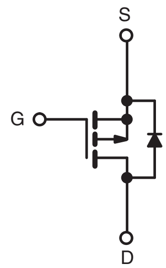
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | - 50 | |
| $R_{DS(on)}$ ($\Omega$) | $V_{GS}$ = - 10 V | 0.50 |
| $Q_g$ (Max.) (nC) | 9.1 | |
| $Q_{gs}$ (nC) | 3.0 | |
| $Q_{gd}$ (nC) | 5.9 | |
| Configuration | Single | |

**DPAK (TO-252)** **IPAK (TO-251)**




P-Channel MOSFET

## FEATURES

- Surface Mountable (Order as IRFR9010, SiHFR9010)
- Straight Lead Option (Order as IRFU9010, SiHFU9010)
- Repetitive Avalanche Ratings
- Dynamic dV/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE Available

## DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt capability.

The power MOSFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface mount package brings the advantages of power MOSFETs to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9010, SiHFR9010 is provided on 16 mm tape. The straight lead option IRFU9010, SiHFU9010 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

| ORDERING INFORMATION | | | | |
|---|---|---|---|---|
| Package | DPAK (TO-252) | DPAK (TO-252) | DPAK (TO-252) | IPAK (TO-251) |
| Lead (Pb)-free and Halogen-free | SiHFR9010-GE3 | SiHFR9010TR-GE3[a] | SiHFR9010TRL-GE3[a] | SiHFU9010-GE3 |
| Lead (Pb)-free | IRFR9010PbF | IRFR9010TRPbF[a] | IRFR9010TRLPbF[a] | IRFU9010PbF |
| | SiHFR9010-E3 | SiHFR9010T-E3[a] | SiHFR9010TL-E3[a] | SiHFU9010-E3 |

**Note**
a. See device orientation.

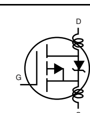
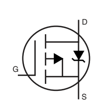
| **ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | | $V_{DS}$ | - 50 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current | $V_{GS}$ at - 10 V | $T_C$ = 25 °C | $I_D$ | - 5.3 | A |
| | | $T_C$ = 100 °C | | - 3.3 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | - 21 | |
| Linear Derating Factor | | | | 0.20 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 136 | mJ |
| Repetitive Avalanche Current[a] | | | $I_{AR}$ | - 5.3 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 2.5 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 25 | W |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 5.8 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature)[d] | for 10 s | | | 300 | |

**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
b. $V_{DD}$ = - 25 V, starting $T_J$ = 25 °C, L = 9.7 mH, $R_g$ = 25 $\Omega$, peak $I_L$ = - 5.3 A.
c. $I_{SD} \leq$ - 5.3 A, dI/dt $\leq$ - 80 A/μs, $V_{DD} \leq$ 40 V, $T_J \leq$ 150 °C, suggested $R_g$ = 24 $\Omega$.
d. 0.063" (1.6 mm) from case.

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | - | 110 | °C/W |
| Case-to-Sink | $R_{thCS}$ | - | 1.7 | - | |
| Maximum Junction-to-Case (Drain)[a] | $R_{thJC}$ | - | - | 5.0 | |

**Note**

a. Mounting pad must cover heatsink surface area.

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = - 250 μA | - 50 | - | - | V |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = - 250 μA | - 2.0 | - | - 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 500 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = max. rating, $V_{GS}$ = 0 V | - | - | - 250 | μA |
| | | $V_{DS}$ = 0.8 x max. rating, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | - 1000 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = - 10 V; $I_D$ = - 2.8 A[b] | - | 0.35 | 0.5 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ ≤ - 50 V, $I_{DS}$ = - 2.8 A | 1.1 | 1.7 | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = - 25 V, f = 1.0 MHz, see fig. 9 | - | 240 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 160 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 30 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = - 10 V; $I_D$ = - 4.7 A, $V_{DS}$ = 0.8 x max. rating, see fig. 16 (Independent operating temperature) | - | 6.1 | 9.1 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 2.0 | 3.0 | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 3.9 | 5.9 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = - 25 V, $I_D$ = - 4.7 A, $R_g$ = 24 Ω, $R_D$ = 5.6 Ω, see fig. 15 (Independent operating temperature) | - | 6.1 | 9.2 | ns |
| Rise Time | $t_r$ | | - | 47 | 71 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 13 | 20 | |
| Fall Time | $t_f$ | | - | 35 | 59 | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact.  | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | - 5.3 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | - | - | - 18 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = - 5.3 A, $V_{GS}$ = 0 V[b] | - | - | - 5.5 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = - 4,7 A, dI/dt = 100 A/μs[b] | 33 | 75 | 160 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | 0.090 | 0.22 | 0.52 | μC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

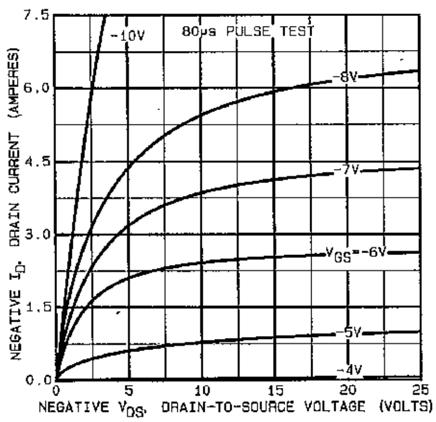



**Fig. 1 - Typical Output Characteristics**

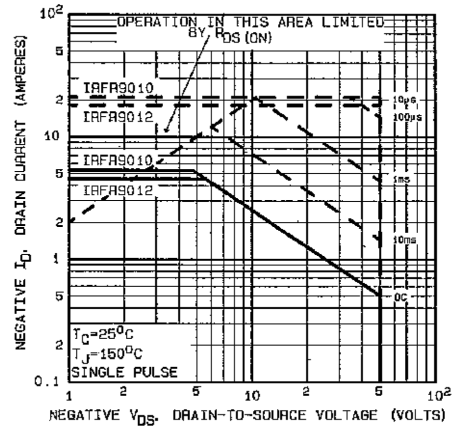



**Fig. 4 - Maximum Safe Operating Area**

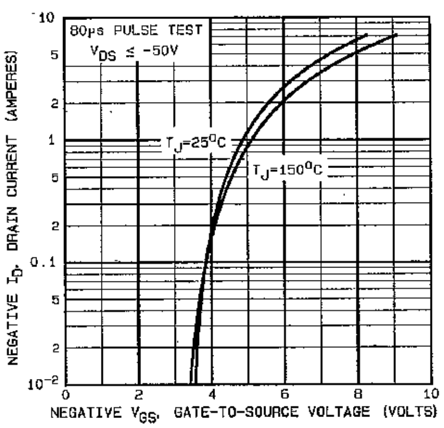



**Fig. 2 - Typical Transfer Characteristics**

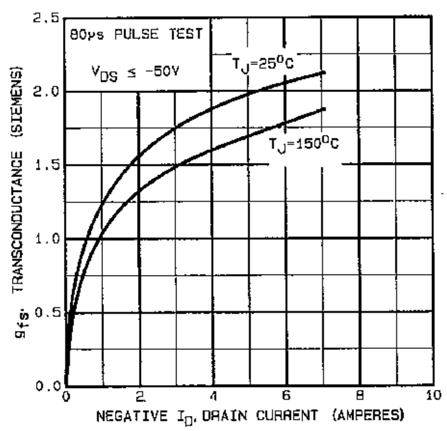



**Fig. 5 - Typical Transconductance vs. Drain Current**

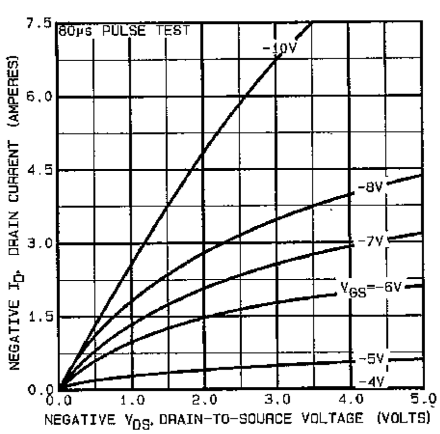



**Fig. 3 - Typical Saturation Characteristics**

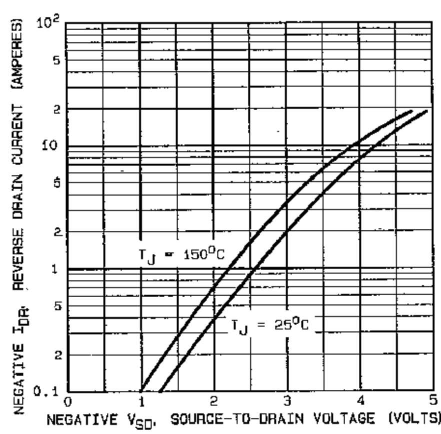



**Fig. 6 - Typical Source-Drain Diode Forward Voltage**

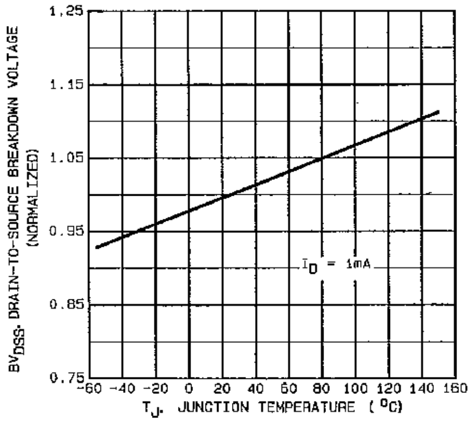



Fig. 7 - Breakdown Voltage vs. Temperature

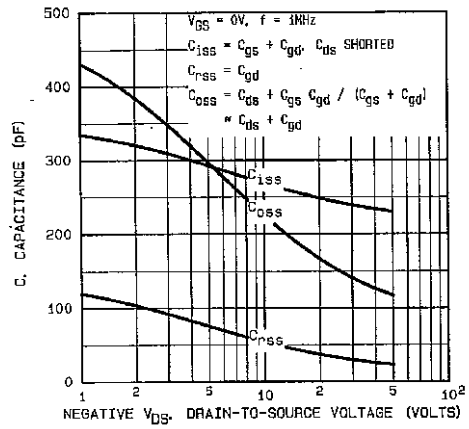



Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

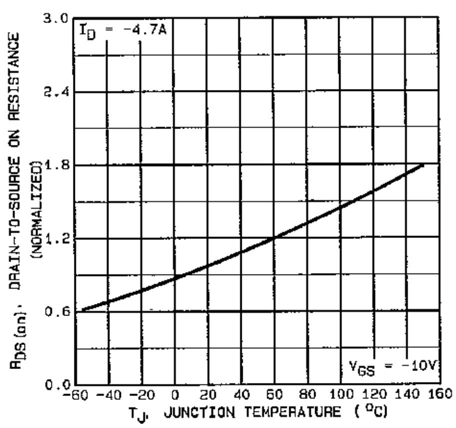



Fig. 8 - Normalized On-Resistance vs. Temperature

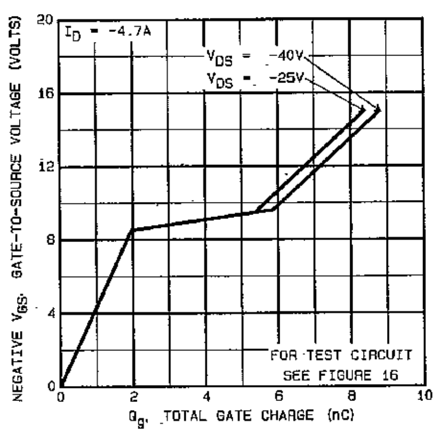



Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

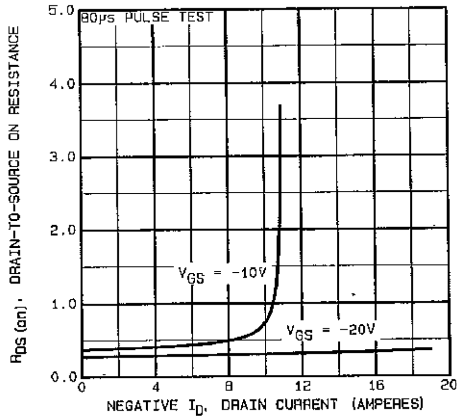



**Fig. 11 - Typical On-Resistance vs. Drain Current**

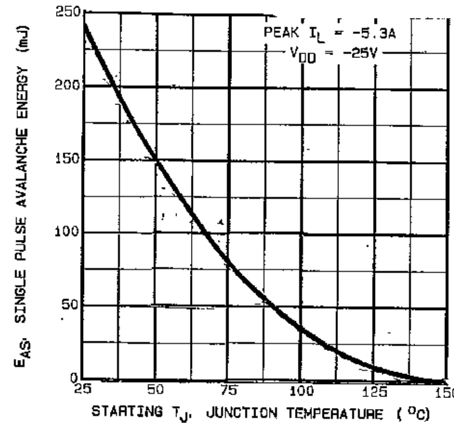



**Fig. 13a - Maximum Avalanche vs. Starting Junction Temperature**

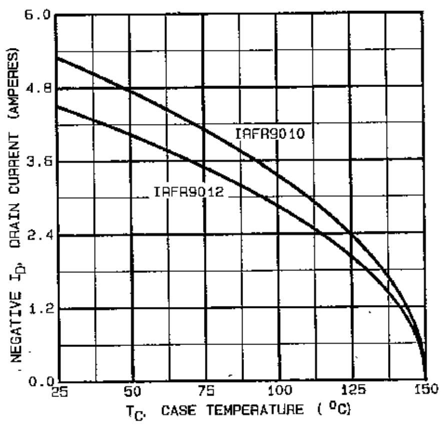



**Fig. 12 - Maximum Drain Current vs. Case Temperature**

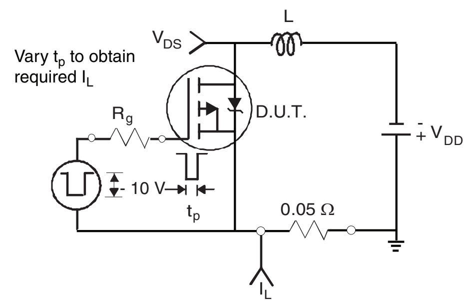



**Fig. 13b - Unclamped Inductive Test Circuit**

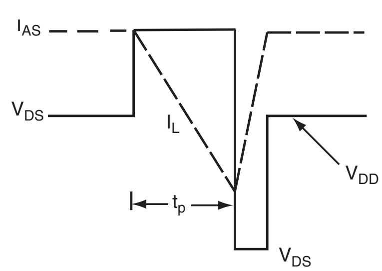



**Fig. 13c - Unclamped Inductive Waveforms**

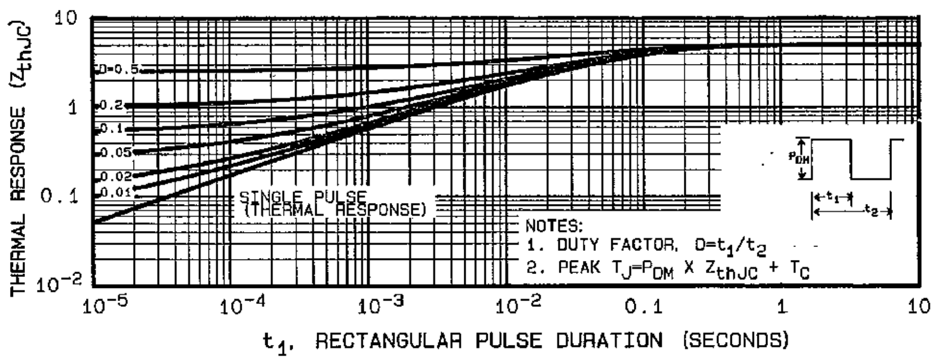



**Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration**

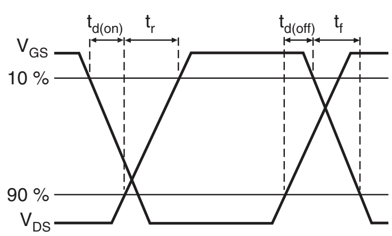



**Fig. 15a - Switching Time Waveforms**

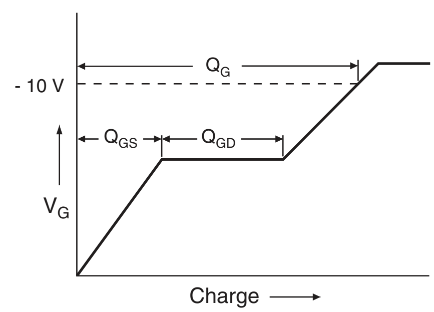



**Fig. 16a - Basic Gate Charge Waveform**

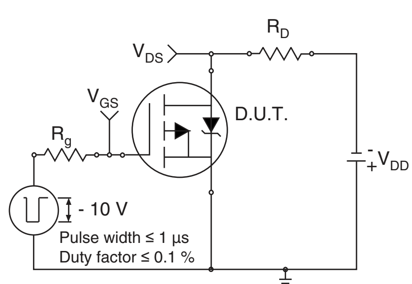



**Fig. 15b - Switching Time Test Circuit**

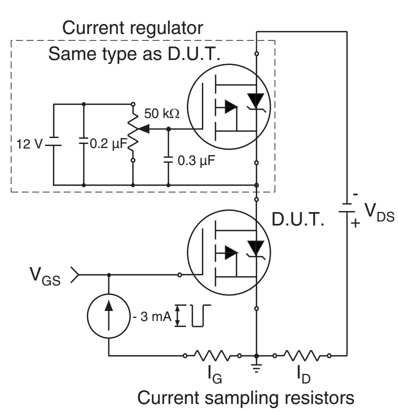
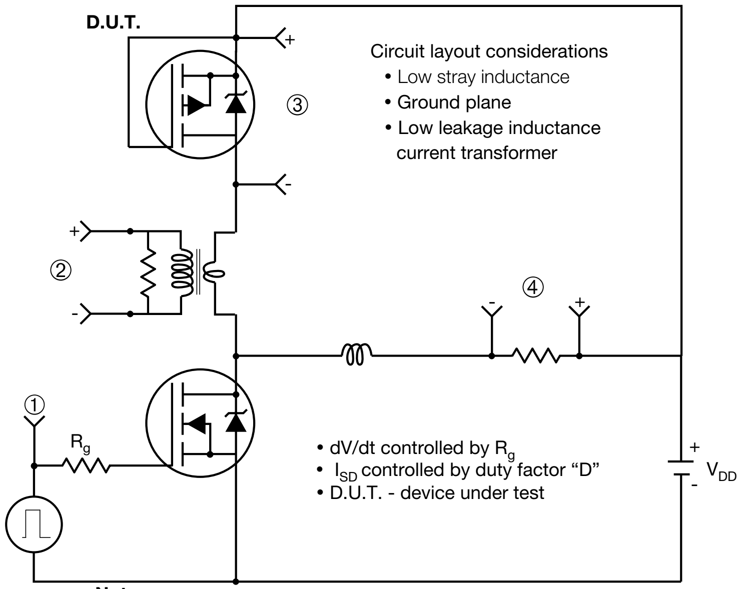
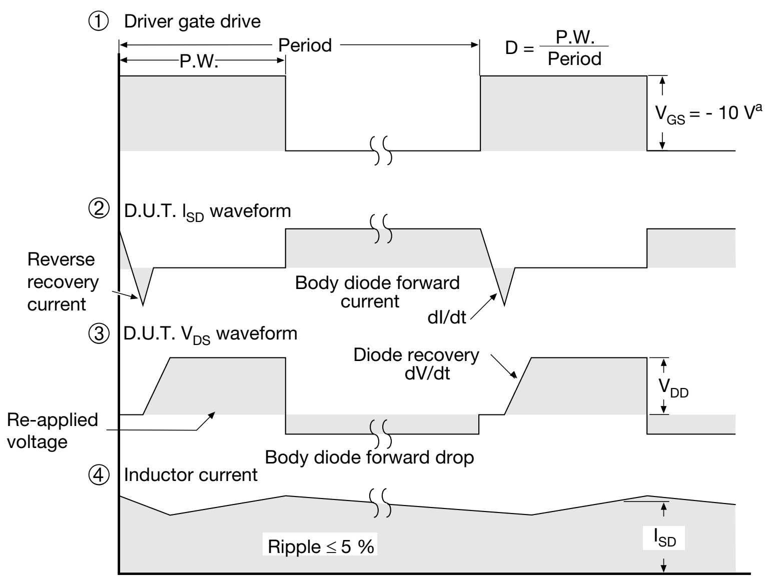



**Fig. 16b - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**




**Note**
• Compliment N-Channel of D.U.T. for driver




**Note**
a. $V_{GS}$ = - 5 V for logic level and - 3 V drive devices

**Fig. 17 - For P-Channel**

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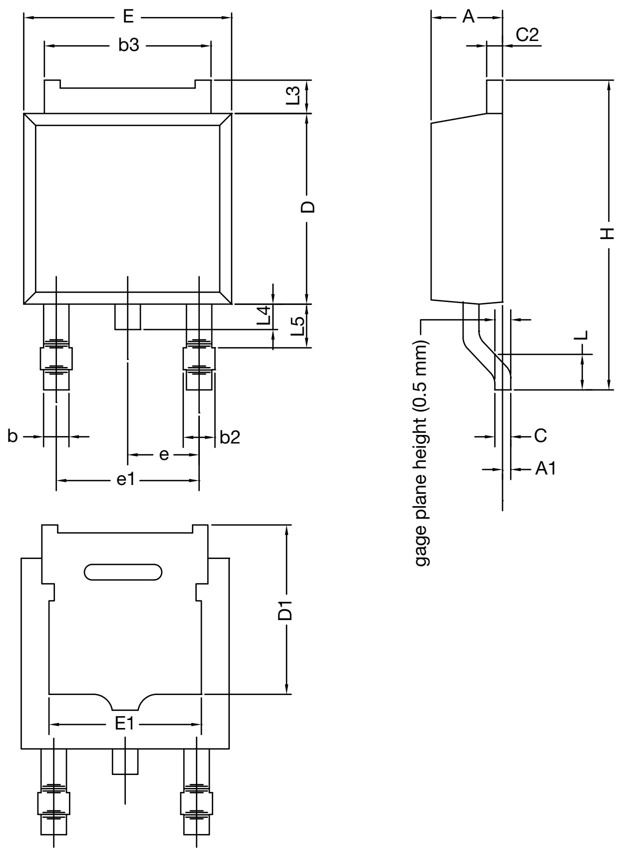
# TO-252AA Case Outline

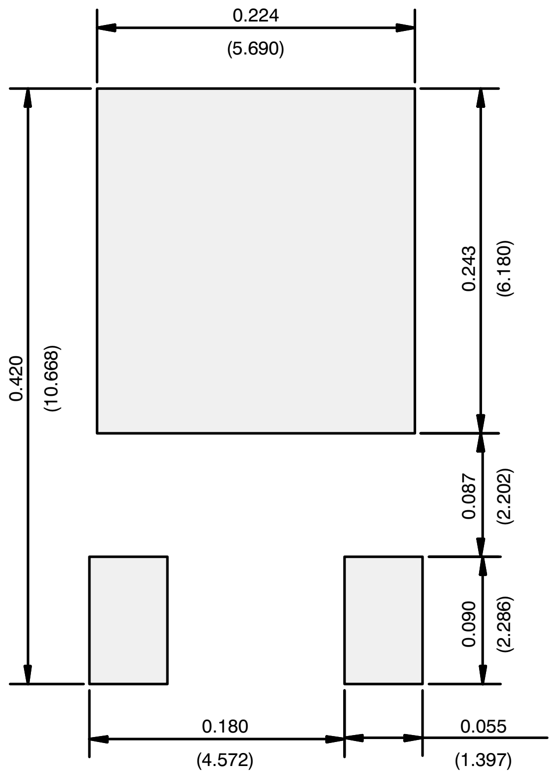



| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 2.18 | 2.38 | 0.086 | 0.094 |
| A1 | - | 0.127 | - | 0.005 |
| b | 0.64 | 0.88 | 0.025 | 0.035 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 |
| b3 | 4.95 | 5.46 | 0.195 | 0.215 |
| C | 0.46 | 0.61 | 0.018 | 0.024 |
| C2 | 0.46 | 0.89 | 0.018 | 0.035 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 4.10 | - | 0.161 | - |
| E | 6.35 | 6.73 | 0.250 | 0.265 |
| E1 | 4.32 | - | 0.170 | - |
| H | 9.40 | 10.41 | 0.370 | 0.410 |
| e | 2.28 BSC | | 0.090 BSC | |
| e1 | 4.56 BSC | | 0.180 BSC | |
| L | 1.40 | 1.78 | 0.055 | 0.070 |
| L3 | 0.89 | 1.27 | 0.035 | 0.050 |
| L4 | - | 1.02 | - | 0.040 |
| L5 | 1.01 | 1.52 | 0.040 | 0.060 |
| ECN: T16-0236-Rev. P, 16-May-16<br>DWG: 5347 | | | | |

**Notes**

- Dimension L3 is for reference only.

### RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)




Recommended Minimum Pads
Dimensions in Inches/(mm)

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