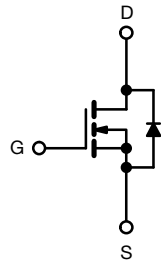


Power MOSFET



N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Surface-mount (IRFR420, SiHFR420)
- Straight lead (IRFU420, SiHFU420)
- Available in tape and reel
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	3.0
Q_g max. (nC)	19	
Q_{gs} (nC)	3.3	
Q_{gd} (nC)	13	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface-mount applications.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFR420-GE3	SiHFR420TR-GE3 ^a	SiHFR420TRL-GE3 ^a	SiHFR420TRR-GE3 ^a	SiHFU420-GE3
	IRFR420PbF-BE3	IRFR420TRPbF-BE3	IRFR420TRLPbF-BE3	-	-
Lead (Pb)-free	IRFR420PbF	IRFR420TRPbF ^a	IRFR420TRLPbF ^a	IRFR420TRRPbF ^a	IRFU420PbF

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	500	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current	V_{GS} at 10 V	$T_C = 25^\circ\text{C}$	2.4
		$T_C = 100^\circ\text{C}$	1.5
Pulsed drain current ^a	I_{DM}	8.0	A
Linear derating factor		0.33	W/ $^\circ\text{C}$
Linear derating factor (PCB mount) ^e		0.020	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	400	mJ
Repetitive avalanche current ^a	I_{AR}	2.4	A
Repetitive avalanche energy ^a	E_{AR}	4.2	mJ
Maximum power dissipation	P_D	$T_C = 25^\circ\text{C}$	42
Maximum power dissipation (PCB mount) ^e		$T_A = 25^\circ\text{C}$	2.5
Peak diode recovery dV/dt ^c	dV/dt	3.5	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d	For 10 s	260	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50$ V, starting $T_J = 25^\circ\text{C}$, $L = 124$ mH, $R_g = 25 \Omega$, $I_{AS} = 2.4$ A (see fig. 12)
- $I_{SD} \leq 2.4$ A, $dI/dt \leq 50$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	110	°C/W
Maximum junction-to-ambient (PCB mount) ^a	R _{thJA}	-	50	
Maximum junction-to-case (drain)	R _{thJC}	-	3.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	500	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.59	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V	-	-	25	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C	-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 1.4 A ^b	-	-	3.0	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1.4 A	1.5	-	-	S
Dynamic						
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	360	-	pF
Output capacitance	C _{oss}		-	92	-	
Reverse transfer capacitance	C _{rss}		-	37	-	
Total gate charge	Q _g	V _{GS} = 10 V, I _D = 2.1 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	19	nC
Gate-source charge	Q _{gs}		-	-	3.3	
Gate-drain charge	Q _{gd}		-	-	13	
Turn-on delay time	t _{d(on)}	V _{DD} = 250 V, I _D = 2.1 A, R _g = 18 Ω, R _D = 120 Ω, see fig. 10 ^b	-	8.0	-	ns
Rise time	t _r		-	8.6	-	
Turn-off delay time	t _{d(off)}		-	33	-	
Fall time	t _f		-	16	-	
Gate input resistance	R _g	f = 1 MHz, open drain	1.8	-	12.6	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact	-	4.5	-	nH
Internal source inductance	L _S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode	-	-	2.4	A
Pulsed diode forward current ^a	I _{SM}		-	-	8.0	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 2.4 A, V _{GS} = 0 V ^b	-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 2.1 A, dI/dt = 100 A/μs ^b	-	260	520	ns
Body diode reverse recovery charge	Q _{rr}		-	0.70	1.4	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

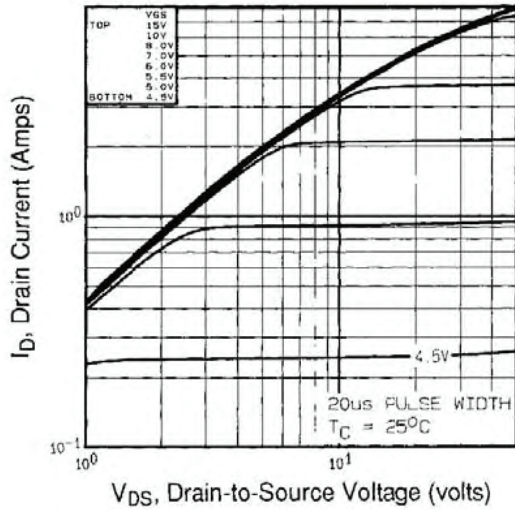


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

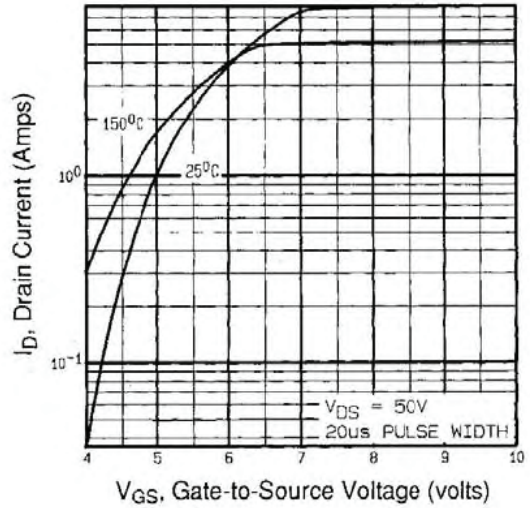


Fig. 3 - Typical Transfer Characteristics

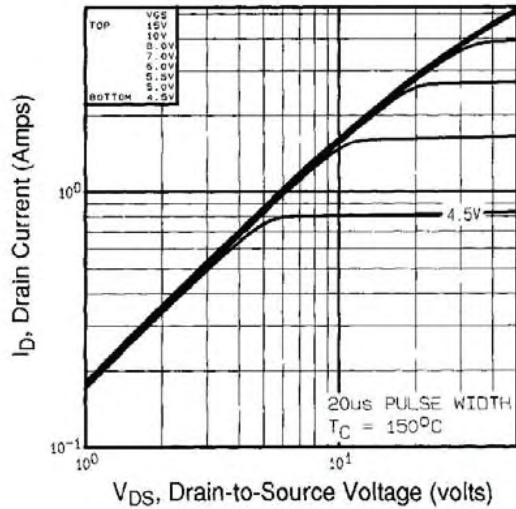


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

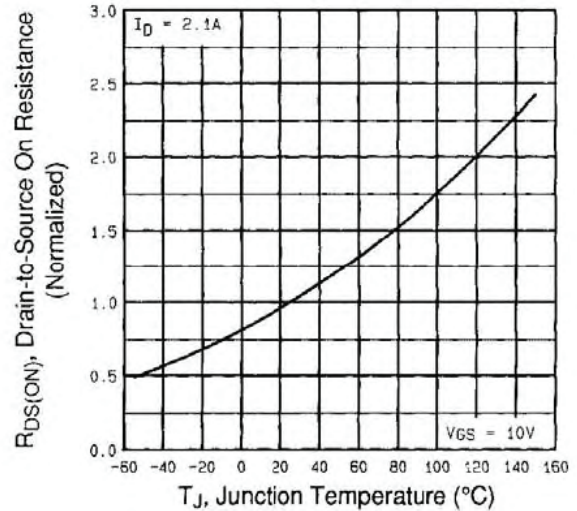


Fig. 4 - Normalized On-Resistance vs. Temperature

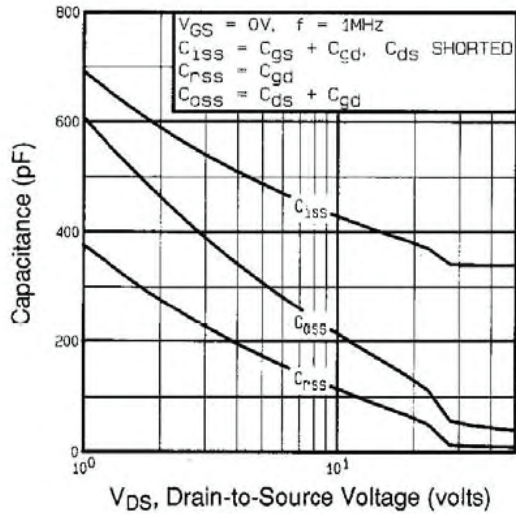


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

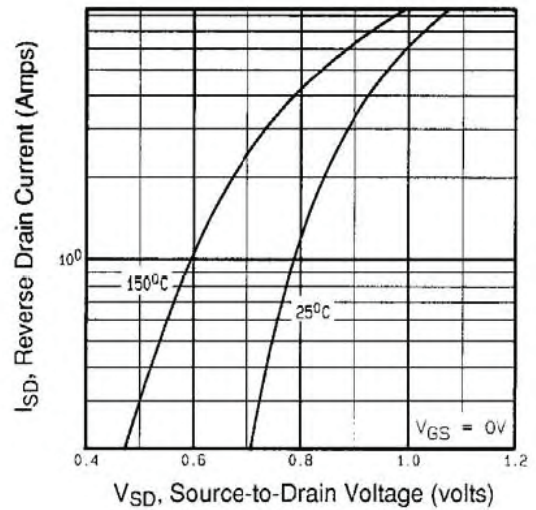


Fig. 7 - Typical Source-Drain Diode Forward Voltage

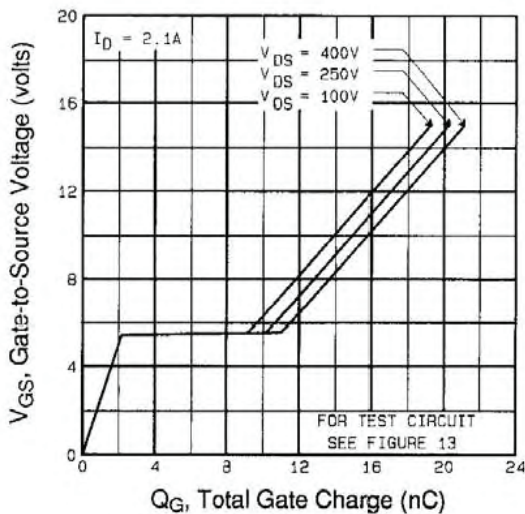


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

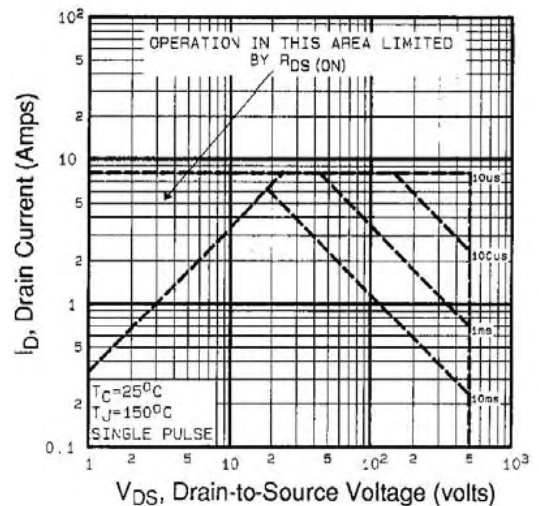


Fig. 8 - Maximum Safe Operating Area

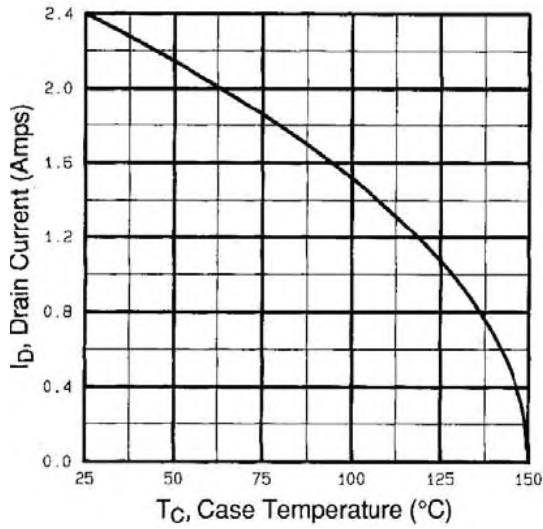


Fig. 9 - Maximum Drain Current vs. Case Temperature

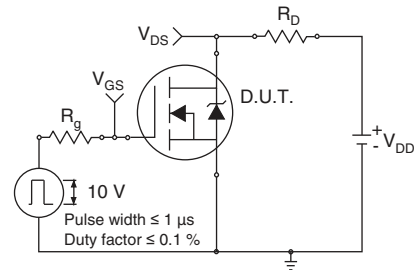


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

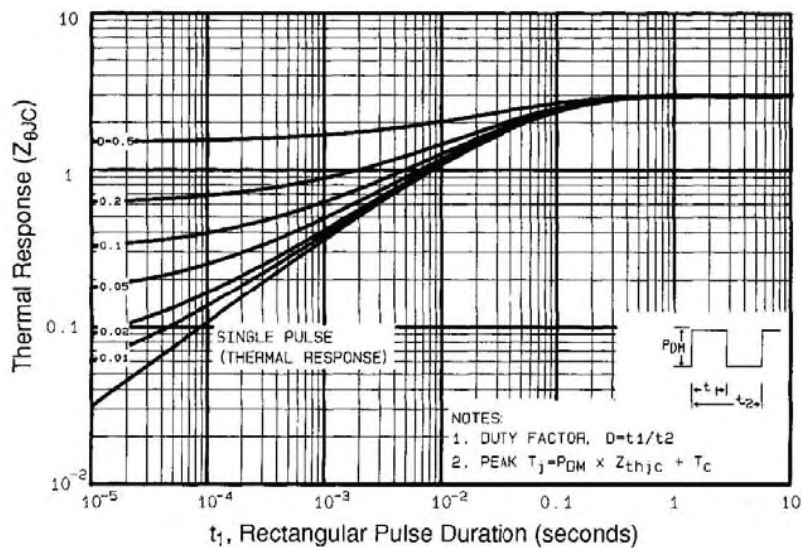


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

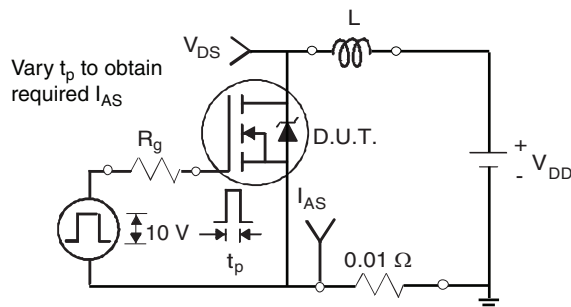


Fig. 12a - Unclamped Inductive Test Circuit

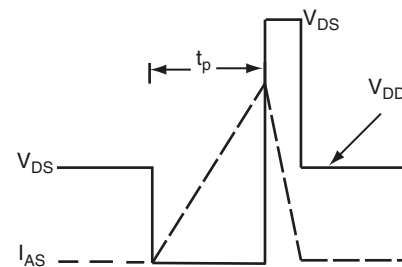


Fig. 12b - Unclamped Inductive Waveforms

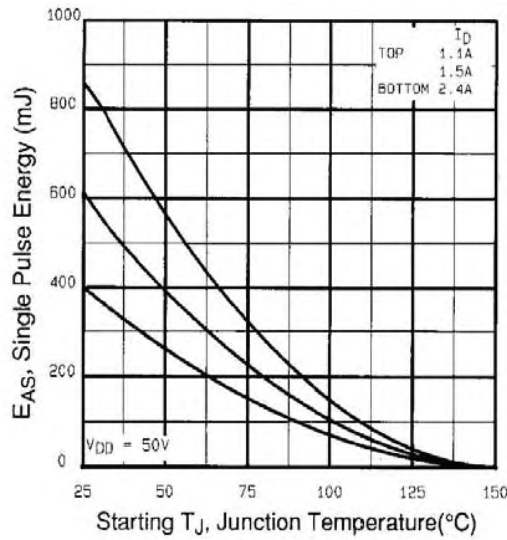


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

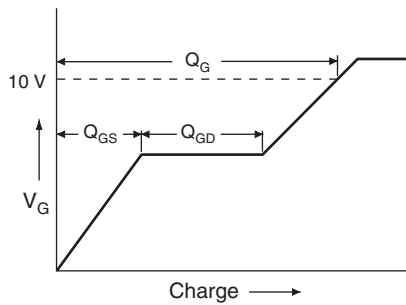


Fig. 13a - Basic Gate Charge Waveform

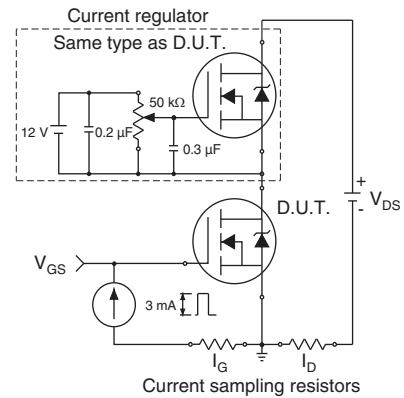
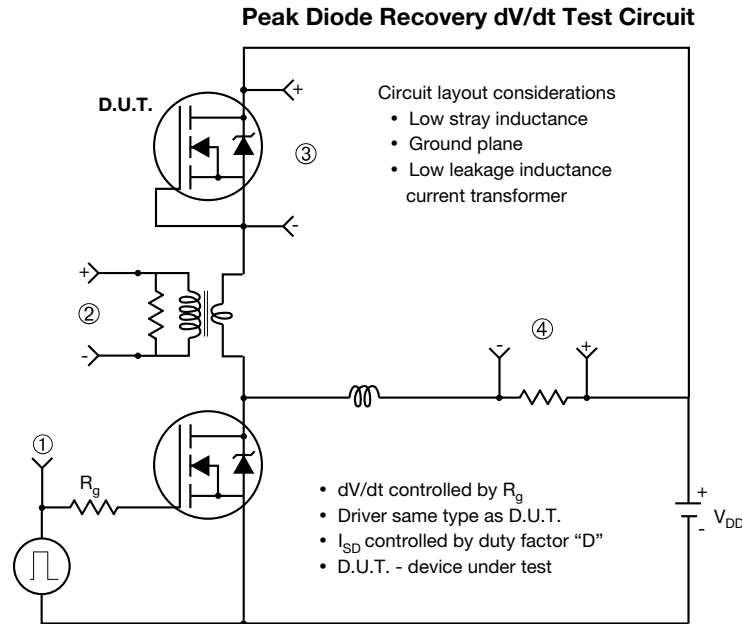


Fig. 13b - Gate Charge Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91275.



TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

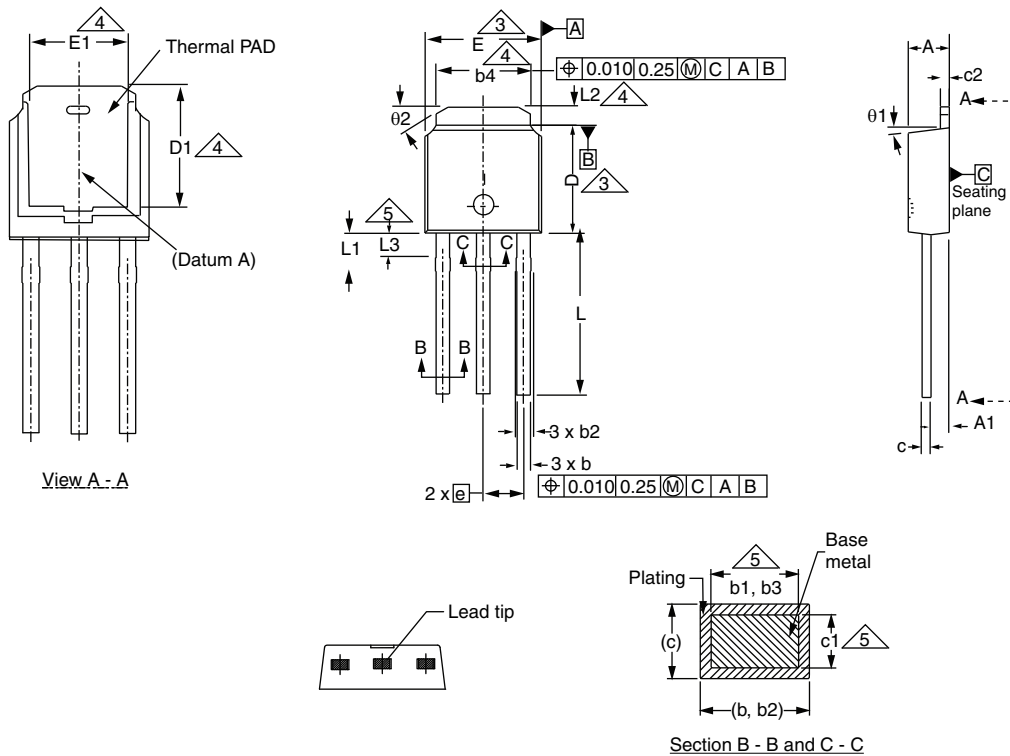
Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
 DWG: 5347

Case Outline for TO-251AA (High Voltage)

OPTION 1:



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

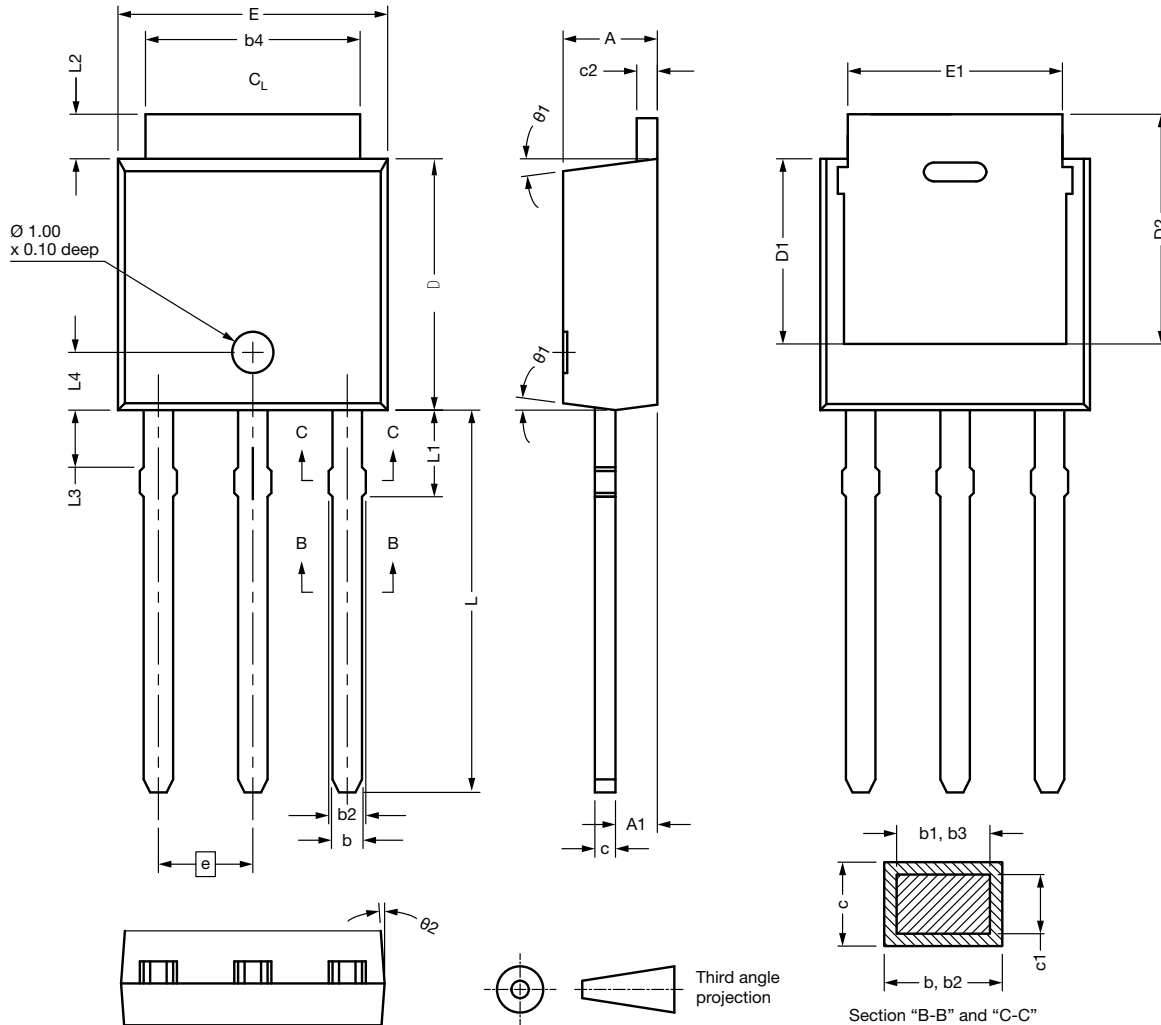
ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA



OPTION 2: FACILITY CODE = N



DIM.	MIN.	NOM.	MAX.
A	2.180	2.285	2.390
A1	0.890	1.015	1.140
b	0.640	0.765	0.890
b1	0.640	0.715	0.790
b2	0.760	0.950	1.140
b3	0.760	0.900	1.040
b4	4.950	5.205	5.460
c	0.460	-	0.610
c1	0.410	-	0.560
c2	0.460	-	0.610
D	5.970	6.095	6.220
D1	4.300	-	-

DIM.	MIN.	NOM.	MAX.
D2	5.380	-	-
E	6.350	6.540	6.730
E1	4.32	-	-
e	2.29 BSC		
L	8.890	9.270	9.650
L1	1.910	2.100	2.290
L2	0.890	1.080	1.270
L3	1.140	1.330	1.520
L4	1.300	1.400	1.500
θ_1	0°	7.5°	15°
θ_2	4°	-	-

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimension are in millimeters, angles are in degrees
- Heat sink side flash is max. 0.8 mm

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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