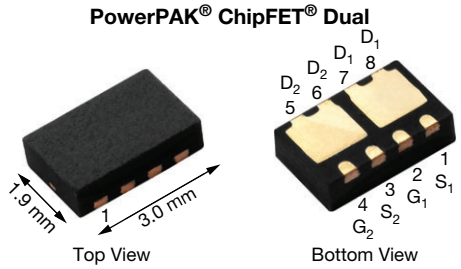
N- and P-Channel 20 V (D-S) MOSFET

PowerPAK® ChipFET® Dual



Marking code: EA

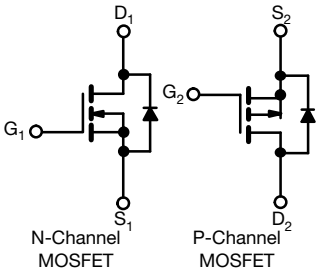
FEATURES

- TrenchFET® power MOSFETs
- Thermally enhanced PowerPAK ChipFET package
  - Small footprint area
  - Low on-resistance
  - Thin 0.8 mm profile
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Complementary MOSFET for portable devices
  - Ideal for buck-boost circuits



PRODUCT SUMMARY

	N-CHANNEL	P-CHANNEL
V_{DS} (V)	20	-20
$R_{DS(on)}$ (Ω) at V_{GS} = ± 4.5 V	0.039	0.072
$R_{DS(on)}$ (Ω) at V_{GS} = ± 2.5 V	0.045	0.100
$R_{DS(on)}$ (Ω) at V_{GS} = ± 1.8 V	0.055	0.131
Q_g typ. (nC)	6	5.5
I_D (A) [a]	6	-6
Configuration	N- and p-pair	

ORDERING INFORMATION

Package	PowerPAK ChipFET
Lead (Pb)-free and halogen-free	Si5517DU-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage		V_{DS}	20	-20	V
Gate-source voltage		V_{GS}	± 8	± 8	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	6 [a]	-6 [a]	A
	T_C = 70 °C		6 [a]	-6 [a]	
	T_A = 25 °C		7.2 [b, c]	-4.6 [b, c]	
	T_A = 70 °C		5.8 [b, c]	-3.7 [b, c]	
Pulsed drain current		I_{DM}	20	-15	
Source-drain current diode current	T_C = 25 °C	I_S	6.9	-6.9	
	T_A = 25 °C		1.9 [b, c]	-1.9 [b, c]	
Maximum power dissipation	T_C = 25 °C	P_D	8.3	8.3	W
	T_C = 70 °C		5.3	5.3	
	T_A = 25 °C		2.3 [b, c]	2.3 [b, c]	
	T_A = 70 °C		1.5 [b, c]	1.5 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [d, e]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient [b, f]	t ≤ 5 s	R_{thJA}	45	55	45	55	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	12	15	12	15	

Notes

a. Based on T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 5 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 105 °C/W for both channels

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.** [a]	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 1 mA	N-Ch	20	-	-	V
		V_{GS} = 0 V, I_D = -1 mA	P-Ch	-20	-	-	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch	-	17	-	mV/°C
		I_D = -250 µA	P-Ch	-	-20	-	
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch	-	-2.6	-	
		I_D = -250 µA	P-Ch	-	2.4	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.4	-	1	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-0.4	-	-1	
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V	N-Ch	-	-	100	nA
			P-Ch	-	-	-100	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch	-	-	1	µA
		V_{DS} = -20 V, V_{GS} = 0 V	P-Ch	-	-	-1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch	-	-	10	
		V_{DS} = -20 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch	-	-	-10	
On-state drain current [b]	$I_{D(on)}$	$V_{DS} \leq$ 5 V, V_{GS} = 4.5 V	N-Ch	20	-	-	A
		$V_{DS} \leq$ -5 V, V_{GS} = -4.5 V	P-Ch	-15	-	-	
Drain-source on-state resistance [b]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.4 A	N-Ch	-	0.0320	0.0390	Ω
		V_{GS} = -4.5 V, I_D = -3.3 A	P-Ch	-	0.0600	0.0720	
		V_{GS} = 2.5 V, I_D = 4.1 A	N-Ch	-	0.0370	0.0450	
		V_{GS} = -2.5 V, I_D = -2.8 A	P-Ch	-	0.0830	0.1000	
		V_{GS} = 1.8 V, I_D = 1.8 A	N-Ch	-	0.0455	0.0550	
		V_{GS} = -1.8 V, I_D = -0.76 A	P-Ch	-	0.1080	0.1310	
Forward transconductance [b]	g_{fs}	V_{DS} = 10 V, I_D = 4.4 A	N-Ch	-	22	-	S
		V_{DS} = -10 V, I_D = -3.3 A	P-Ch	-	0.9	-	
Dynamic [a]							
Input capacitance	C_{iss}	N-channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz P-channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	-	520	-	pF
			P-Ch	-	455	-	
Output capacitance	C_{oss}		N-Ch	-	100	-	
			P-Ch	-	105	-	
Reverse transfer capacitance	C_{rss}		N-Ch	-	60	-	
			P-Ch	-	65	-	
Total gate charge	Q_g	V_{DS} = 10 V, V_{GS} = 8 V, I_D = 4.4 A	N-Ch	-	10.5	16	nC
		V_{DS} = -10 V, V_{GS} = -8 V, I_D = -4.6 A	P-Ch	-	9.1	14	
		V_{DS} = 10 V, V_{GS} = 4.5 V I_D = 4.4 A	N-Ch	-	6	9	
		V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -1.8 A	P-Ch	-	5.5	8.5	
Gate-source charge	Q_{gs}	N-channel V_{DS} = 10 V, V_{GS} = 4.5 V I_D = 4.4 A P-channel V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -1.8 A	N-Ch	-	0.91	-	
			P-Ch	-	0.75	-	
Gate-drain charge	Q_{gd}		N-Ch	-	0.7	-	
			P-Ch	-	1.5	-	
Gate resistance	R_g	f = 1 MHz	N-Ch	-	1.9	-	Ω
			P-Ch	-	8	-	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.** [a]	**MAX.**	**UNIT**
Dynamic [a]							
Turn-on delay time	$t_{d(on)}$	N-channel V_{DD} = 10 V, R_L = 2.8 Ω, $I_D \cong$ 3.6 A, V_{GEN} = 4.5 V, R_g = 1 Ω P-channel V_{DD} = -10 V, R_L = 2.7 Ω, $I_D \cong$ -3.7 A, V_{GEN} = -4.5 V, R_g = 1 Ω	N-Ch	-	20	30	ns
			P-Ch	-	8	15	
Rise time	t_r		N-Ch	-	65	100	
			P-Ch	-	35	55	
Turn-off delay time	$t_{d(off)}$		N-Ch	-	40	60	
			P-Ch	-	40	60	
Fall time	t_f		N-Ch	-	10	15	
			P-Ch	-	55	85	
Turn-on delay time	$t_{d(on)}$	N-channel V_{DD} = 10 V, R_L = 2.8 Ω, $I_D \cong$ 3.6 A, V_{GEN} = 8 V, R_g = 1 Ω P-channel V_{DD} = -10 V, R_L = 2.7 Ω, $I_D \cong$ -3.7 A, V_{GEN} = -8 V, R_g = 1 Ω	N-Ch	-	5	10	
			P-Ch	-	5	10	
Rise time	t_r		N-Ch	-	12	20	
			P-Ch	-	15	25	
Turn-off delay time	$t_{d(off)}$		N-Ch	-	26	40	
			P-Ch	-	30	45	
Fall Time	t_f		N-Ch	-	8	15	
			P-Ch	-	45	70	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	T_C = 25 °C	N-Ch	-	-	6.9	A
			P-Ch	-	-	-6.9	
Pulse diode forward current [a]	I_{SM}		N-Ch	-	-	20	
			P-Ch	-	-	-15	
Body diode voltage	V_{SD}	I_S = 1.2 A, V_{GS} = 0 V	N-Ch	-	0.8	1.2	V
		I_S = -1.0 A, V_{GS} = 0 V	P-Ch	-	-0.8	-1.2	
Body diode reverse recovery time	t_{rr}	N-channel I_F = 1.2 A, di/dt = 100 A/µs, T_J = 25 °C P-channel I_F = -1 A, di/dt = -100 A/µs, T_J = 25 °C	N-Ch	-	45	70	ns
			P-Ch	-	30	60	
Body diode reverse recovery charge	Q_{rr}		N-Ch	-	21	32	nC
			P-Ch	-	15	30	
Reverse recovery fall time	t_a		N-Ch	-	29	-	ns
			P-Ch	-	11	-	
Reverse recovery rise time	t_b		N-Ch	-	16	-	
			P-Ch	-	19	-	

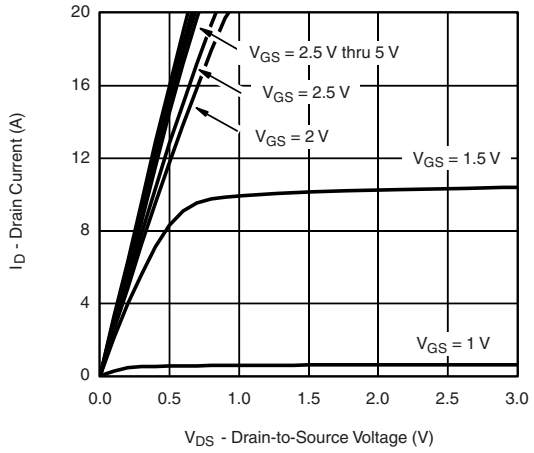
Notes

a. Guaranteed by design, not subject to production testing

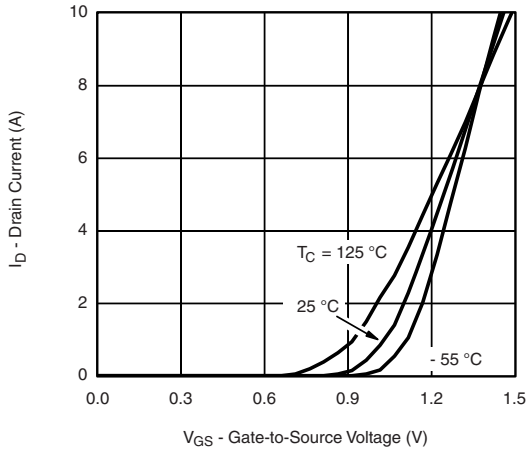
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

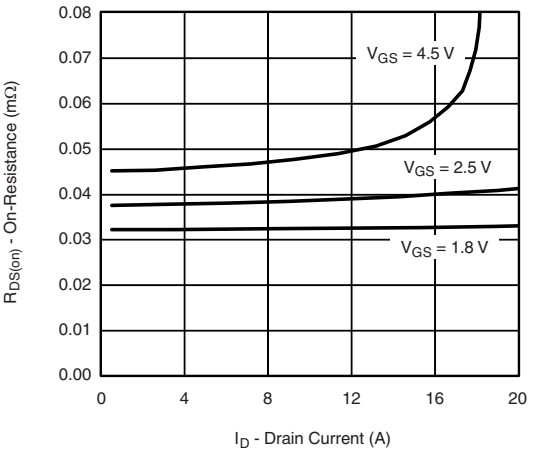
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



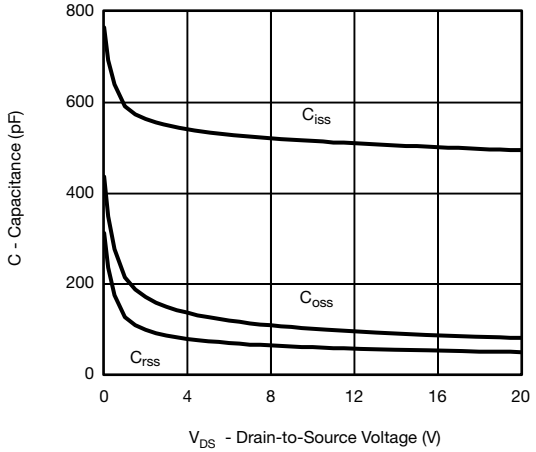
Output Characteristics



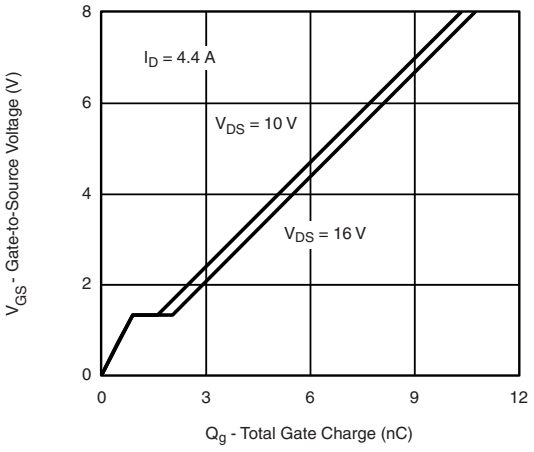
Transfer Characteristics



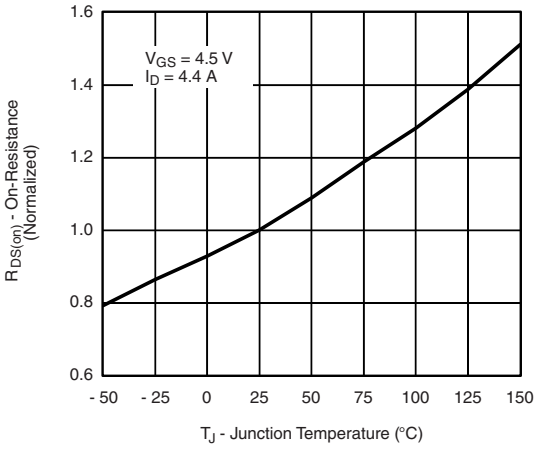
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

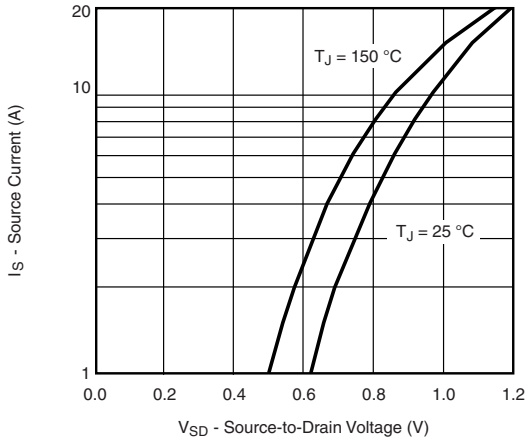


Gate Charge

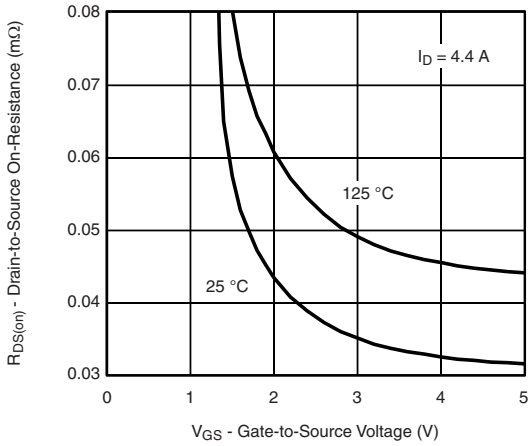


On-Resistance vs. Junction Temperature

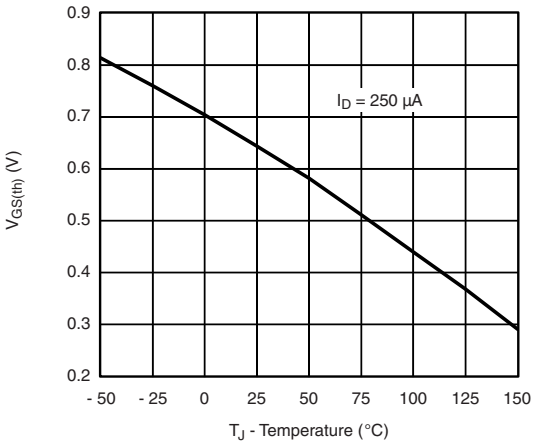
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



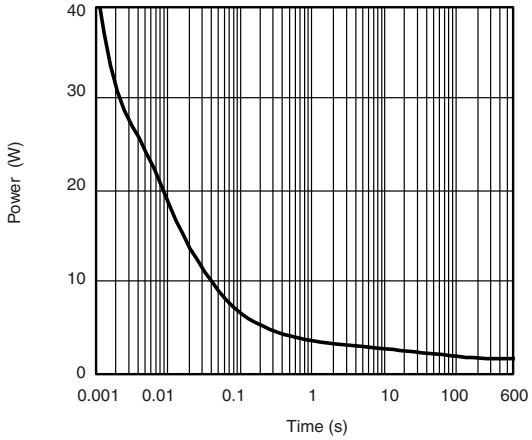
Source-Drain Diode Forward Voltage



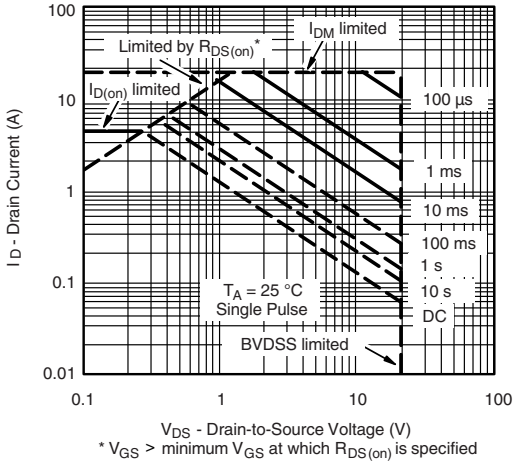
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

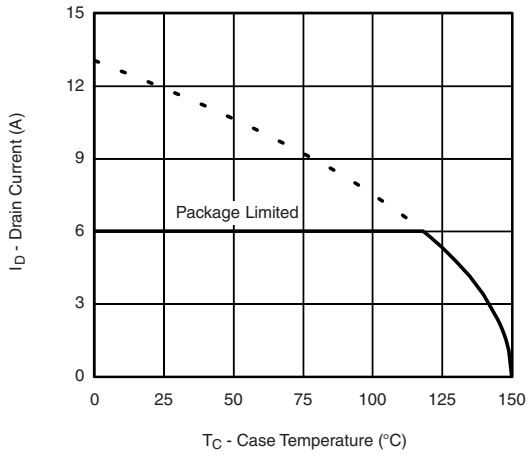


Single Pulse Power, Junction-to-Ambient

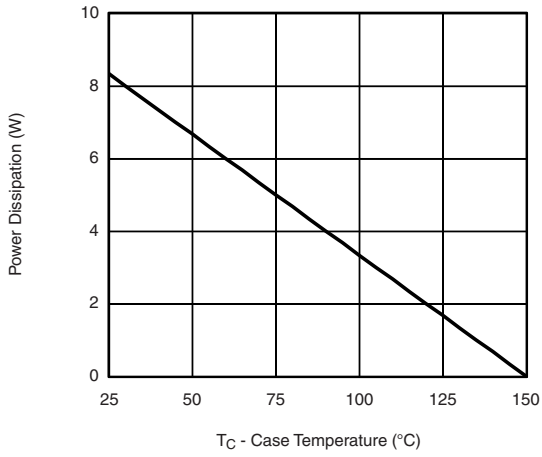


Safe Operating Area, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

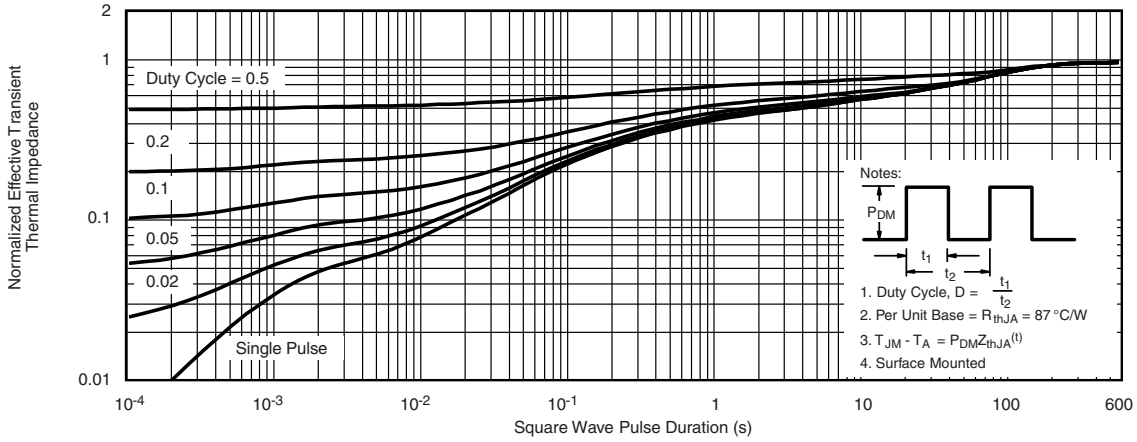


Power Derating

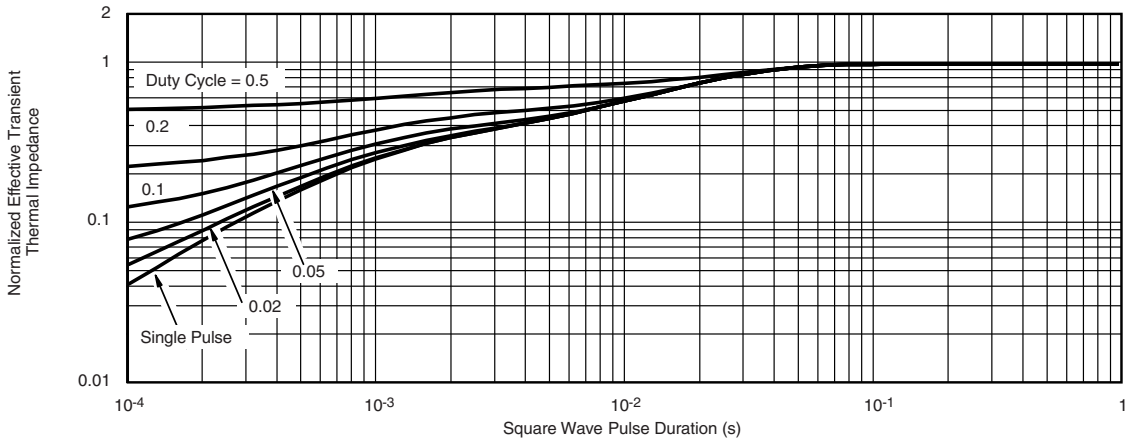
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

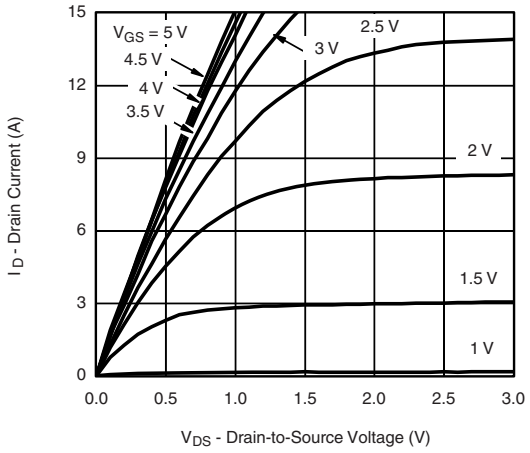


Normalized Thermal Transient Impedance, Junction-to-Ambient

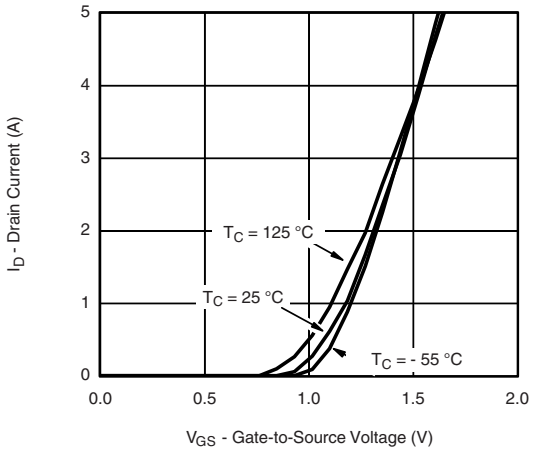


Normalized Thermal Transient Impedance, Junction-to-Case

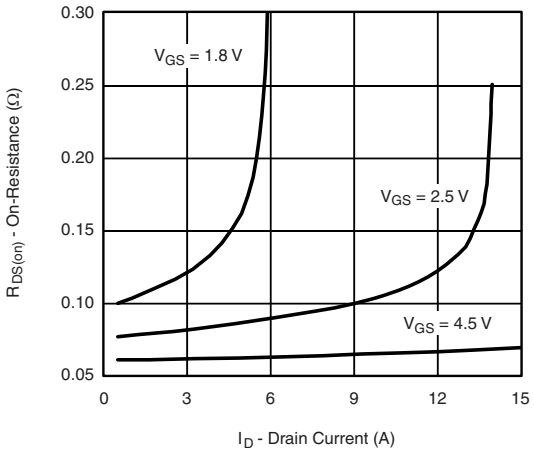
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



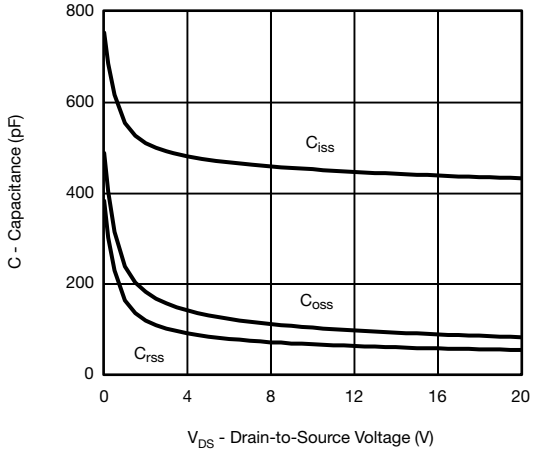
Output Characteristics



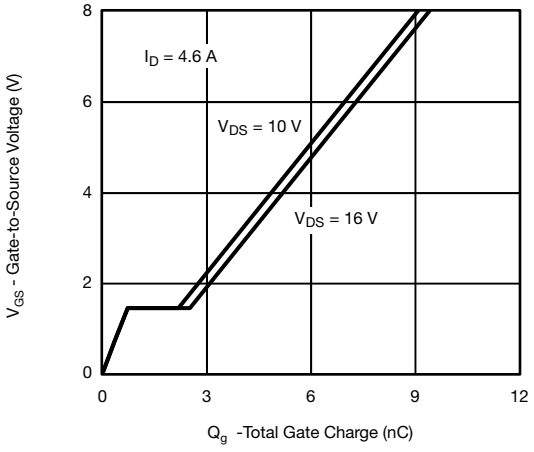
Transfer Characteristics



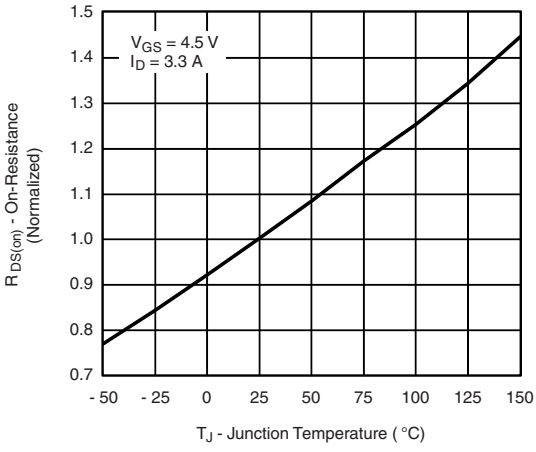
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

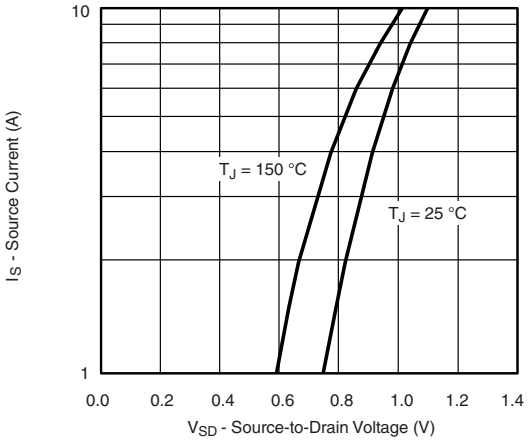


Gate Charge

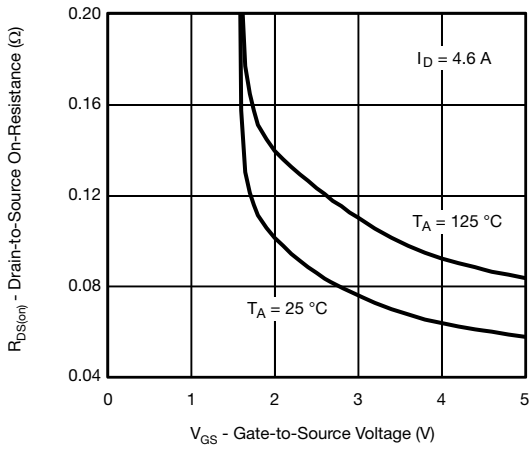


On-Resistance vs. Junction Temperature

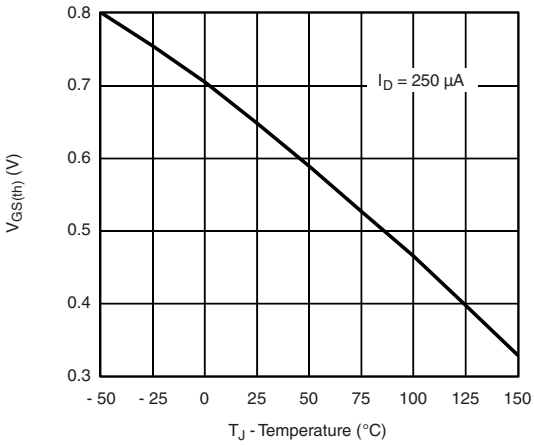
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



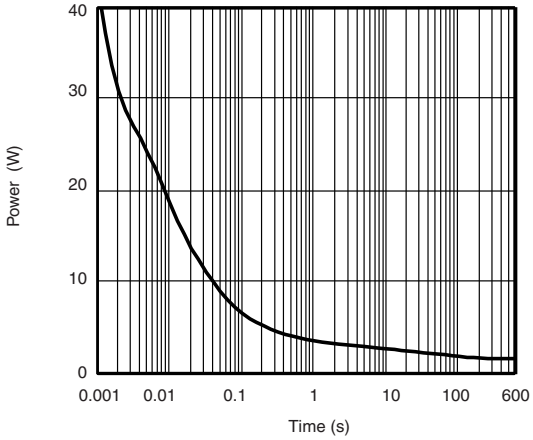
Source-Drain Diode Forward Voltage



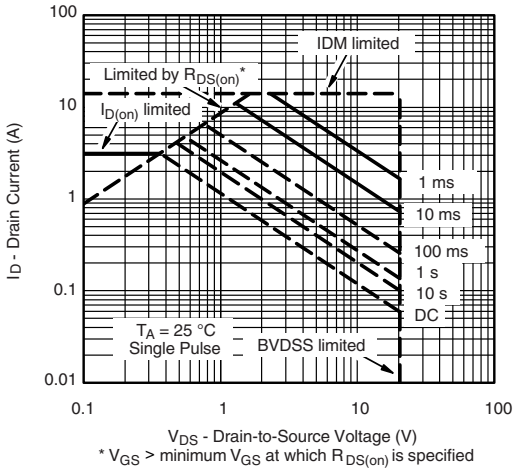
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

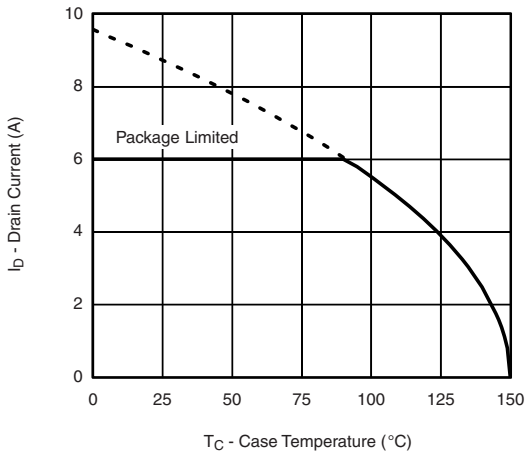


Single Pulse Power, Junction-to-Ambient

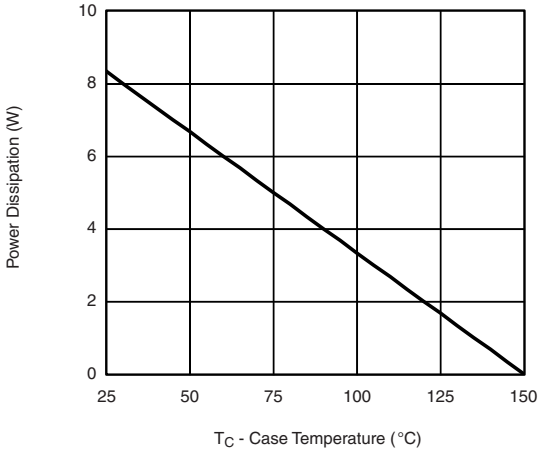


Safe Operating Area, Junction-to-Case

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

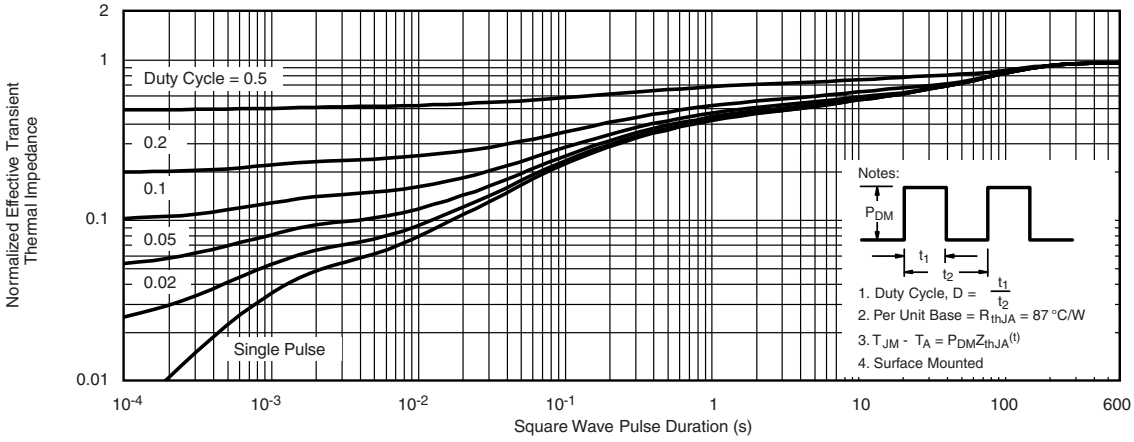


Power Derating

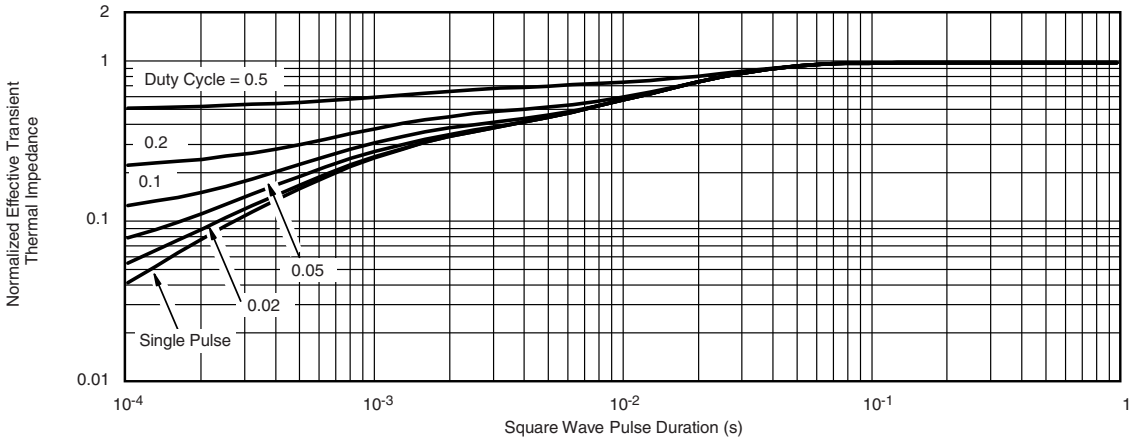
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



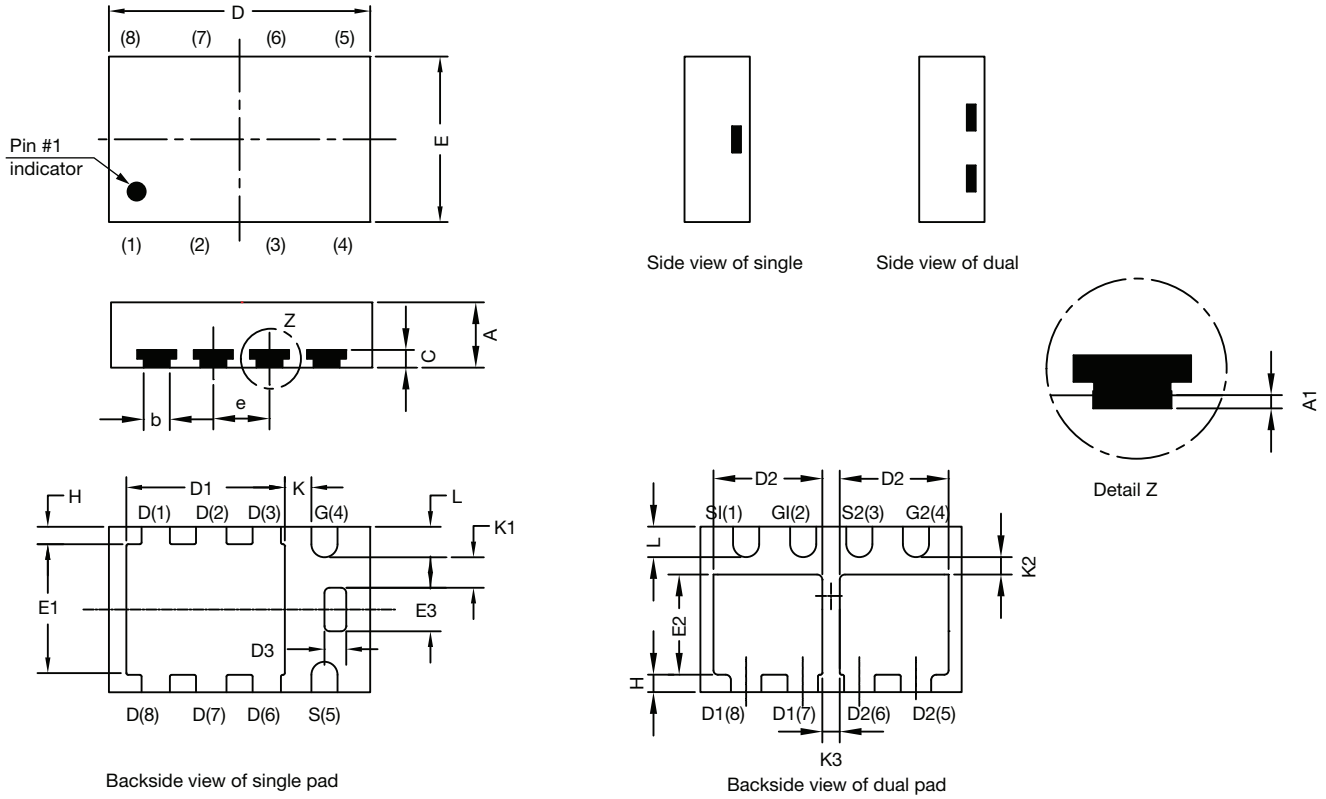
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73529.

PowerPAK® ChipFET® Case Outline

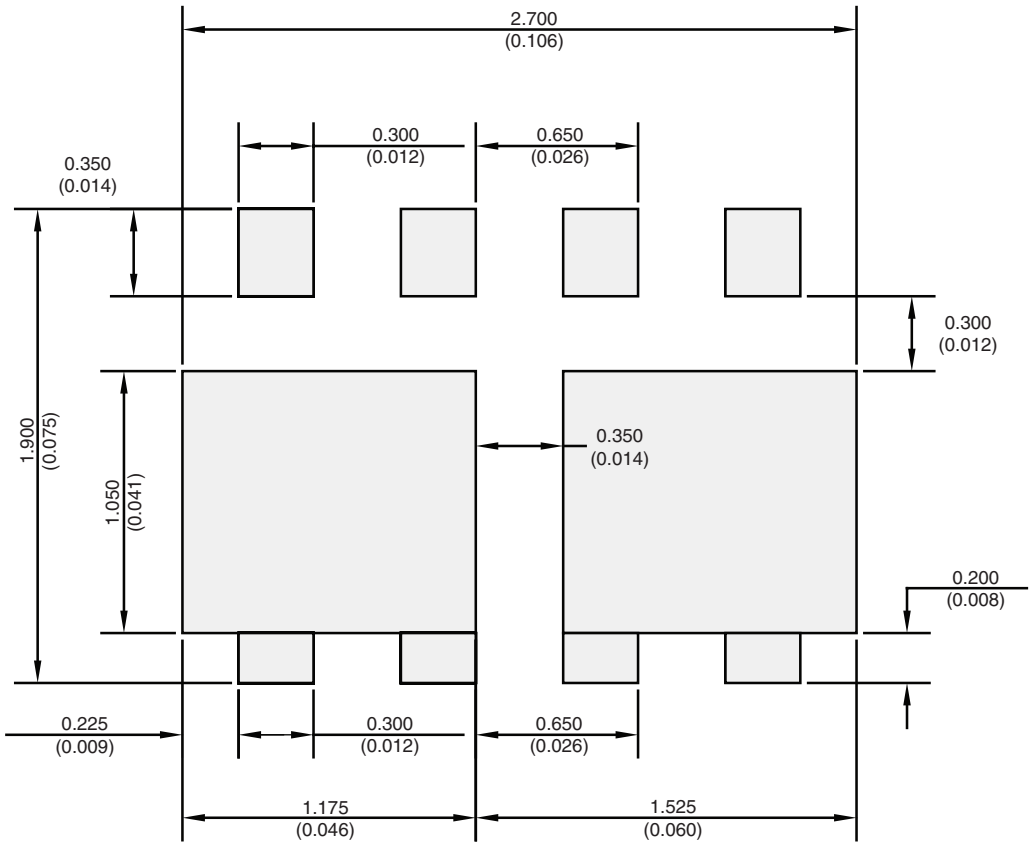


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14 DWG: 5940						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner

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