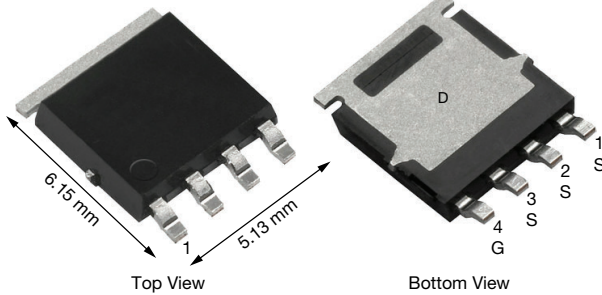


## N-Channel 40 V (D-S) 150 °C MOSFET

PowerPAK® SO-8L Single



PRODUCT SUMMARY	
$V_{DS}$ (V)	40
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00265
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.00360
$Q_g$ typ. (nC)	23
$I_D$ (A) <sup>a</sup>	109
Configuration	Single

### FEATURES

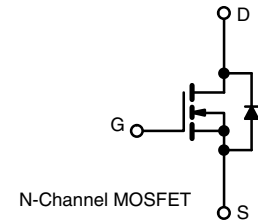
- TrenchFET® Gen IV power MOSFET
- Tuned for the lowest  $R_{DS}-Q_{oss}$  FOM
- 100 %  $R_g$  and UIS tested
- $Q_{gd}/Q_{gs}$  ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- DC/AC inverters



ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SiJA58DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	40	V
Gate-source voltage		$V_{GS}$	+20 / -16	V
Continuous drain current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	109	A
	$T_C = 70$ °C		87.3	
	$T_A = 25$ °C		29.3 <sup>b</sup>	
	$T_A = 70$ °C		23.3 <sup>b</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)		$I_{DM}$	150	A
Continuous source-drain diode current	$T_C = 25$ °C	$I_S$	51.6	A
	$T_A = 25$ °C		3.7 <sup>b, c</sup>	
Single pulse avalanche current	L = 0.1 mH	$I_{AS}$	30	mJ
Single pulse avalanche energy		$E_{AS}$	45	
Maximum power dissipation	$T_C = 25$ °C	$P_D$	56.8	W
	$T_C = 70$ °C		36.3	
	$T_A = 25$ °C		4.1 <sup>b</sup>	
	$T_A = 70$ °C		2.6 <sup>b</sup>	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c</sup>			260	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	t < 10 s	$R_{thJA}$	25	30	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	1.7	2.2	

### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W



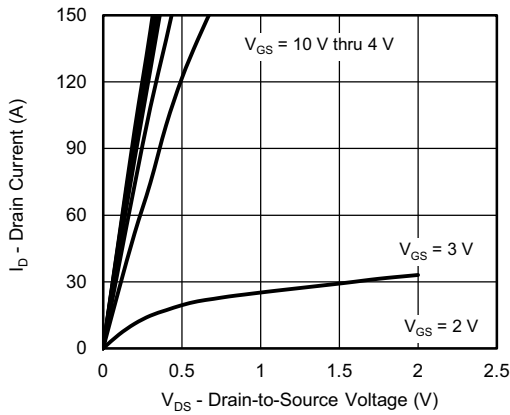
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	24	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-5.5	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.1	-	2.4	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20 / -16 V	-	-	100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 10 V	30	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	-	0.00220	0.00265	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	-	0.00300	0.00360	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A	-	125	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	3750	-	pF
Output capacitance	C <sub>OSS</sub>		-	560	-	
Reverse transfer capacitance	C <sub>RSS</sub>		-	72	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	50	75	nC
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	-	23	35	
Gate-source charge	Q <sub>gs</sub>		-	10.3	-	
Gate-drain charge	Q <sub>gd</sub>		-	4.3	-	
Output charge	Q <sub>OSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	-	24	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.5	1.2	2.4	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	10	20	ns
Rise time	t <sub>r</sub>		-	19	38	
Turn-off delay time	t <sub>d(off)</sub>		-	28	56	
Fall time	t <sub>f</sub>		-	8	16	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	22	44	
Rise time	t <sub>r</sub>		-	52	100	
Turn-off delay time	t <sub>d(off)</sub>		-	23	46	
Fall time	t <sub>f</sub>		-	10	20	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	51.6	A
Pulse diode forward current	I <sub>SM</sub>		-	-	150	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.73	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	38	76	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	33	66	nC
Reverse recovery fall time	t <sub>a</sub>		-	20	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	18	-	

**Notes**

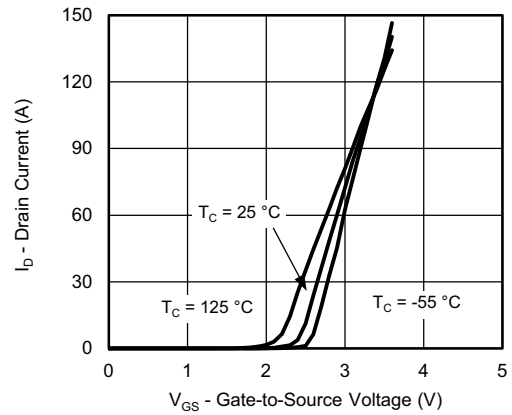
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

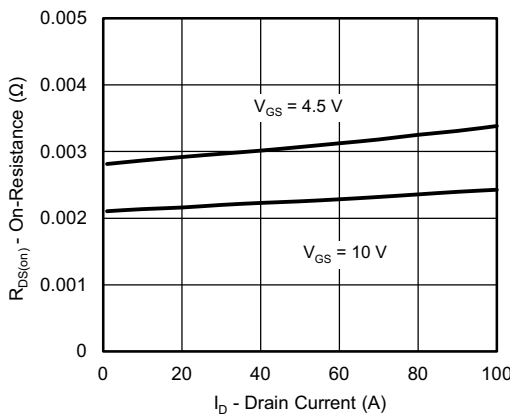
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



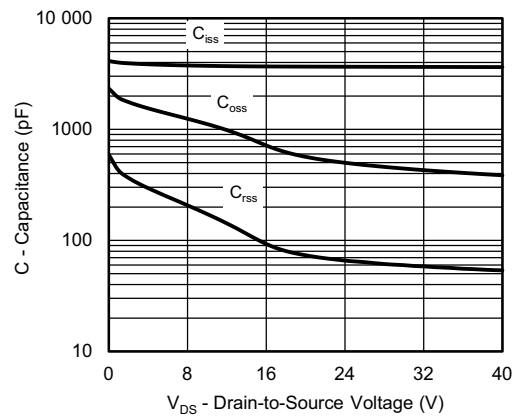
**Output Characteristics**



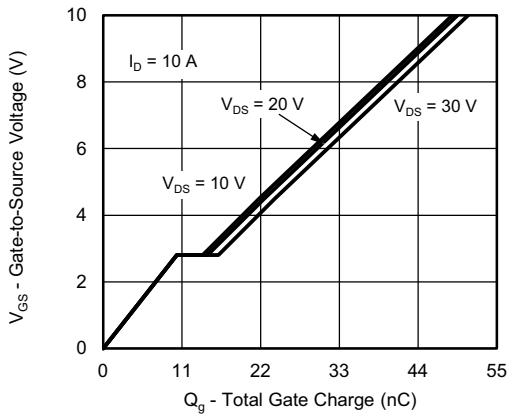
**Transfer Characteristics**



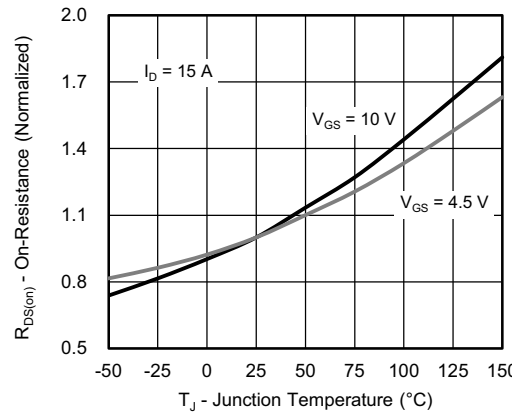
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



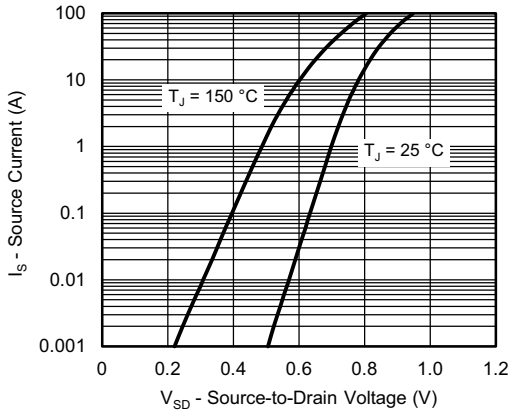
**Gate Charge**



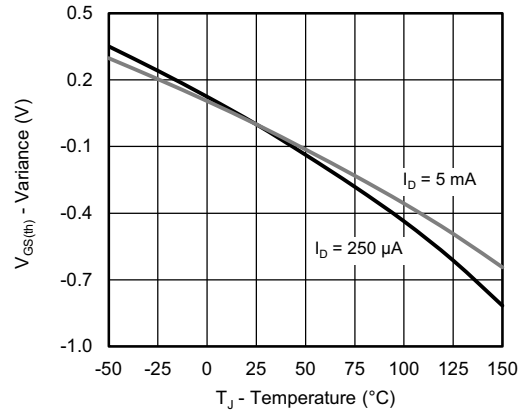
**On-Resistance vs. Junction Temperature**



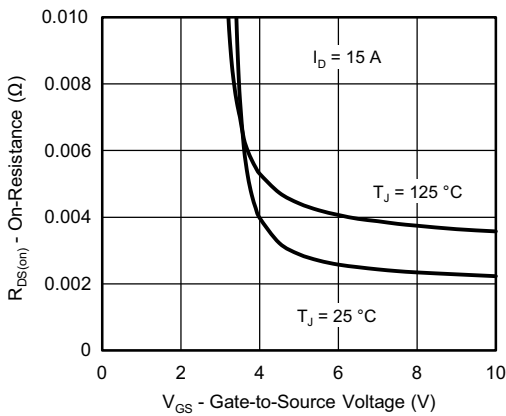
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



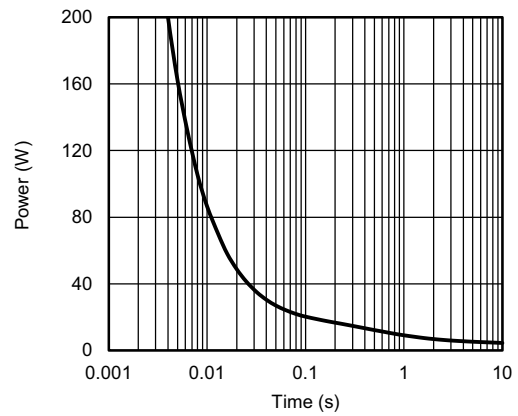
Source-Drain Diode Forward Voltage



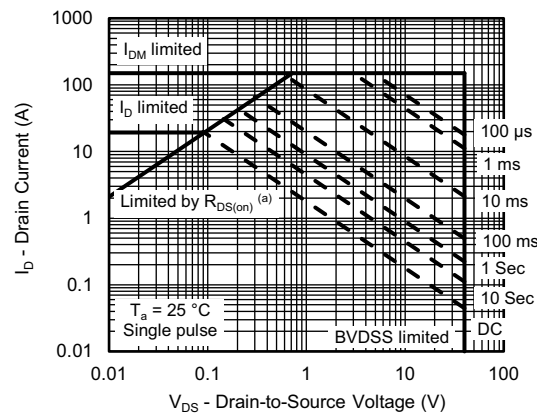
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

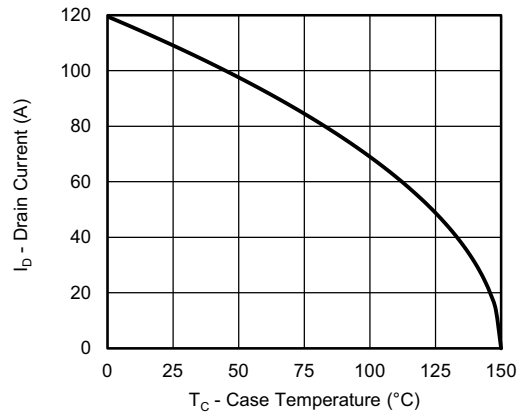


Safe Operating Area, Junction-to-Ambient

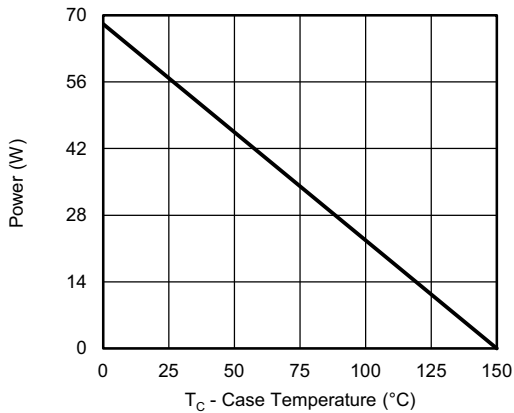
Note

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

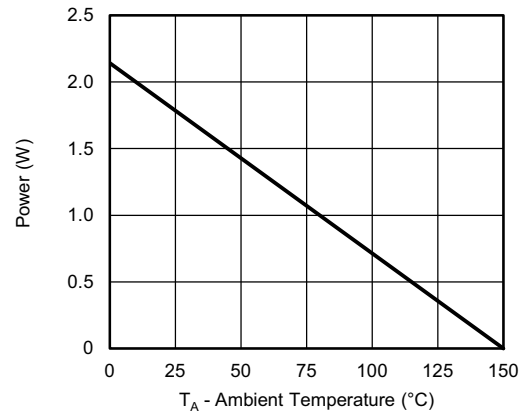
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



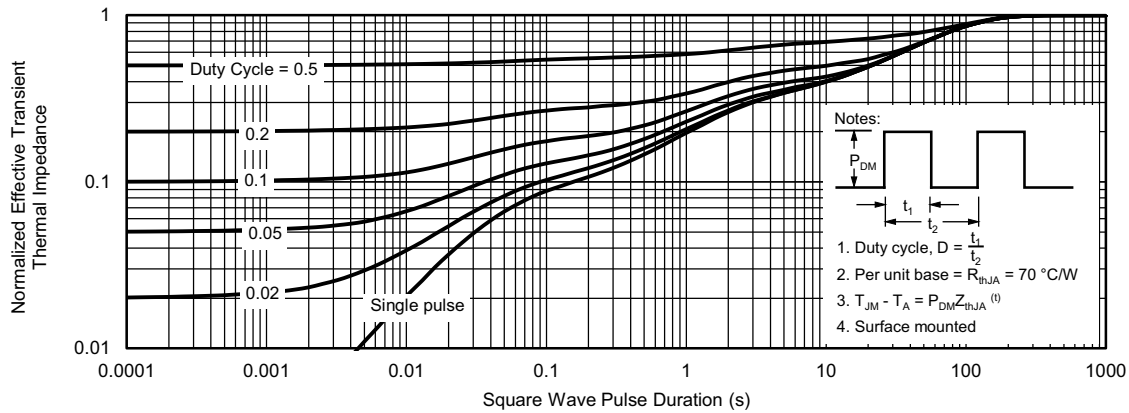
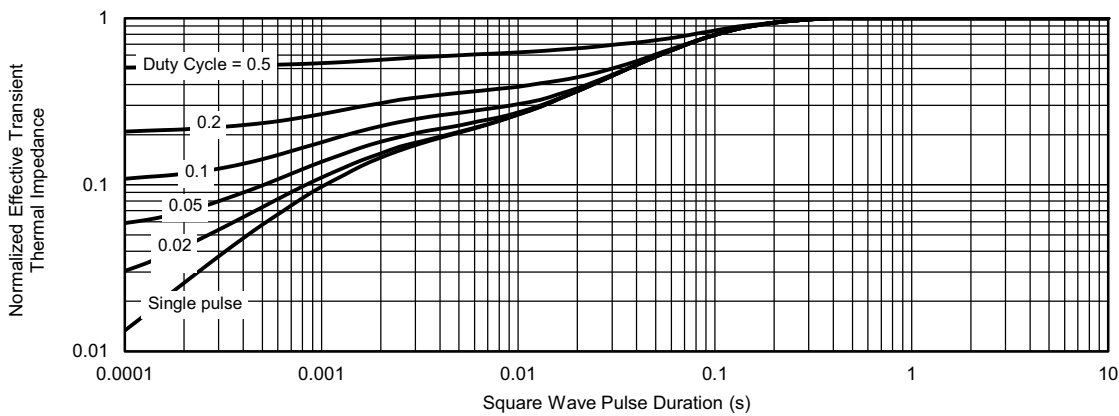
**Power, Junction-to-Case**



**Power, Junction-to-Ambient**

### Note

- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**

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# PowerPAK<sup>®</sup> SO-8L Case Outline 1



Topside view



Backside view (single)



Backside view (dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°

ECN: S19-0643-Rev. E, 05-Aug-2019  
DWG: 5976

Note

- Millimeters will govern





## RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads  
Dimensions in mm (inches)



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