


THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	600	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$	-	0.67	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.5	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 2.2\text{ A}^b$	-	-	2.2	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 2.2\text{ A}$	2.1	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	510	-	pF	
Output Capacitance	C_{oss}		-	70	-		
Reverse Transfer Capacitance	C_{rss}		-	3.5	-		
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	730	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	19	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 3.6\text{ A}, V_{DS} = 480\text{ V}$, see fig. 6 and 13 ^b	-	-	23	nC
Gate-Source Charge	Q_{gs}			-	-	5.4	
Gate-Drain Charge	Q_{gd}			-	-	11	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 3.6\text{ A}, R_g = 12\text{ }\Omega, R_D = 82\text{ }\Omega$, see fig. 10 ^{b, d}	-	9.8	-	ns	
Rise Time	t_r		-	13	-		
Turn-Off Delay Time	$t_{d(off)}$		-	19	-		
Fall Time	t_f		-	12	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.6	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	14		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 3.6\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 3.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	400	600	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.1	1.7	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .
- Uses IRFBC30A/SiHFBC30A data and test conditions.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

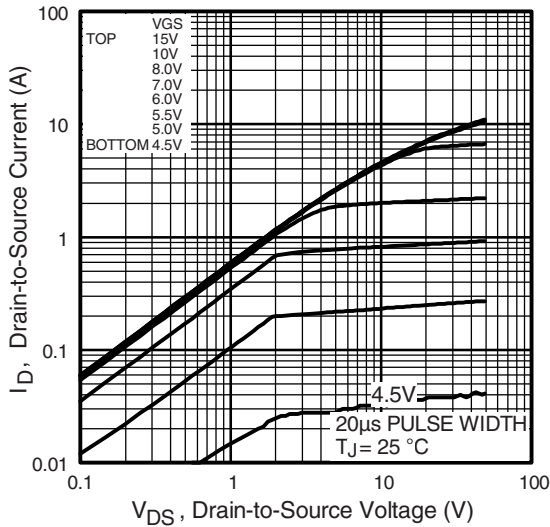


Fig. 1 - Typical Output Characteristics

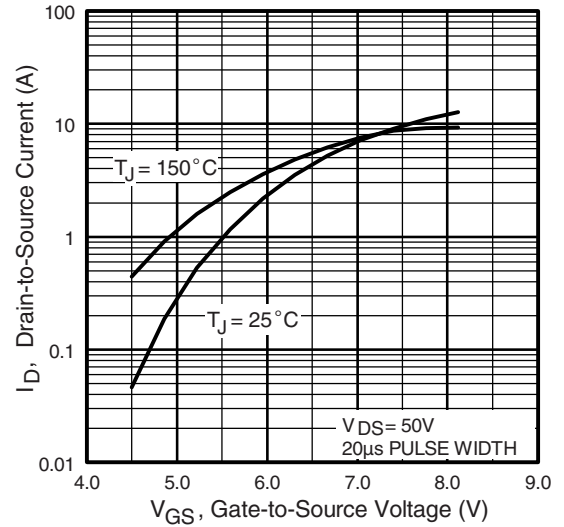


Fig. 3 - Typical Transfer Characteristics

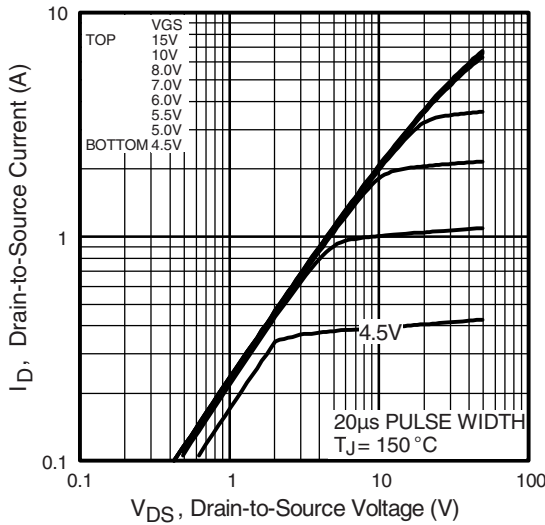


Fig. 2 - Typical Output Characteristics

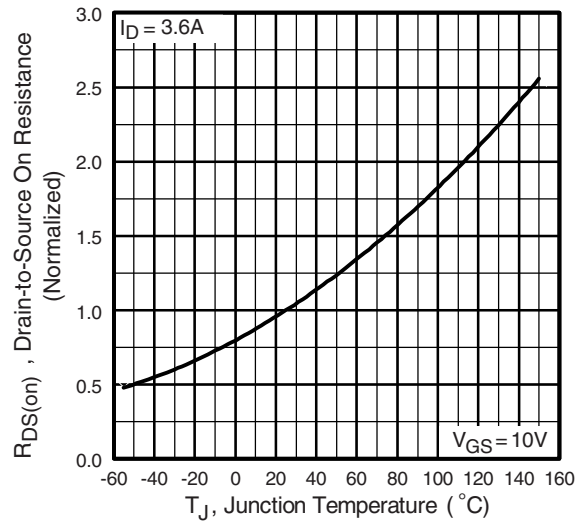
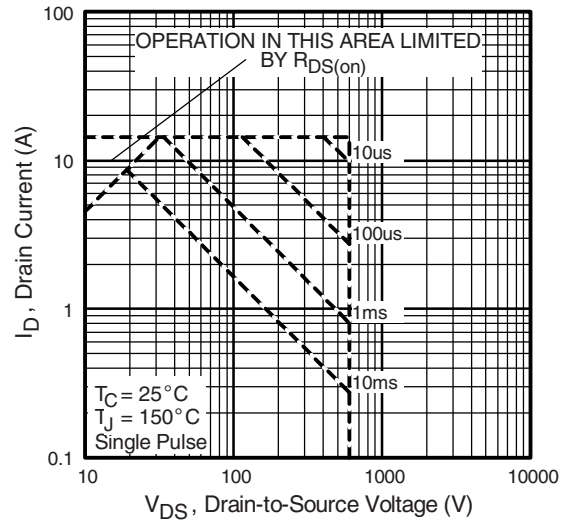
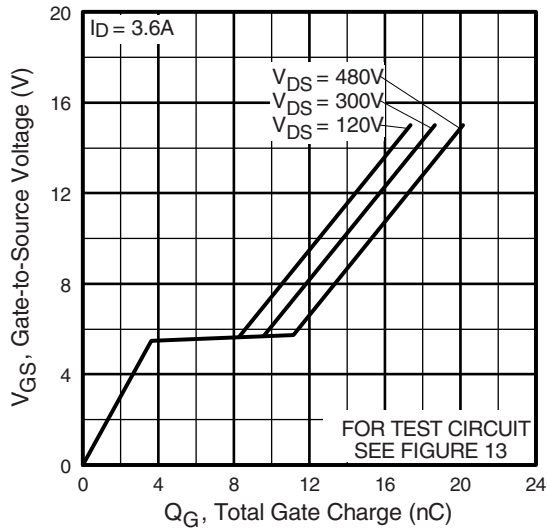
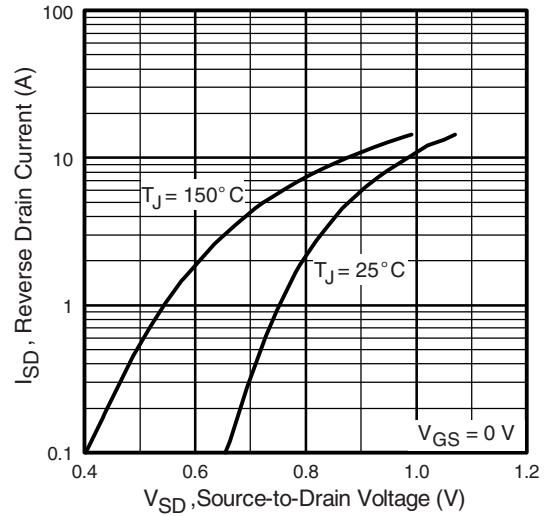
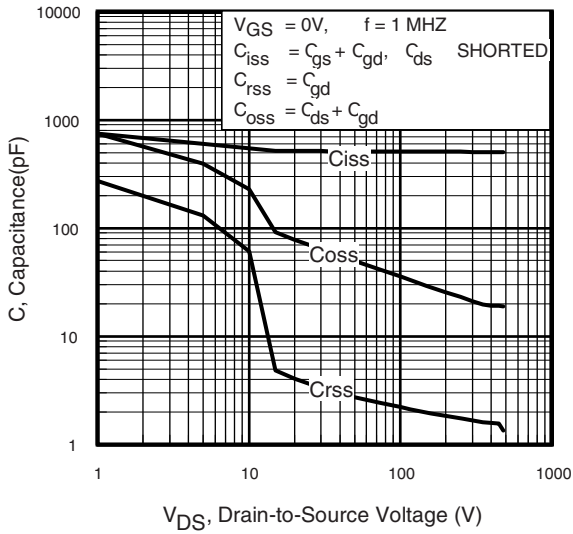


Fig. 4 - Normalized On-Resistance vs. Temperature



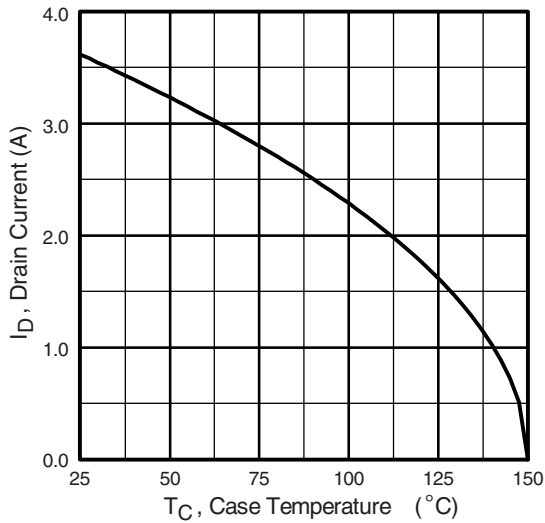


Fig. 9 - Maximum Drain Current vs. Case Temperature

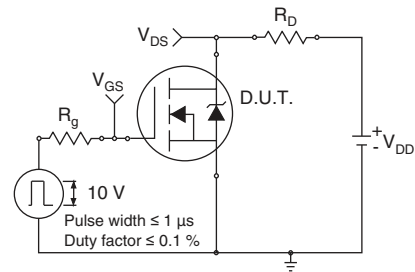


Fig. 10a - Switching Time Test Circuit

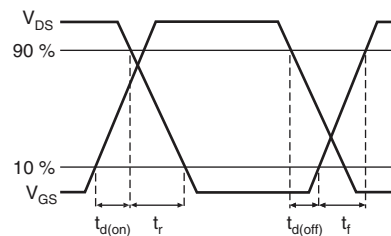


Fig. 10b - Switching Time Waveforms

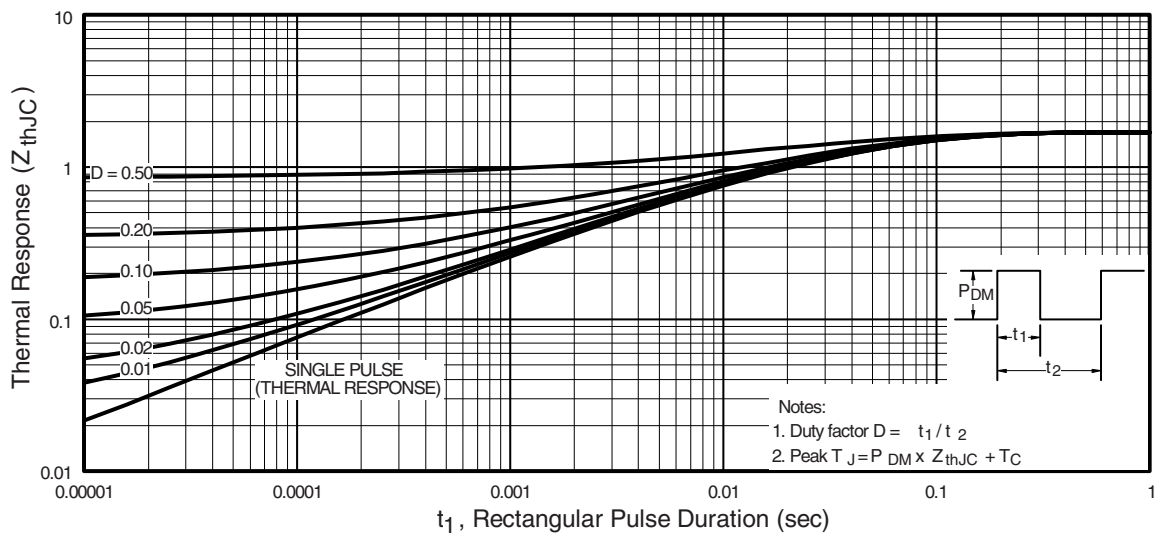


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

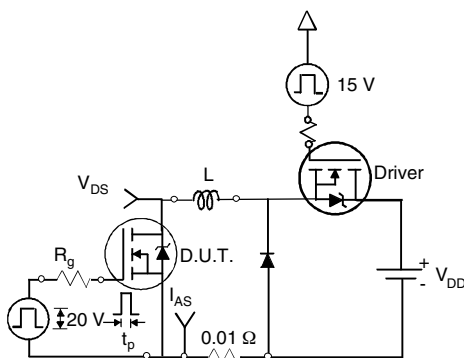


Fig. 12a - Unclamped Inductive Test Circuit

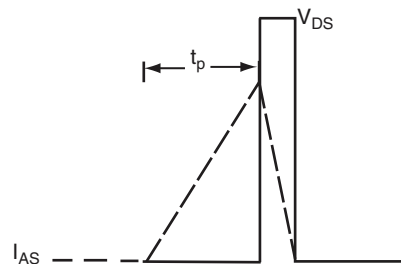


Fig. 12b - Unclamped Inductive Waveforms

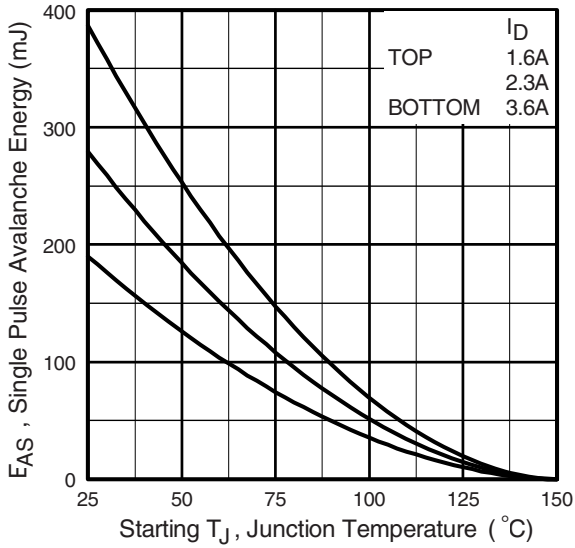


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

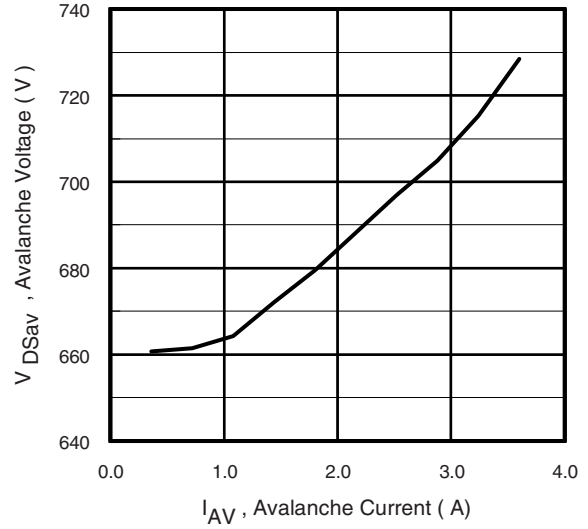


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

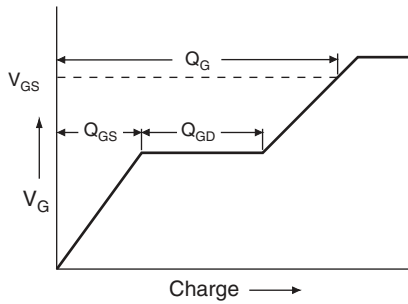


Fig. 13a - Basic Gate Charge Waveform

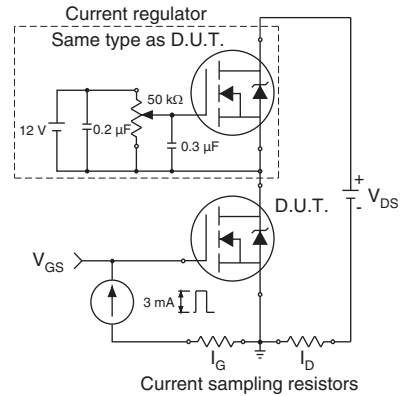
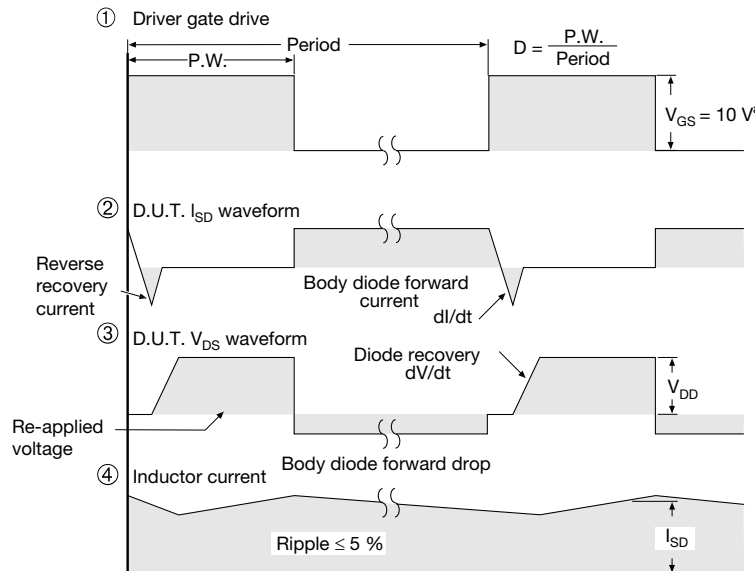


Fig. 13b - Gate Charge Test Circuit



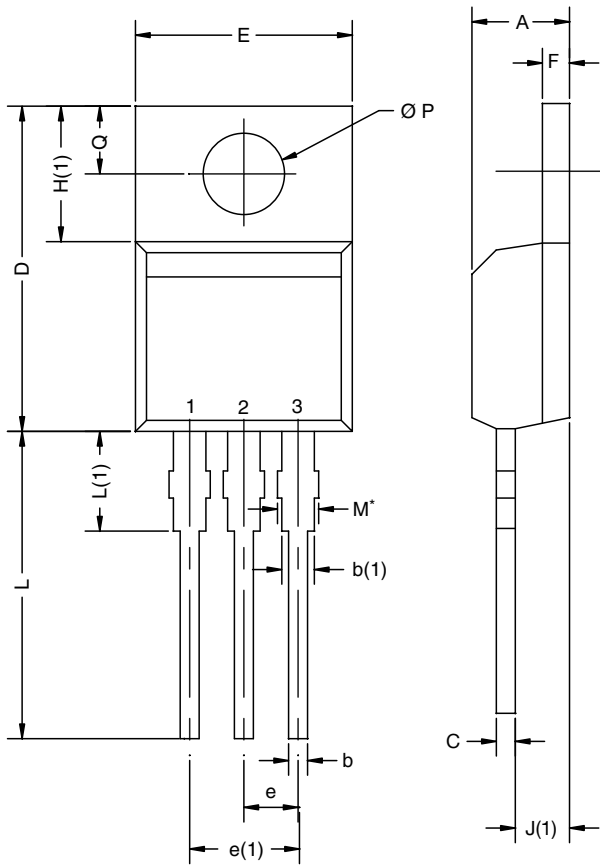
Note
 a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-220AB

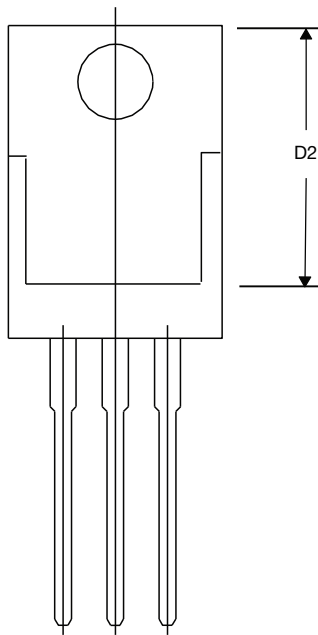


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

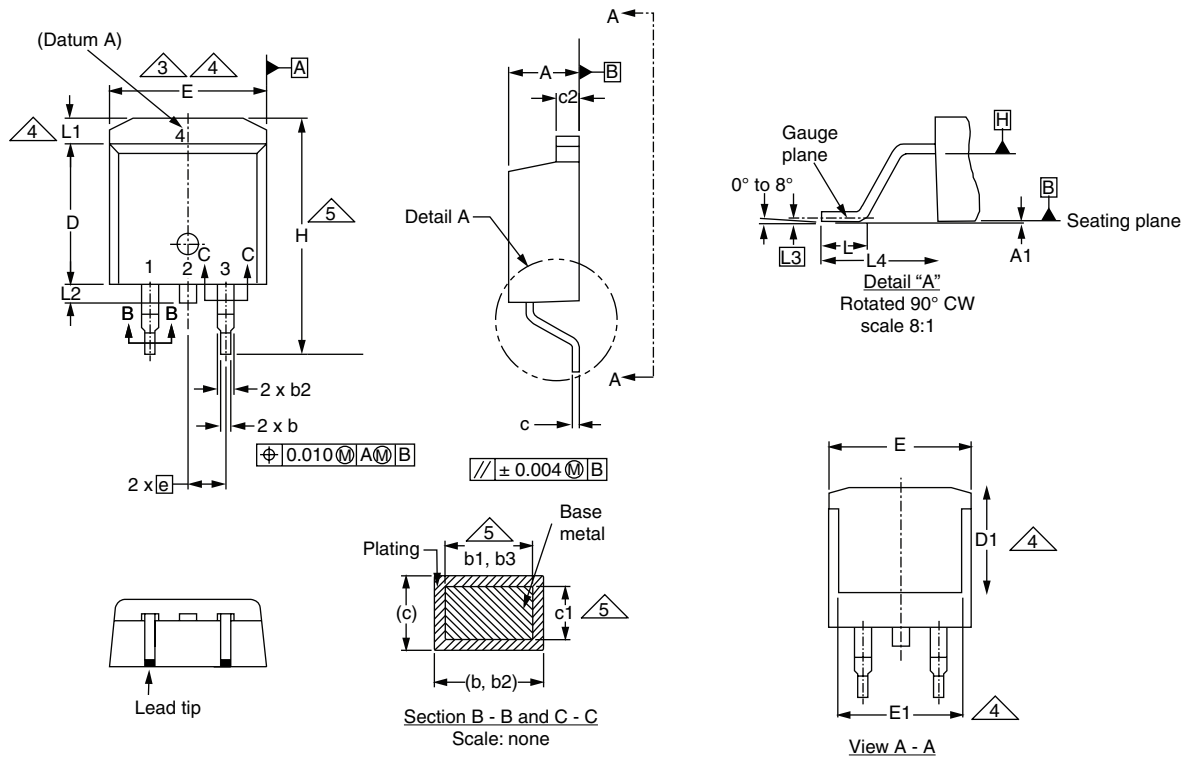
ECN: T14-0413-Rev. P, 16-Jun-14
DWG: 5471

Note

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM



TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

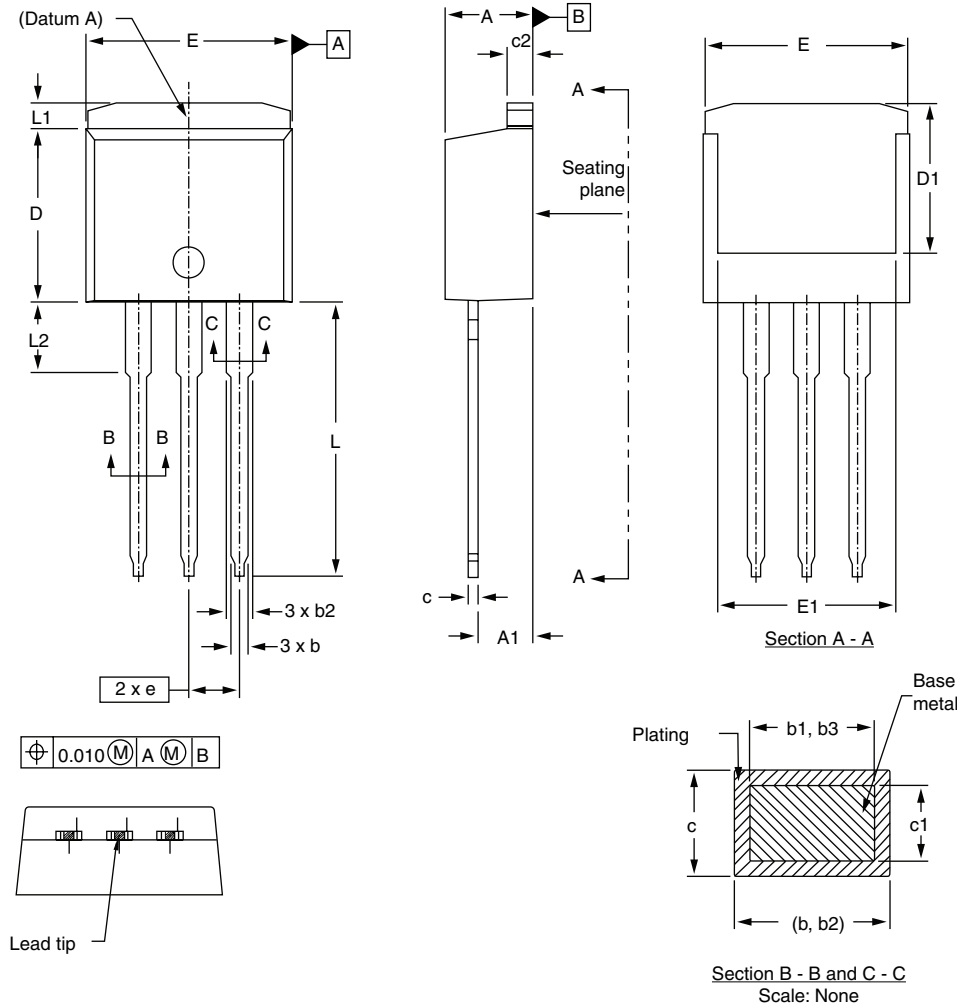
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

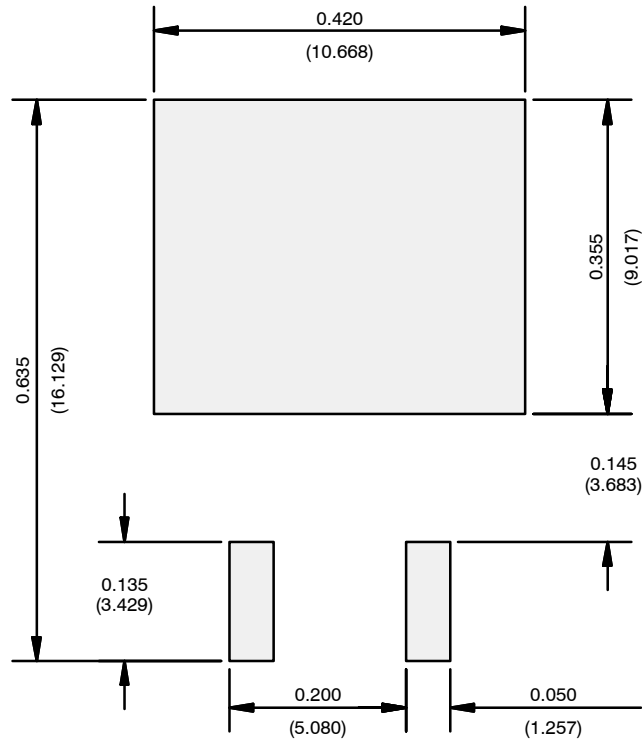
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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