

## S Series Power MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

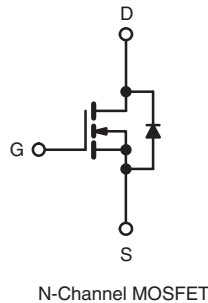
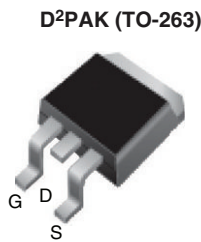
PRODUCT SUMMARY		
$V_{DS}$ at $T_J$ max. (V)	650	
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.190
$Q_g$ max. (nC)	98	
$Q_{gs}$ (nC)	17	
$Q_{gd}$ (nC)	25	
Configuration	Single	

### FEATURES

- Generation one
- High  $E_{AR}$  capability
- Lower figure-of-merit  $R_{on} \times Q_g$
- 100 % avalanche tested
- Ultra low  $R_{on}$
- $dV/dt$  ruggedness
- Ultra low gate charge ( $Q_g$ )
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### APPLICATIONS

- PFC power supply stages
- Hard switching topologies
- Solar inverters
- UPS
- Motor control
- Lighting
- Server telecom



N-Channel MOSFET

ORDERING INFORMATION	
Package	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHB22N60S-GE3
Lead (Pb)-free	SiHB22N60S-E3


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	600	V
Gate-Source Voltage			$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	$I_D$	22	A
		$T_C = 100$ °C		13	
Pulsed Drain Current <sup>a</sup>			$I_{DM}$	65	
Linear Derating Factor	D <sup>2</sup> PAK (TO-263)			2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			$E_{AS}$	690	mJ
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	25	
Maximum Power Dissipation	D <sup>2</sup> PAK (TO-263)		$P_D$	250	W
Drain-Source Voltage Slope	$T_J = 125$ °C		$dV/dt$	37	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>				5.3	
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	-55 to +150	°C
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s			300	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.



THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	D <sup>2</sup> PAK (TO-263)	R <sub>thJA</sub>	-	62	°C/W	
Maximum Junction-to-Case (Drain)	D <sup>2</sup> PAK (TO-263)	R <sub>thJC</sub>	-	0.5		

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	100	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 11 A	-	0.160	0.190	Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 13 A		-	9.4	-	S
<b>Dynamic</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz		-	2810	-	pF
Output Capacitance	C <sub>oss</sub>			-	1480	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	33	-	
Effective Output Capacitance (Time Related)	C <sub>oss eff. (TR)</sub> <sup>a</sup>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 0 V to 480 V	-	155	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 22 A, V <sub>DS</sub> = 480 V	-	75	110	nC
Gate-Source Charge	Q <sub>gs</sub>			-	17	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	25	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 380 V, I <sub>D</sub> = 22 A, R <sub>g</sub> = 9.1 Ω, V <sub>GS</sub> = 10 V		-	24	50	ns
Rise Time	t <sub>r</sub>			-	68	100	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	77	115	
Fall Time	t <sub>f</sub>			-	59	90	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	0.65	-	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	22	A
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	88	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 22 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> , di/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	462	690	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	8.3	16	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	30	60	A

**Note**

a. C<sub>oss eff. (TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DS</sub>.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

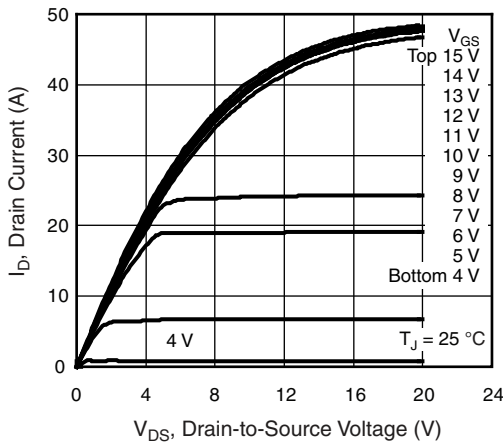


Fig. 1 - Typical Output Characteristics,  $T_J = 25\text{ }^\circ\text{C}$

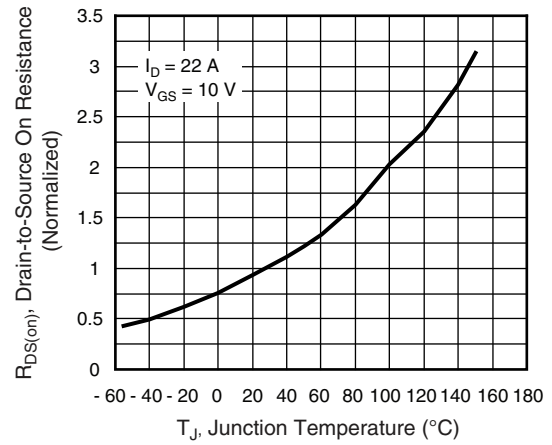


Fig. 4 - Normalized On-Resistance vs. Temperature

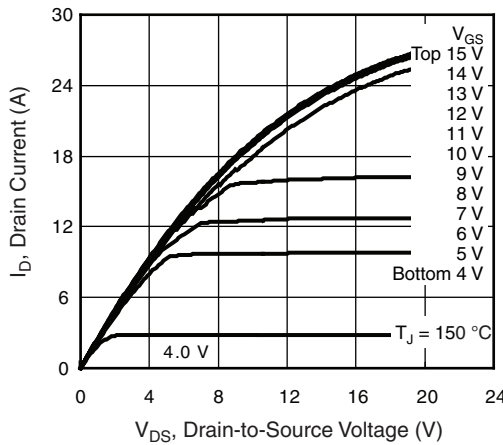


Fig. 2 - Typical Output Characteristics,  $T_J = 150\text{ }^\circ\text{C}$

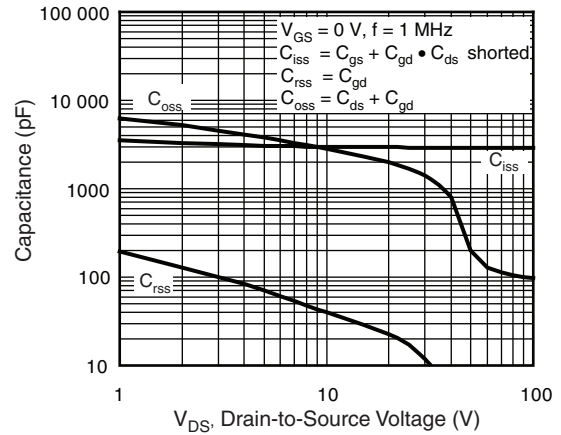


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

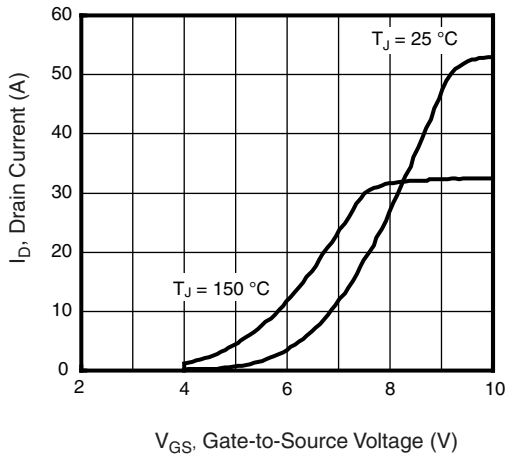


Fig. 3 - Typical Transfer Characteristics

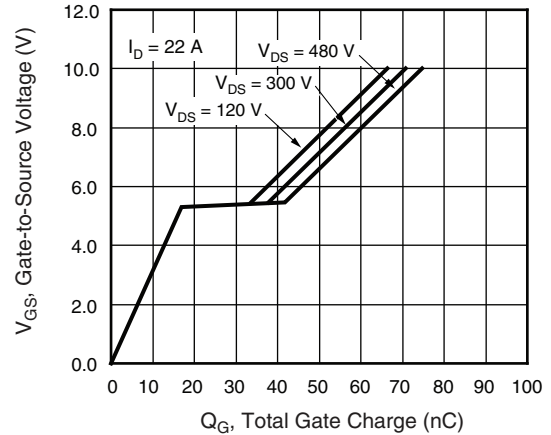


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

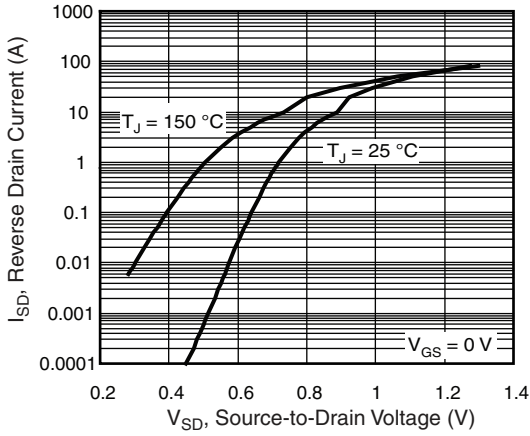


Fig. 7 - Typical Source-Drain Diode Forward Voltage

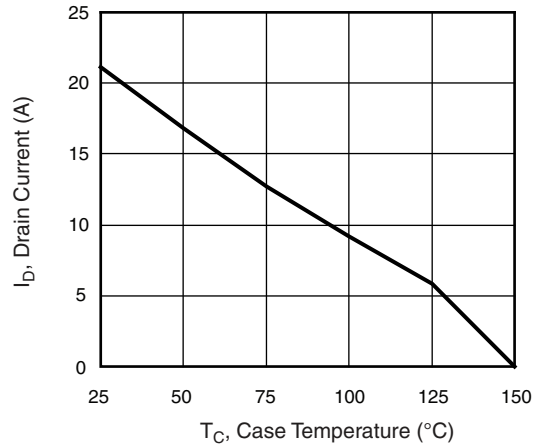


Fig. 9 - Maximum Drain Current vs. Case Temperature

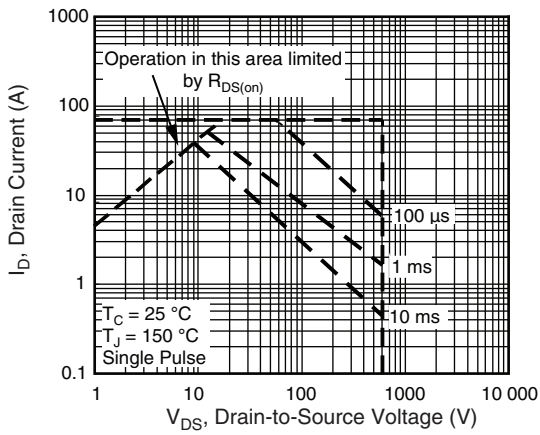


Fig. 8 - Maximum Safe Operating Area

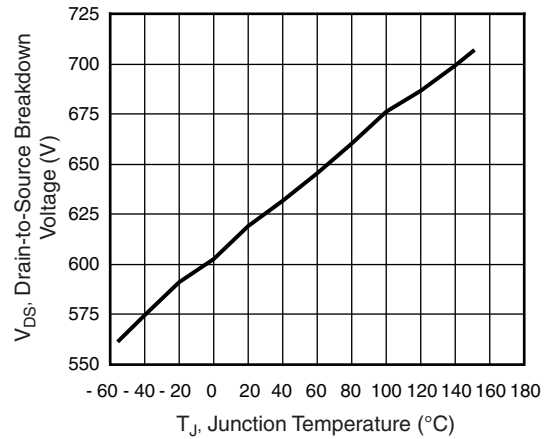


Fig. 10 - Drain-to-Source Breakdown Voltage

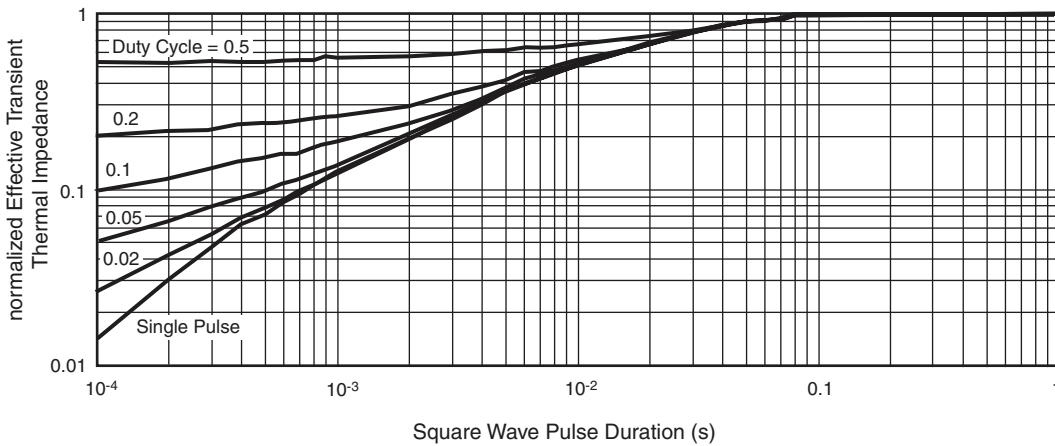


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

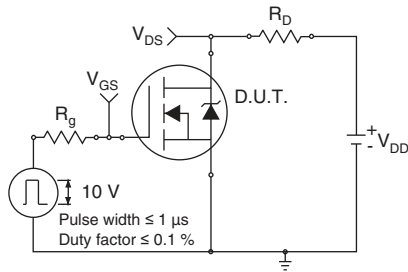


Fig. 12 - Switching Time Test Circuit

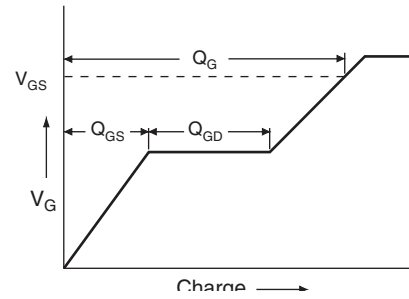


Fig. 16 - Basic Gate Charge Waveform

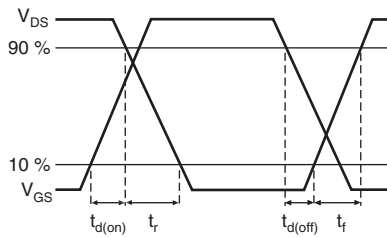


Fig. 13 - Switching Time Waveforms

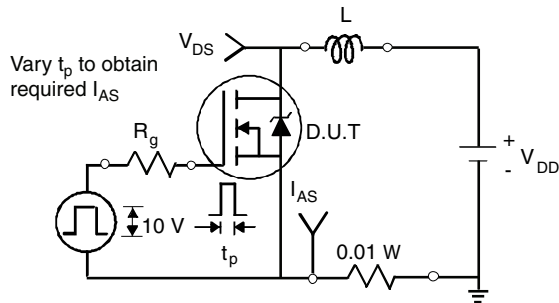


Fig. 14 - Unclamped Inductive Test Circuit

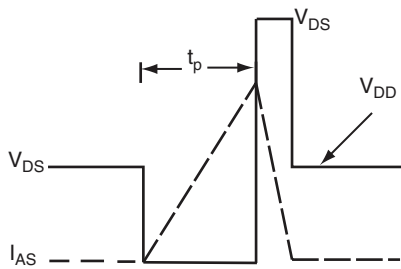


Fig. 15 - Unclamped Inductive Waveforms

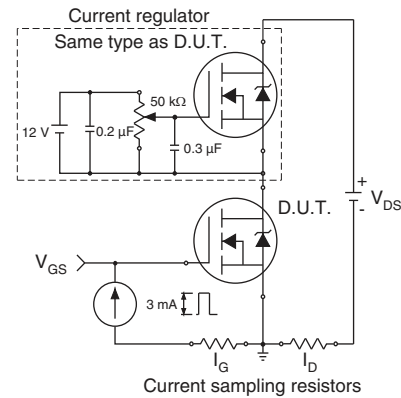
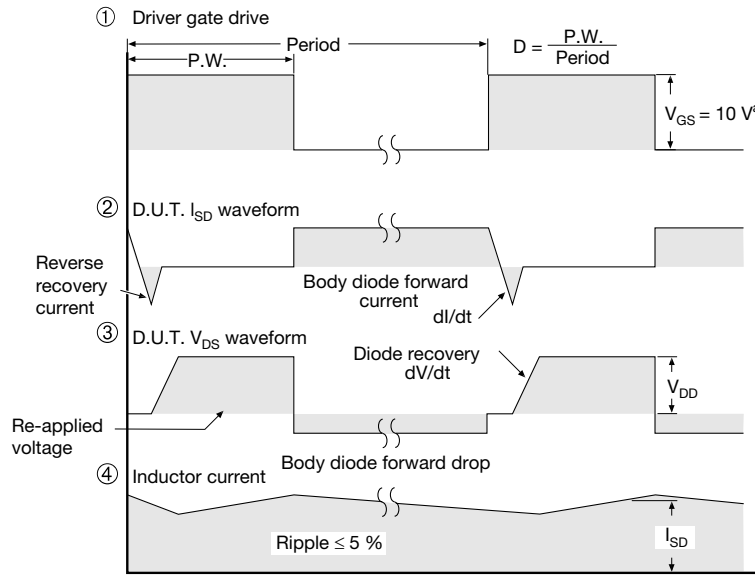
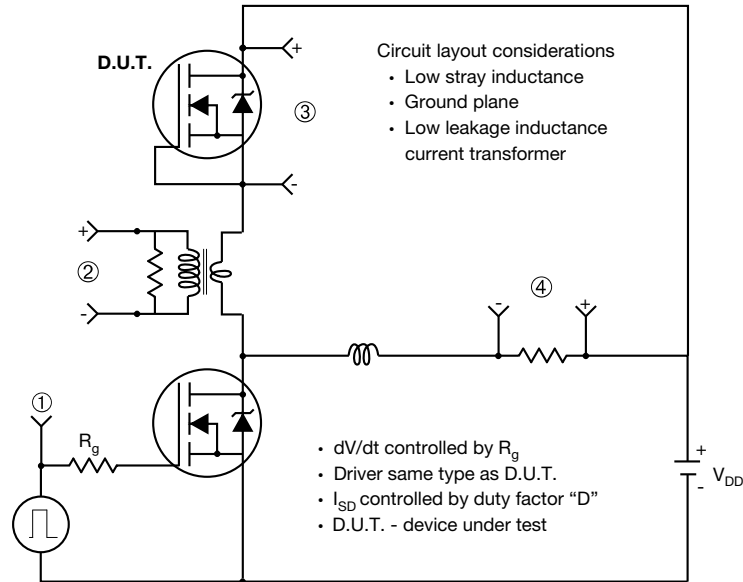


Fig. 17 - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 18 - For N-Channel**

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