



Dual P-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)	
	0.110 at V _{GS} = - 4.5 V	- 3.6		
- 20	0.160 at V _{GS} = - 2.5 V	- 3.0	5.1	
	0.240 at V _{GS} = - 1.8 V	- 2.4		

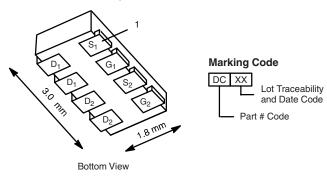
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs: 1.8 V Rated
- · Compliant to RoHS Directive 2002/95/EC



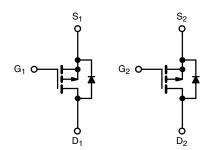


1206-8 ChipFET®



Ordering Information: Si5933DC-T1-E3 (Lead (Pb)-free)

Si5933DC-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$T_A = 25 ^{\circ}C$, unles	ss otherwise r	noted		
Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 20		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	- I _D	- 3.6	- 2.7	
Continuous Diain Curient (1) = 150 °C)	T _A = 85 °C		- 2.6	- 1.9	Α
Pulsed Drain Current		I _{DM}	- 10		A
Continuous Source Current (Diode Conduction) ^a		I _S	- 1.8	- 0.9	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2.1	1.1	W
Maximum Fower Dissipation	T _A = 85 °C		1.1	0.6	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 5 s	R _{thJA}	50	60	°C/W
Maximum Junction-to-Ambient	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	30	40	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. See reliability manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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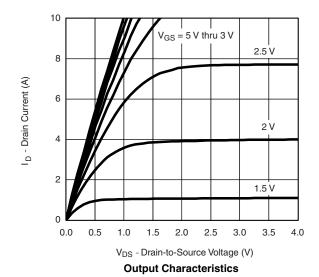
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.45		- 1.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μΑ	
		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 10			Α	
Drain-Source On-State Resistance ^a		V _{GS} = - 4.5 V, I _D = - 2.7 A		0.095	0.110		
	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 2.2 A		0.137	0.160	Ω	
		V _{GS} = - 1.8 V, I _D = - 1 A		0.205	0.240		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 2.7 A		7		S	
Diode Forward Voltage ^a	V_{SD}	I _S = - 0.9 A, V _{GS} = 0 V		- 0.8	- 1.2	V	
Dynamic ^b							
Total Gate Charge	Q_g			5.1	7.7	nC	
Gate-Source Charge	Q_{gs}	Q_{gs} $V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -2.7 \text{ A}$		1.2			
Gate-Drain Charge	Q_{gd}			1.0			
Turn-On Delay Time	t _{d(on)}			16	25		
Rise Time	t _r	t_r $V_{DD} = -10 \text{ V}, R_L = 10 \Omega$		30	45	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -1$ Å, $V_{GEN} = -4.5$ V, $R_g = 6 \Omega$		30	45		
Fall Time	t _f			27	40		
Source-Drain Reverse Recovery Time	t _{rr}	I _E = - 0.9 A, dI/dt = 100 A/μs		20	40		

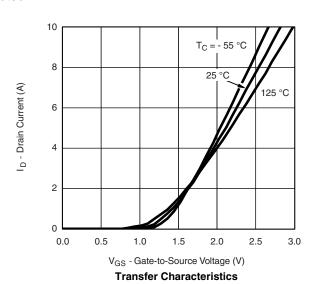
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

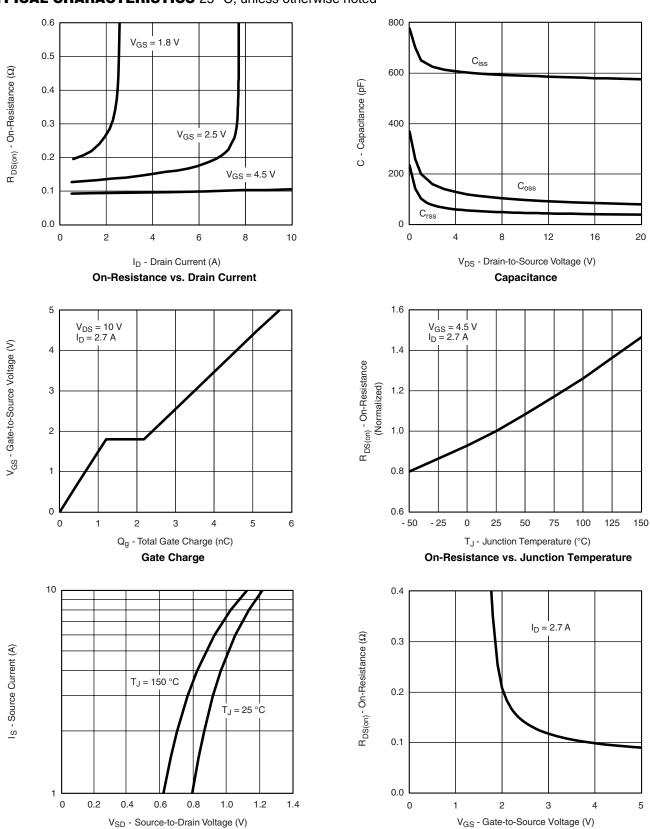








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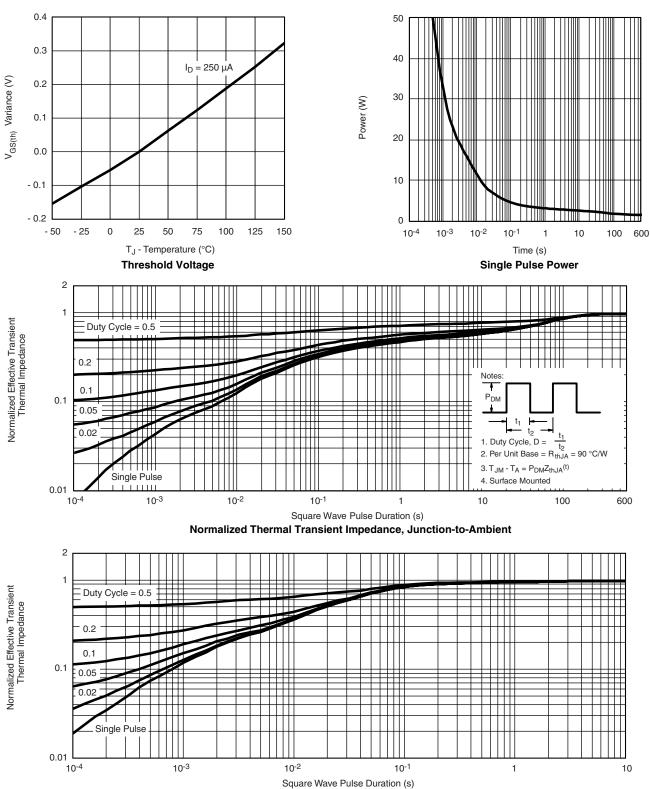
Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71238.



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