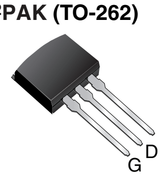
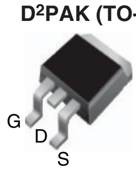
Power MOSFET

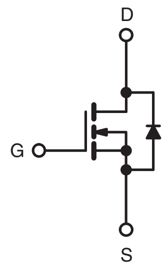
PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.050
Q_g (Max.) (nC)	46	
Q_{gs} (nC)	11	
Q_{gd} (nC)	22	
Configuration	Single	

I²PAK (TO-262)



D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- Advanced process technology
- Surface mount
- Low-profile through-hole (IRFZ34L, SiHFZ34L)
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available
HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2 W in a typical surface mount application.

The through-hole version (IRFZ34L, SiHFZ34L) is available for low-profile applications.

ORDERING INFORMATION			
Package	D²PAK (TO-263)	D²PAK (TO-263)	I²PAK (TO-262)
Lead (Pb)-free and halogen-free	SiHFZ34S-GE3	SiHFZ34STRL-GE3	SiHFZ34L-GE3
Lead (Pb)-free	IRFZ34SPbF	IRFZ34STRLPbF [a]	IRFZ34LPbF

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	60	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	30	A
		T_C = 100 °C		21	
Pulsed Drain Current [a, e]			I_{DM}	120	
Linear Derating Factor				0.59	W/°C
Single Pulse Avalanche Energy [b, e]			E_{AS}	200	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	88	W
	T_A = 25 °C			3.7	
Peak Diode Recovery dV/dt [c, e]			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) [d]	for 10 s			300	

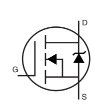
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, Starting T_J = 25 °C, L = 260 μH, R_g = 25 Ω, I_{AS} = 30 A (see fig. 12).
c. $I_{SD} \leq 30$ A, dI/dt ≤ 200 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
d. 1.6 mm from case.
e. Uses IRFZ34, SiHFZ34 data and test conditions.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient (PCB mount) [a]	R_{thJA}	-	40	°C / W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA [c]	-	0.065	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 18 A [b]	-	-	0.05	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 18 A [b]	9.3	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5[c]	-	1200	-	pF
Output Capacitance	C_{oss}		-	600	-	
Reverse Transfer Capacitance	C_{rss}		-	100	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 30 A, V_{DS} = 48 V, see fig. 6 and 13 [b, c]	-	-	46	nC
Gate-Source Charge	Q_{gs}		-	-	11	
Gate-Drain Charge	Q_{gd}		-	-	22	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 30 A, R_g = 12 Ω, R_D = 1.0 Ω, see fig. 10 [b, c]	-	13	-	ns
Rise Time	t_r		-	100	-	
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	
Fall Time	t_f		-	52	-	
Internal Source Inductance	L_S	Between lead, and center of die contact	-	7.5	-	nH
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	30	A
Pulsed Diode Forward Current [a]	I_{SM}		-	-	120	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 30 A, V_{GS} = 0 V [b]	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 30 A, dI/dt = 100 A/μs [b, c]	-	120	230	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	700	1400	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
c. Uses IRFZ34, SiHFZ34 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

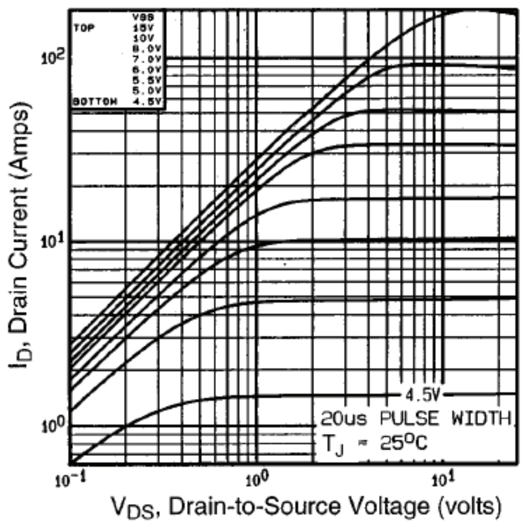


Fig. 1 - Typical Output Characteristics

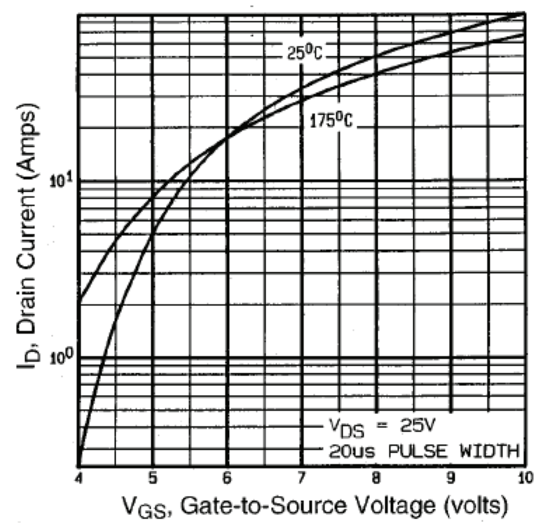


Fig. 3 - Typical Transfer Characteristics

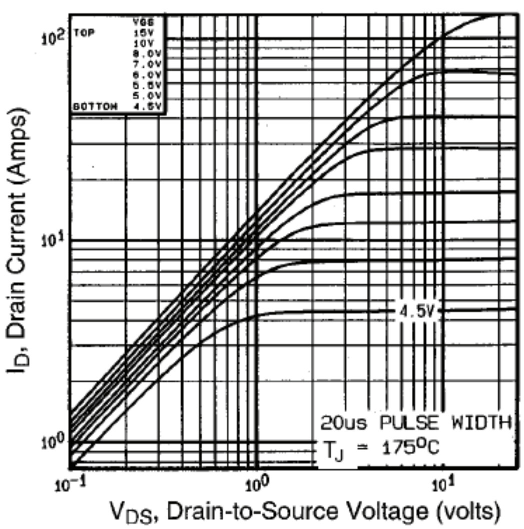


Fig. 2 - Typical Output Characteristics

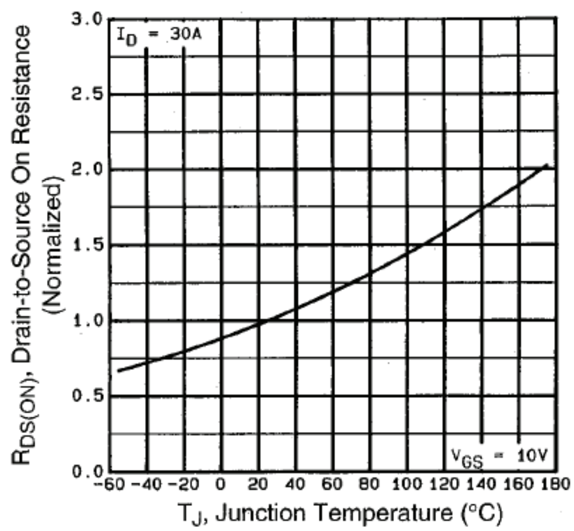


Fig. 4 - Normalized On-Resistance vs. Temperature

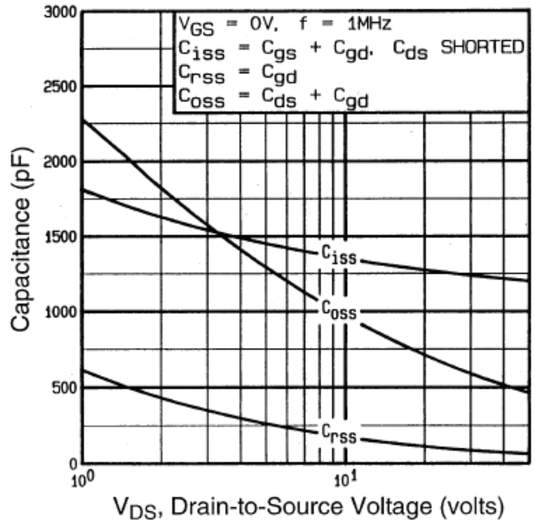


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

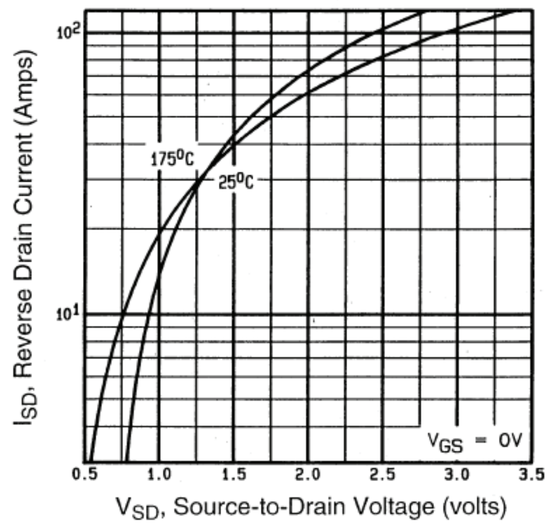


Fig. 7 - Typical Source-Drain Diode Forward Voltage

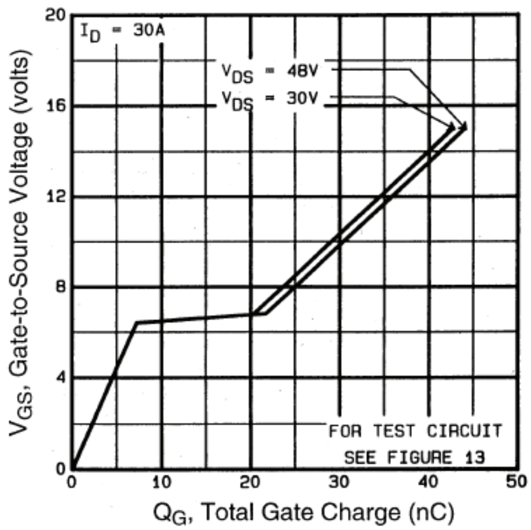


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

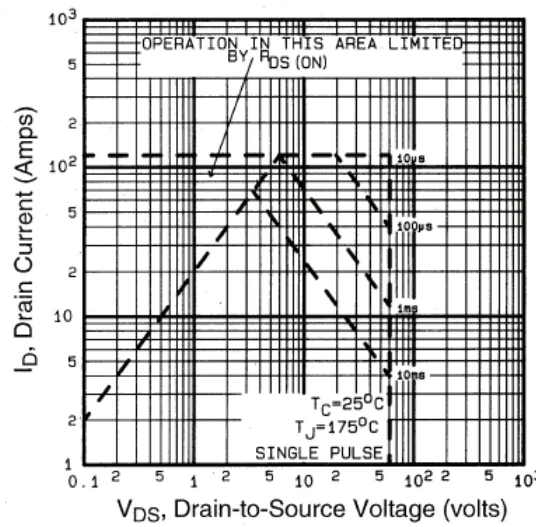


Fig. 8 - Maximum Safe Operating Area

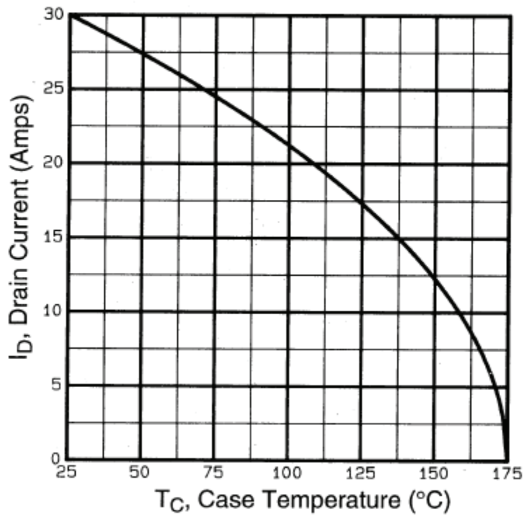


Fig. 9 - Maximum Drain Current vs. Case Temperature

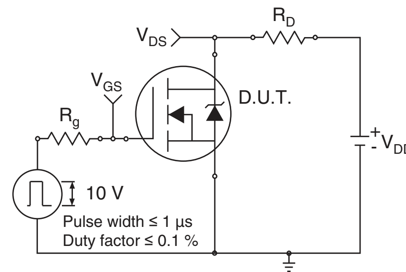


Fig. 10a - Switching Time Test Circuit

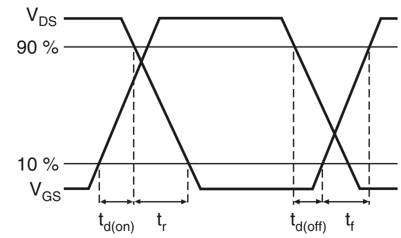


Fig. 10b - Switching Time Waveforms

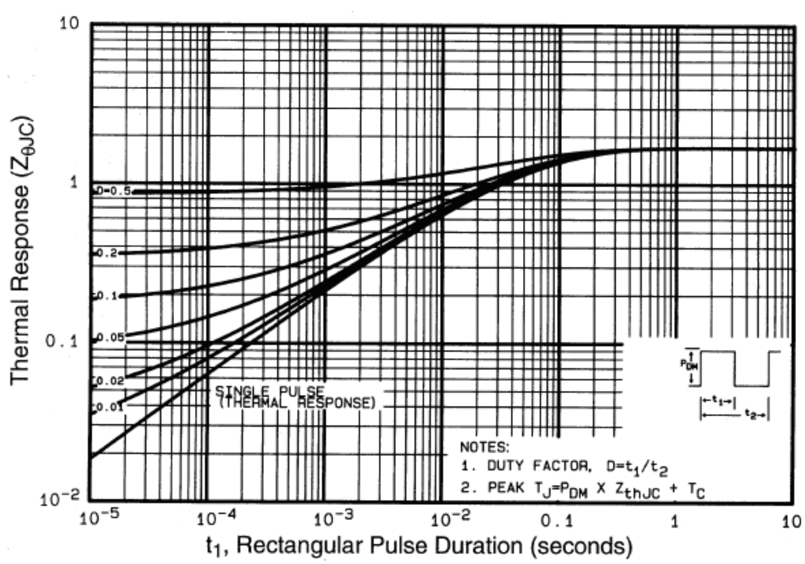


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

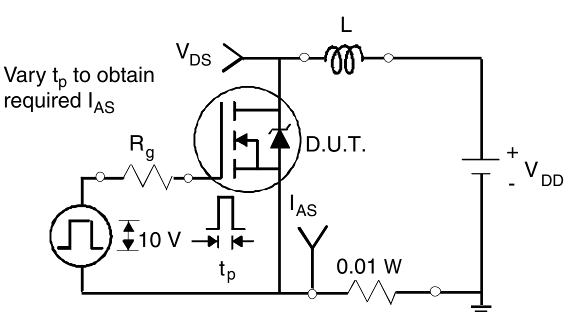


Fig. 12a - Unclamped Inductive Test Circuit

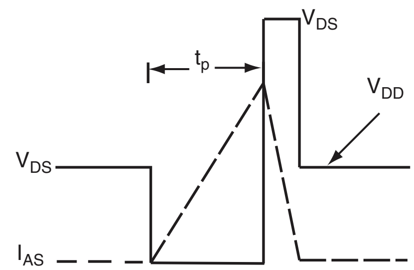


Fig. 12b - Unclamped Inductive Waveforms

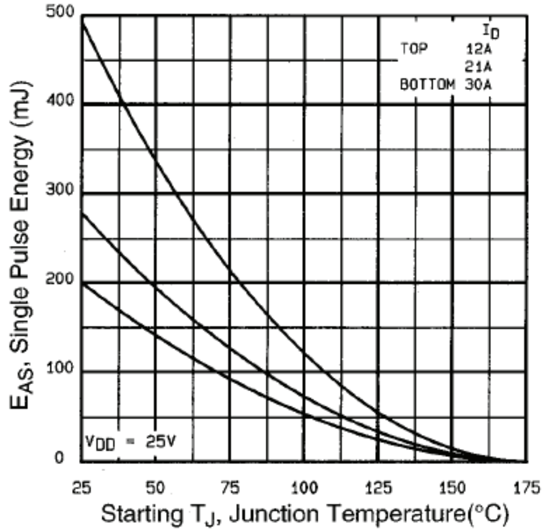


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

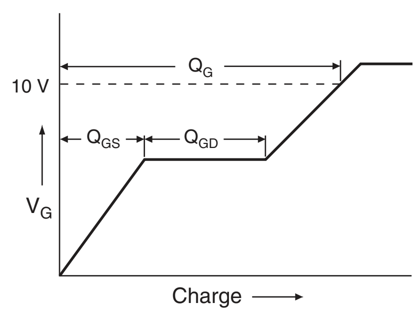


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

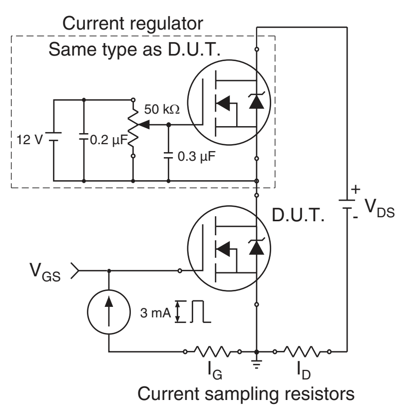
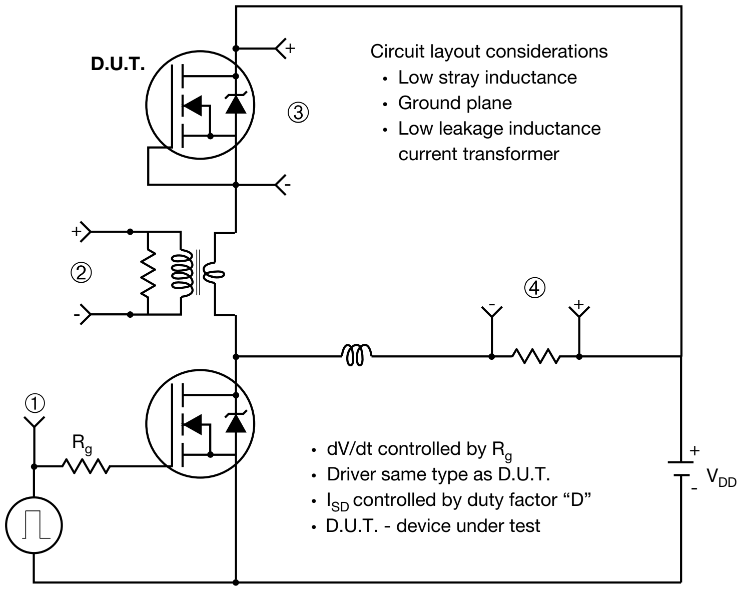
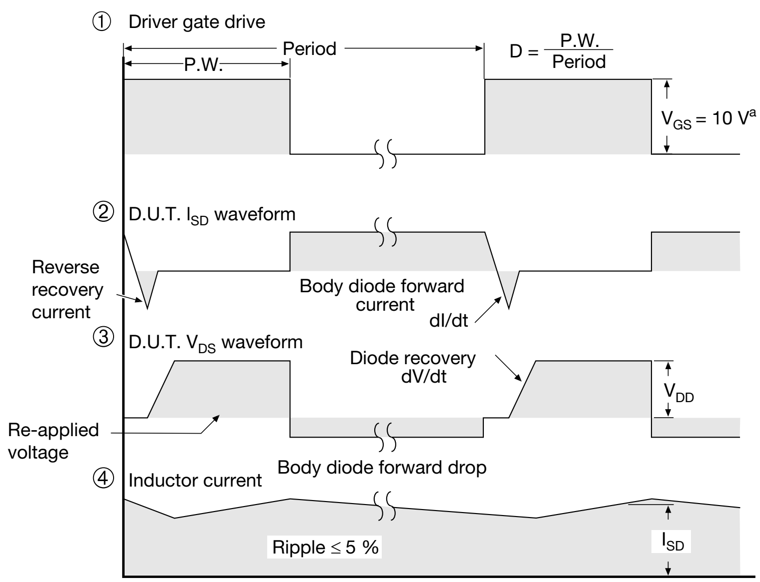


Fig. 13b - Gate Charge Test Circuit

For technical questions, contact: hvm@vishay.com

Peak Diode Recovery dV/dt Test Circuit





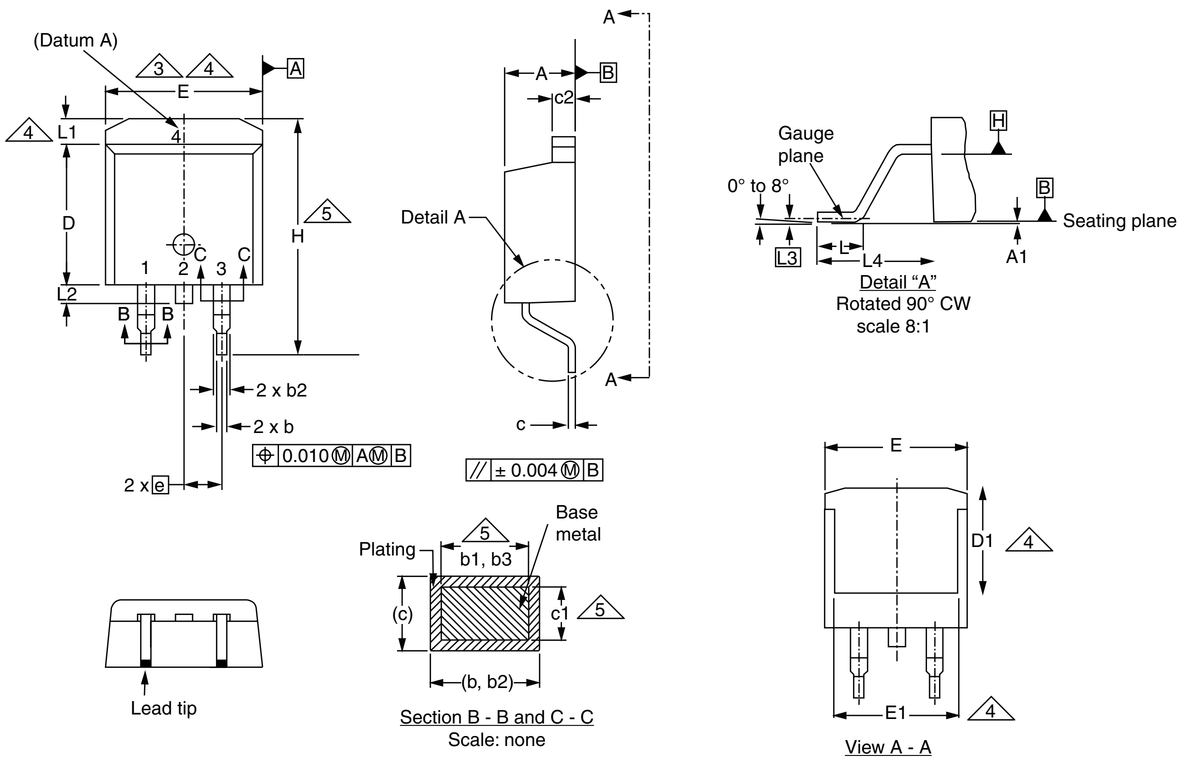
Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?90368.

TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

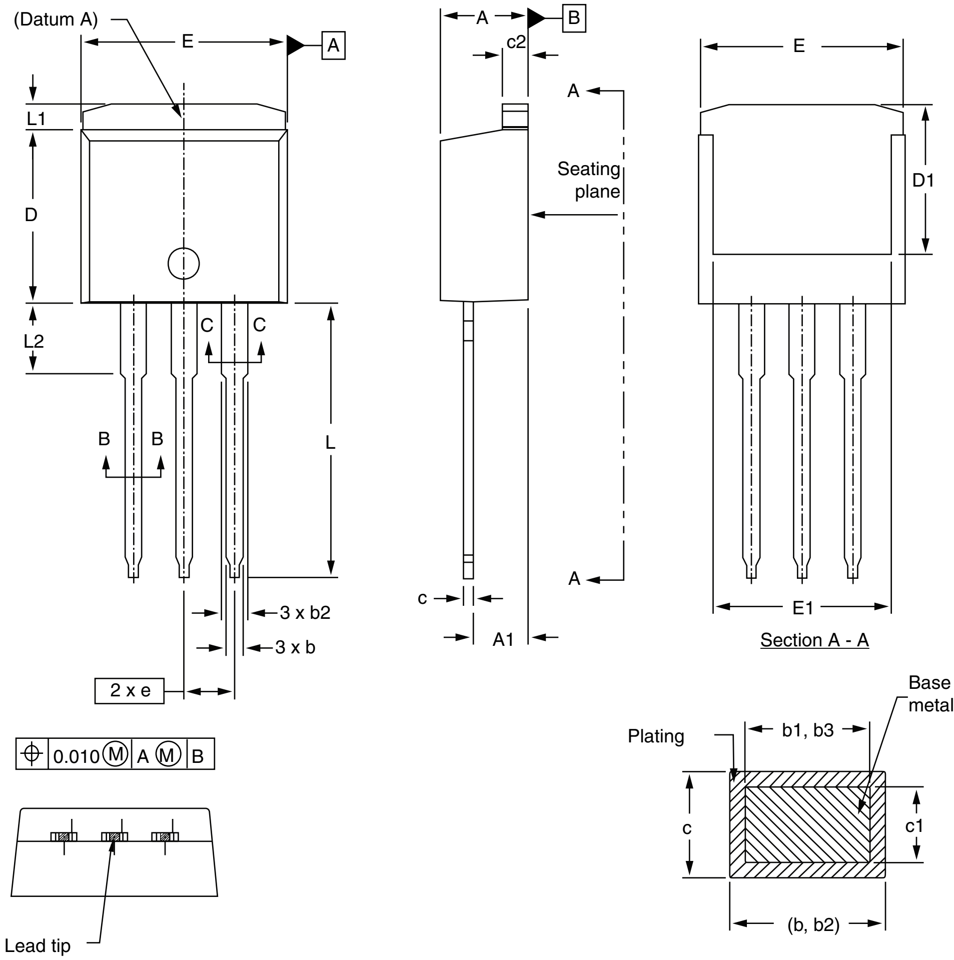
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



Section B - B and C - C
Scale: None

DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

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>>Vishay(威世)