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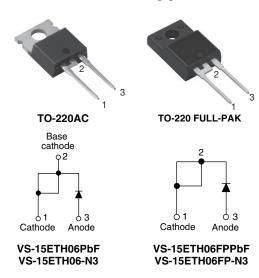
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RoHS

HALOGEN

FREE

Hyperfast Rectifier, 15 A Fred Pt®

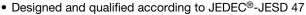


PRODUCT SUMMARY	
Package	TO-220AC, TO-220FP
I _{F(AV)}	15 A
V_{R}	600 V
V _F at I _F	1.3 V
t _{rr} typ.	22 ns
T _J max.	175 °C
Diode variation	Single die

FEATURES

- Hyperfast recovery time
- · Low forward voltage drop
- 175 °C operating junction temperature
- · Low leakage current
- Single die center tap module
- Fully isolated package (V_{INS} = 2500 V_{RMS})
- UL E78996 approved





 Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



State of the art hyperfast recovery rectifiers designed with optimized performance of forward voltage drop, hyperfast recovery time, and soft recovery.

The planar structure and the platinum doped life time control guarantee the best overall performance, ruggedness and reliability characteristics.

These devices are intended for use in PFC boost stage in the AC/DC section of SMPS, inverters or as freewheeling diodes.

Their extremely optimized stored charge and low recovery current minimize the switching losses and reduce over dissipation in the switching element and snubbers.

ABSOLUTE MAXIMUM RATINGS							
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS			
Peak repetitive reverse voltage	V_{RRM}		600	V			
Average rectified femoral comment		T _C = 140 °C	- 15				
Average rectified forward current	I _{F(AV)}	T _C = 80 °C (FULL-PAK)					
NI	I _{FSM}	T _J = 25 °C	120	Α			
Non-repetitive peak surge current		T _J = 25 °C (FULL-PAK)	180	l			
Peak repetitive forward current	I _{FM}		30				
Operating junction and storage temperatures	T _J , T _{Stg}		-65 to +175	°C			

ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise specified)								
PARAMETER	SYMBOL	TEST CONDITIONS MIN.			MAX.	UNITS		
Breakdown voltage, blocking voltage	V_{BR} , V_{R}	$I_R = 100 \mu A$	600	-	-			
Forward voltage	V _F	I _F = 15 A	-	1.8	2.2	V		
		I _F = 15 A, T _J = 150 °C	-	1.3	1.6			
Poverse leekege current	I _R	$V_R = V_R$ rated	-	0.2	50			
Reverse leakage current		$T_J = 150 ^{\circ}\text{C}, V_R = V_R \text{rated}$	-	30	500	- μΑ		
Junction capacitance	C _T	V _R = 600 V	-	20	=	pF		
Series inductance	L _S	Measured lead to lead 5 mm from package body	-	8.0	=	nH		

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DYNAMIC RECOVERY CHARACTERISTICS (T _C = 25 °C unless otherwise specified)								
PARAMETER	SYMBOL	TEST CO	MIN.	TYP.	MAX.	UNITS		
		$I_F = 1 \text{ A, } dI_F/dt = 100 \text{ A/}\mu\text{s, } V_R = 30 \text{ V}$		-	22	30		
Reverse recovery time	+	$I_F = 15 \text{ A}, dI_F/dt = 100$	$I_F = 15 \text{ A}, dI_F/dt = 100 \text{ A/}\mu\text{s}, V_R = 30 \text{ V}$		28	35		
neverse recovery time	t _{rr}	T _J = 25 °C		-	29	-	ns	
		T _J = 125 °C	I _F = 15 A dI _F /dt = 200 A/μs V _R = 390 V	-	75	-		
Deal and a second	I _{RRM}	T _J = 25 °C		=	3.5	-	А	
Peak recovery current		T _J = 125 °C		=	7	-		
Daylaraa raaayan aharaa	Q _{rr}	T _J = 25 °C		-	57	-	nC	
Reverse recovery charge		T _J = 125 °C		-	300	-	nc	
Reverse recovery time	t _{rr}		I _F = 15 A dI _F /dt = 800 A/μs V _R = 390 V	-	51	-	ns	
Peak recovery current	I _{RRM}	T _J = 125 °C		=	20	-	Α	
Reverse recovery charge	Q _{rr}			-	580	-	nC	

THERMAL MECHANICAL	SPECI				7.0	2424	
PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Maximum junction and storage temperature range		T _J , T _{Stg}		-65	-	175	°C
Thermal resistance,		D		-	1.0	1.3	
junction to case (FUL	_L-PAK)	R_{thJC}		-	3.0	3.5	
Thermal resistance, junction to ambient per leg		R _{thJA}	Typical socket mount	-	-	70	°C/W
Thermal resistance, case to heatsink		R _{thCS}	Mounting surface, flat, smooth and greased	-	0.5	-	
Weight				-	2.0	-	g
Weight				-	0.07	-	oz.
Mounting torque				6.0 (5.0)	-	12 (10)	kgf · cm (lbf · in)
Marking device			Case style TO-220AC	15ETH06		•	
			Case style TO-220 FULL-PAK	15ETH06FP			

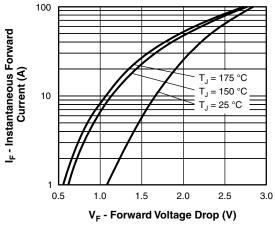


Fig. 1 - Typical Forward Voltage Drop Characteristics

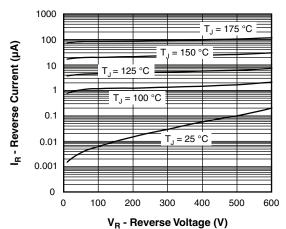


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

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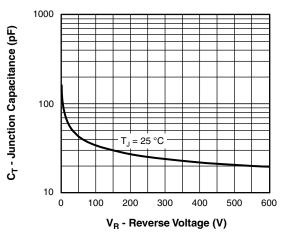


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

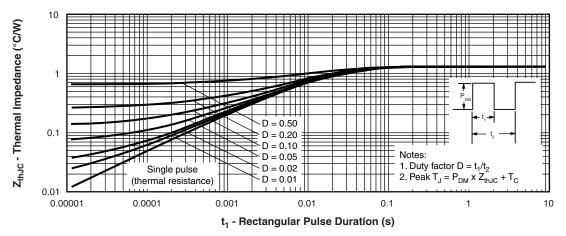


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

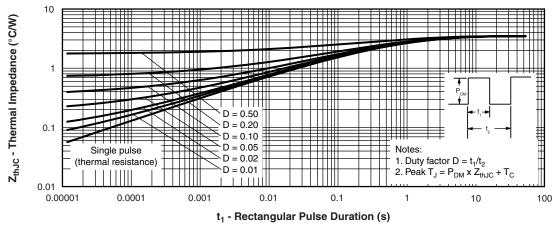
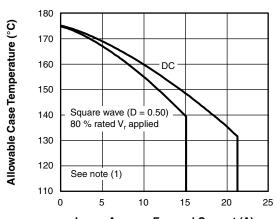


Fig. 5 - Maximum Thermal Impedance Z_{thJC} Characteristics (FULL-PAK)

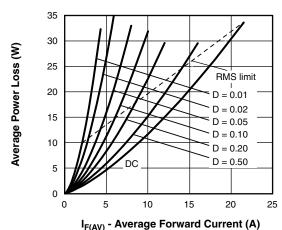
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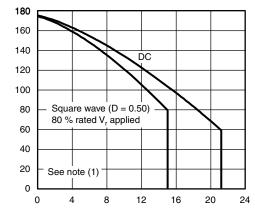
I_{F(AV)} - Average Forward Current (A)

Fig. 6 - Maximum Allowable Case Temperature vs. Average Forward Current



- F(AV) Therage Fernand Current (1.)

Fig. 8 - Forward Power Loss Characteristics



I_{F(AV)} - Average Forward Current (A)

Fig. 7 - Maximum Allowable Case Temperature vs. Average Forward Current (FULL-PAK)

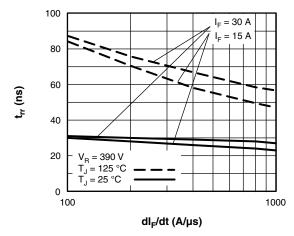


Fig. 9 - Typical Reverse Recovery Time vs. dl_F/dt

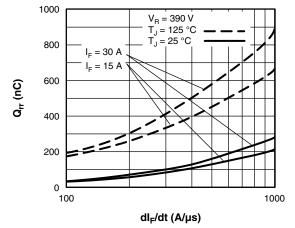


Fig. 10 - Typical Stored Charge vs. dl_F/dt

Note

Allowable Case Temperature (°C)

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{th,JC}$; $Pd = Forward power loss = I_{F(AV)} \times V_{FM} at (I_{F(AV)}/D)$ (see fig. 8); $Pd_{REV} = Inverse power loss = V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = Rated V_R$

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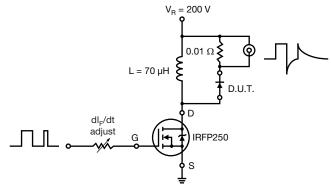
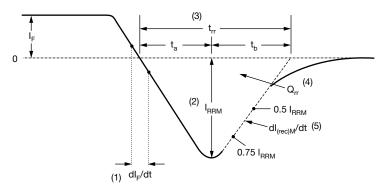


Fig. 11 - Reverse Recovery Parameter Test Circuit



- (1) dl_F/dt rate of change of current through zero crossing
- (2) I_{RRM} peak reverse recovery current
- (3) t_{rr} reverse recovery time measured from zero crossing point of negative going I_F to point where a line passing through 0.75 I_{RBM} and 0.50 I_{RBM} extrapolated to zero current.
- (4) ${\rm Q_{rr}}$ area under curve defined by ${\rm t_{rr}}$ and ${\rm I_{BBM}}$

$$Q_{rr} = \frac{t_{rr} \times I_{RRM}}{2}$$

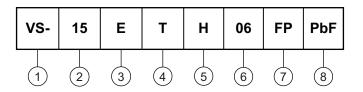
(5) $dI_{(rec)M}/dt$ - peak rate of change of current during t_b portion of t_{rr}

Fig. 12 - Reverse Recovery Waveform and Definitions

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ORDERING INFORMATION TABLE

Device code



1 - Vishay Semiconductors product

2 - Current rating (15 = 15 A)

3 - E = single diode

4 - $T = TO-220, D^2PAK$

- H = hyperfast recovery

Voltage rating (06 = 600 V)

7 - • None = TO-220AC

• FP = TO-220 FULL-PAK

8 - Environmental digit:

PbF = lead (Pb)-free and RoHS-compliant

-N3 = halogen-free, RoHS-compliant and totally lead (Pb)-free

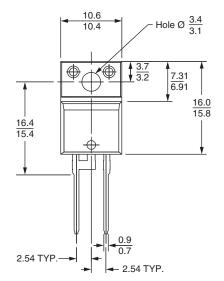
ORDERING INFORMATION (Example)							
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION				
VS-15ETH06PbF	50	1000	Antistatic plastic tube				
VS-15ETH06-N3	50	1000	Antistatic plastic tube				
VS-15ETH06FPPbF	50	1000	Antistatic plastic tube				
VS-15ETH06FP-N3	50	1000	Antistatic plastic tube				

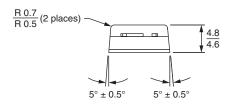
LINKS TO RELATED DOCUMENTS						
Dimensions	TO-220AC	www.vishay.com/doc?95221				
Dimensions	TO-220FP	www.vishay.com/doc?95005				
	TO-220ACPbF	www.vishay.com/doc?95224				
Part marking information	TO-220AC-N3	www.vishay.com/doc?95068				
Fait marking information	TO-220FPPbF	www.vishay.com/doc?95009				
	TO-220FP-N3	www.vishay.com/doc?95440				

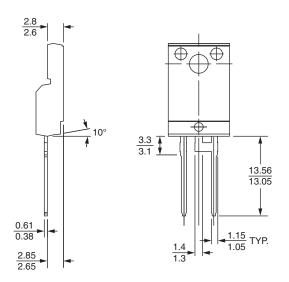


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DIMENSIONS in millimeters







Lead assignments

Diodes 1 + 2 - Cathode

3 - Anode

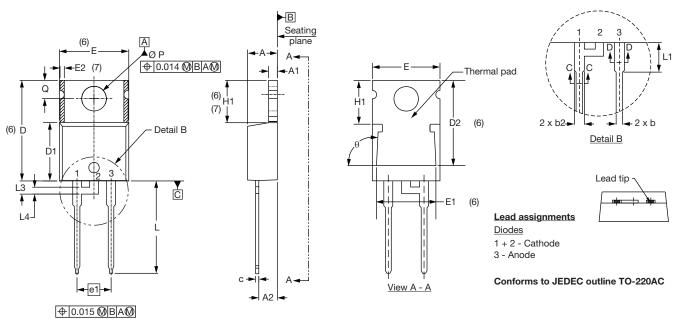
Conforms to JEDEC outline TO-220 FULL-PAK



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TO-220AC

DIMENSIONS in millimeters and inches



SYMBOL	MILLIM	IETERS	INC	HES	NOTES
STWIDOL	MIN.	MAX.	MIN.	MAX.	NOTES
Α	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
С	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
Е	10.11	10.51	0.398	0.414	3, 6

SYMBOL	MILLIM	IETERS	INC	HES	NOTES
STIVIBOL	MIN.	MAX.	MIN.	MAX.	NOTES
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
е	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
L3	1.78	2.13	0.070	0.084	
L4	0.76	1.27	0.030	0.050	2
ØΡ	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° t	o 93°	90° to 93°		
		•		•	•

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, D2 (minimum) where dimensions are derived from the actual package outline





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