## **SQ4153EY**

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**Vishay Siliconix** 

## Automotive P-Channel 12 V (D-S) 175 °C MOSFET



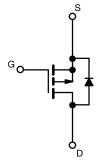
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-12			
$R_{DS(on)}$ (Ω) at $V_{GS}$ = -4.5 V	0.00832			
$R_{DS(on)}\left(\Omega\right)$ at $V_{GS}$ = -2.5 V	0.01000			
$R_{DS(on)}\left(\Omega\right)$ at $V_{GS}$ = -1.8 V	0.01430			
I <sub>D</sub> (A)	-25			
Configuration	Single			

#### **FEATURES**

- TrenchFET<sup>®</sup> power MOSFET
- AEC-Q101 qualified
- 100 %  $R_q$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



FREE



P-Channel MOSFET

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	SQ4153EY (for detailed order number please see <u>www.vishay.com/doc?79771</u> )

ABSOLUTE MAXIMUM RATING	<b>iS</b> (T <sub>C</sub> = 25 °C, unless	otherwise noted	ł)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	-12	V
Gate-source voltage		V <sub>GS</sub>	± 8	
Continuous drain current <sup>a</sup>	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	-25	
	T <sub>C</sub> = 125 °C		-14	
Continuous source current (diode conduction) <sup>a</sup>		I <sub>S</sub>	-6.5	А
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	-100	
Single pulse avalanche current		I <sub>AS</sub>	-19	
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	18	mJ
Maximum power dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	PD	7.1	W
	T <sub>C</sub> = 125 °C		2.3	vv
Operating junction and storage temperature	erange	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	85	°C/W	
Junction-to-foot (drain)		R <sub>thJF</sub>	21	0/10	

#### Notes

a. Package limited

b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

c. When mounted on 1" square PCB (FR4 material)

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static		•						
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0, I_D = -250 \ \mu A$		-12	-	-	v	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}$ , $I_D = -250 \ \mu A$		-0.6	-0.9	v	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 8 V$		-	-	± 100	nA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = -12 V	-	-	-1		
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS}$ = -12 V, T <sub>J</sub> = 125 °C	-	-	-50	μA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = -12 V, T <sub>J</sub> = 175 °C	-	-	-150		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -4.5 V	$V_{DS} \ge -5 V$	-30	-	-	Α	
		$V_{GS} = -4.5 V$	I <sub>D</sub> = -14 A	-	0.00510	0.00832		
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -14 A, T <sub>J</sub> = 125 °C	-	-	0.00900		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -14 A, T <sub>J</sub> = 175 °C	-	-	0.01100	Ω	
		V <sub>GS</sub> = -2.5 V	I <sub>D</sub> = -13 A	-	0.00650	0.01000		
		V <sub>GS</sub> = -1.8 V	I <sub>D</sub> = -12 A	-	0.00940	0.01430		
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> =	-6 V, I <sub>D</sub> = -10.5 A	-	54	-	S	
Dynamic <sup>b</sup>		•						
Input capacitance	C <sub>iss</sub>			-	7500	11 000	pF	
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = -6 V, f = 1 MHz	-	2800	4200		
Reverse transfer capacitance	C <sub>rss</sub>	-		-	2400	3600		
Total gate charge <sup>c</sup>	Qg			-	101	151		
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = -4.5 V	$V_{DS} = -6 V, I_D = -10.5 A$	-	15	-	nC	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	45	-		
Gate resistance	Rg	f = 1 MHz		1.1	2.2	3.2	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	$V_{DD} = -6 \text{ V}, \text{ R}_{\text{L}} = 15 \ \Omega$ $\text{I}_{\text{D}} \cong -10.5 \text{ A}, \text{ V}_{\text{GEN}} = -4.5 \text{ V}, \text{ R}_{\text{g}} = 6 \ \Omega$		-	31	42		
Rise time <sup>c</sup>	tr			-	168	224		
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	310	412	ns	
Fall time <sup>c</sup>	t <sub>f</sub>			-	283	376		
Source-Drain Diode Ratings and Cha	racteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	-100	Α	
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = -10.5 A, V <sub>GS</sub> = 0		-	-0.8	-1.2	V	

Notes

a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$ 

b. Guaranteed by design, not subject to production testing

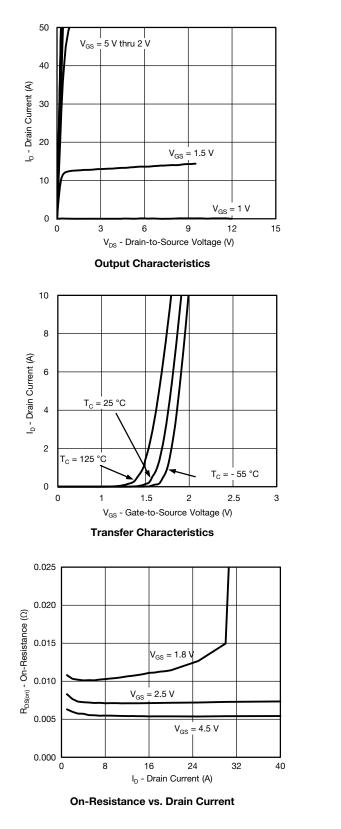
c. Independent of operating temperature

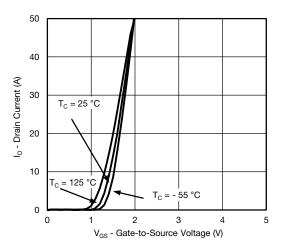
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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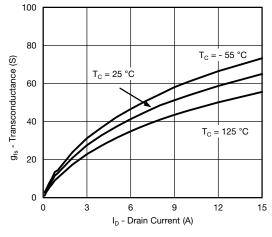


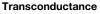
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

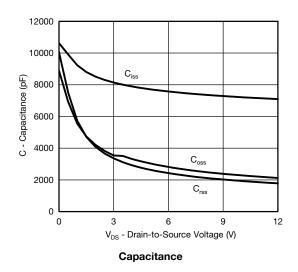




Transfer Characteristics







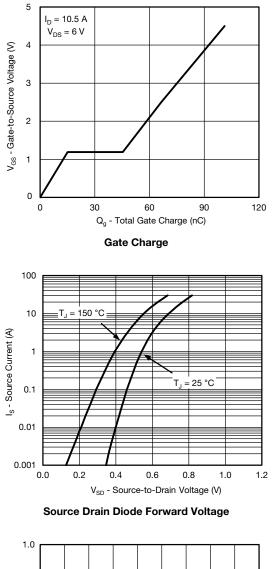
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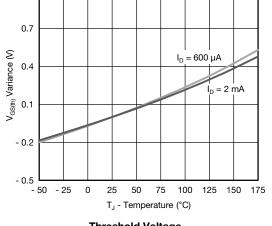
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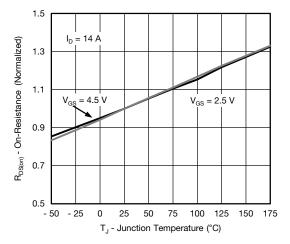


### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)

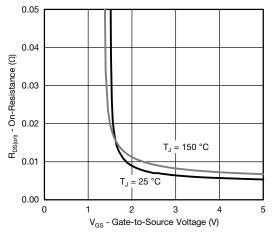




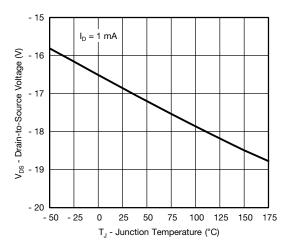
**Threshold Voltage** 



**On-Resistance vs. Junction Temperature** 







Breakdown Voltage vs. Junction Temperature

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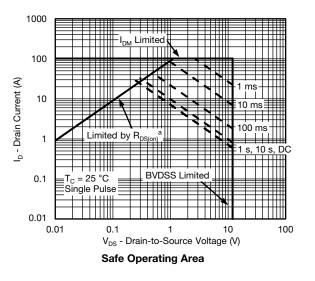
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### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

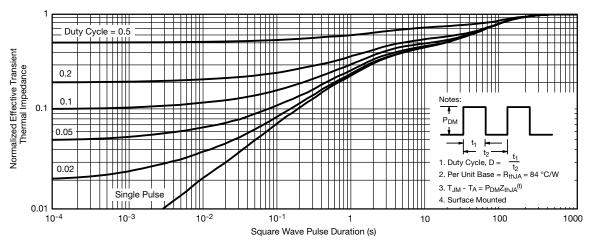


#### Note

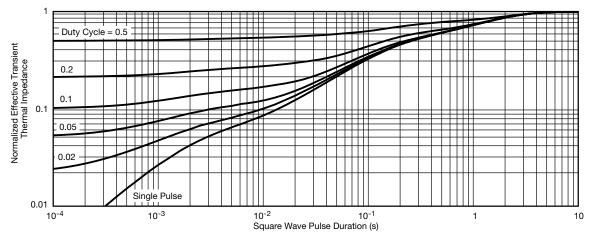
a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



#### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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## Package Information

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### SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012





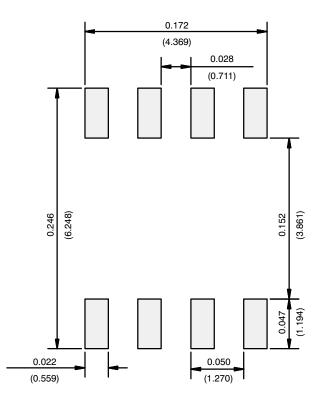
	MILLIMETERS		INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

## **Application Note 826**

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**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)

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# Application Note 826

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#### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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