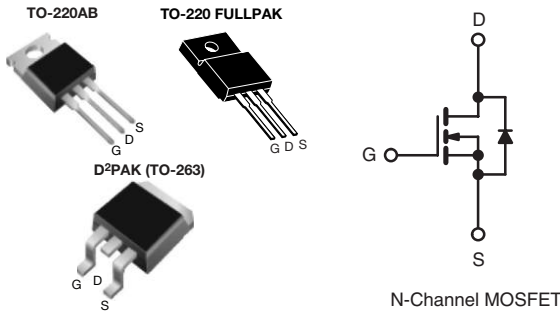


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	560 V
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V   0.555
$Q_g$ (Max.) (nC)	48
$Q_{gs}$ (nC)	12
$Q_{gd}$ (nC)	15
Configuration	Single

### FEATURES

- Low Figure-of-Merit  $R_{on} \times Q_g$
- 100 % Avalanche Tested
- Gate Charge Improved
- $T_{rr}/Q_{rr}$  Improved
- Compliant to RoHS Directive 2002/95/EC



ORDERING INFORMATION			
Package	TO-220AB	D²PAK (TO-263)	TO-220 FULLPAK
Lead (Pb)-free	SiHP12N50C-E3	SiHB12N50C-E3	SiHF12N50C-E3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT		UNIT
		TO220-AB D²PAK (TO-263)	TO-220 FULLPAK	
Drain-Source Voltage	$V_{DS}$	500		V
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$V_{GS}$ at 10 V	$T_C = 25^\circ\text{C}$	12	A
		$T_C = 100^\circ\text{C}$	7.5	
Pulsed Drain Current <sup>c</sup>	$I_{DM}$	28		
Linear Derating Factor		1.67	0.28	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	180		mJ
Maximum Power Dissipation	$P_D$	208	36	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s	300		

### Notes


- Limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25^\circ\text{C}$ ,  $L = 2.5$  mH,  $R_g = 25 \Omega$ ,  $I_{AS} = 12$  A.
- Repetitive rating; pulse width limited by maximum junction temperature.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TO220-AB D <sup>2</sup> PAK (TO-263)	TO-220 FULLPAK	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	62	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	0.6	3.5	
Junction-to-Ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	40	-	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4\text{ A}$	-	0.46	0.555	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 3\text{ A}$		-	3	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$		-	1375	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	165	-	
Reverse Transfer Capacitance	$C_{rss}$			-	17	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, V_{DS} = 400\text{ V}$	-	32	48	nC
Gate-Source Charge	$Q_{gs}$			-	12	-	
Gate-Drain Charge	$Q_{gd}$			-	15	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 10\text{ A}, R_g = 4.3\text{ }\Omega, V_{GS} = 10\text{ V}$		-	18	-	ns
Rise Time	$t_r$			-	35	-	
Turn-Off Delay Time	$t_{d(off)}$			-	23	-	
Fall Time	$t_f$			-	6	-	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$		-	1.1	-	$\Omega$
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	12	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	28	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 10\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S, dI/dt = 100\text{ A}/\mu\text{s}, V_R = 20\text{ V}$		-	580	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	4.3	-	$\mu\text{C}$
Body Diode Reverse Recovery Current	$I_{RRM}$			-	13	-	A

**Note**

- The information shown here is a preliminary product proposal, not a commercial product data sheet. Vishay Siliconix is not committed to produce this or any similar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

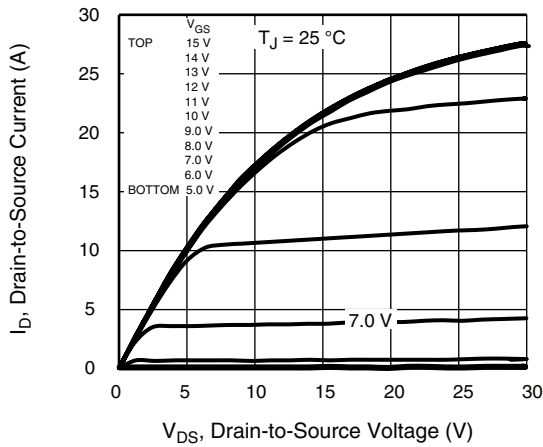


Fig. 1 - Typical Output Characteristics (TO-220)

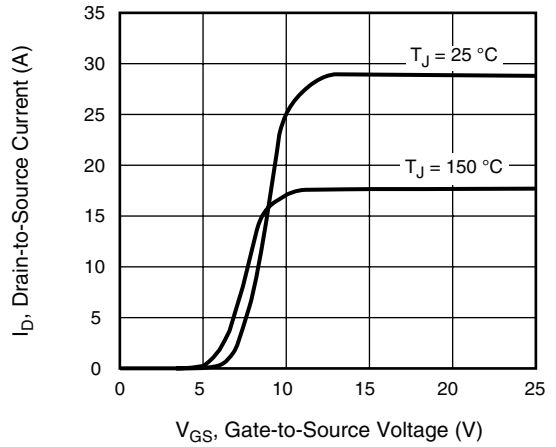


Fig. 3 - Typical Transfer Characteristics

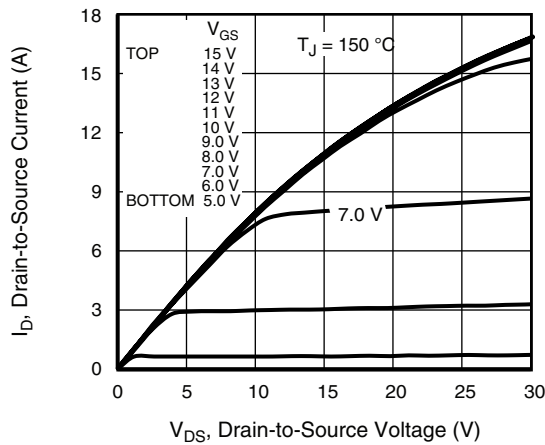


Fig. 2 - Typical Output Characteristics (TO-220)

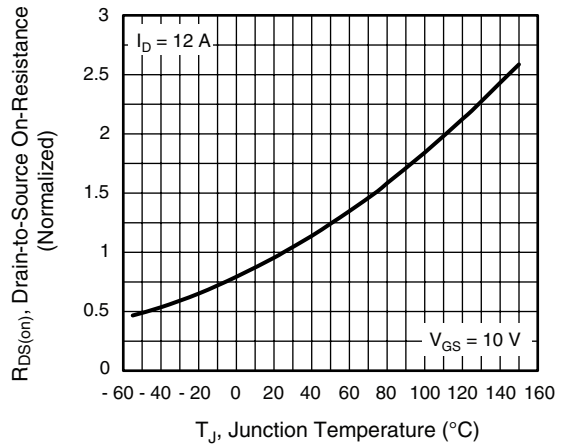


Fig. 4 - Normalized On-Resistance vs. Temperature

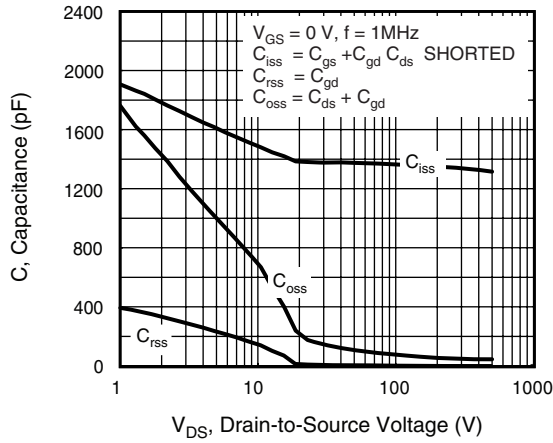


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

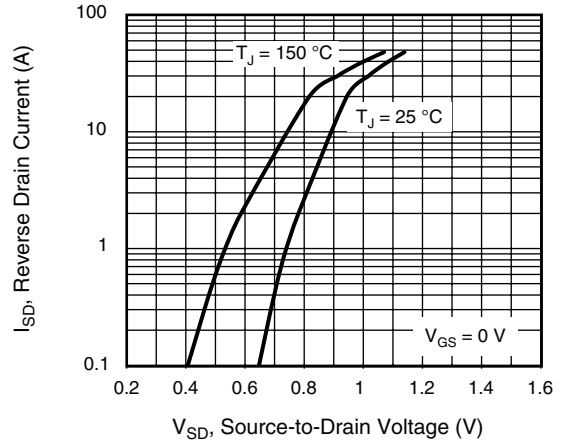


Fig. 7 - Typical Source-Drain Diode Forward Voltage

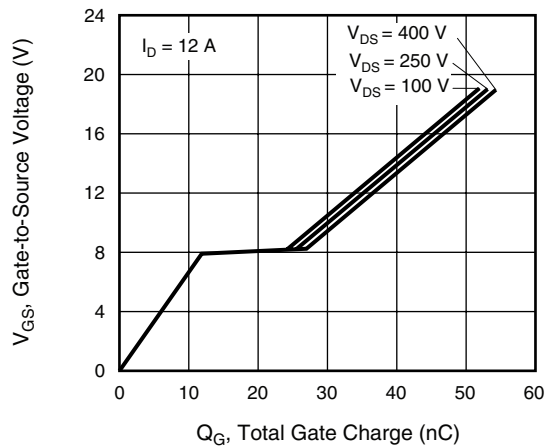


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

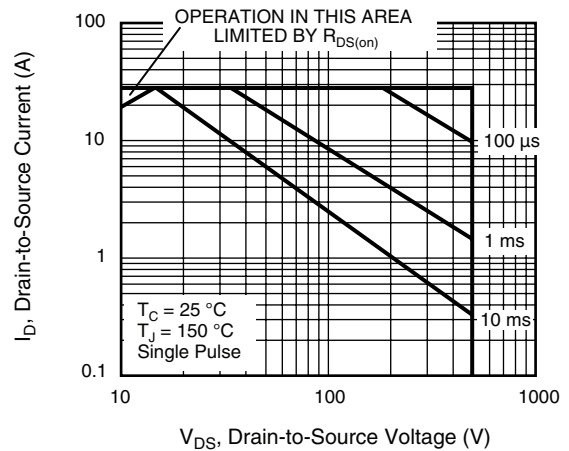


Fig. 8 - Maximum Safe Operating Area (TO-220AB, D<sup>2</sup>PAK)

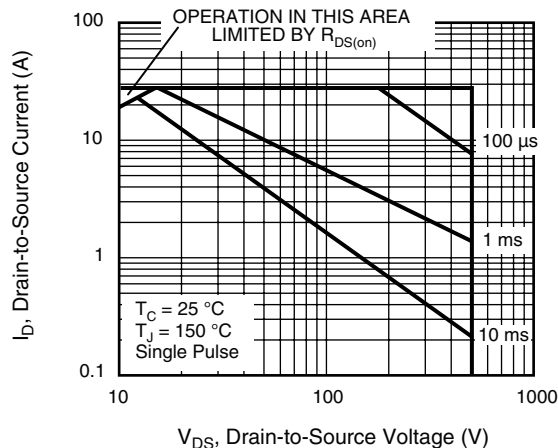
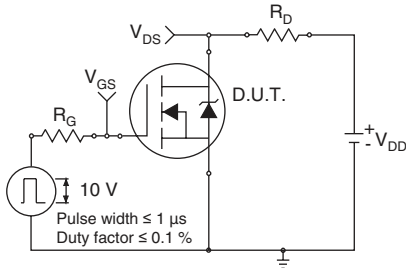
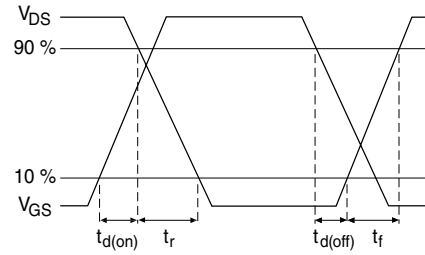


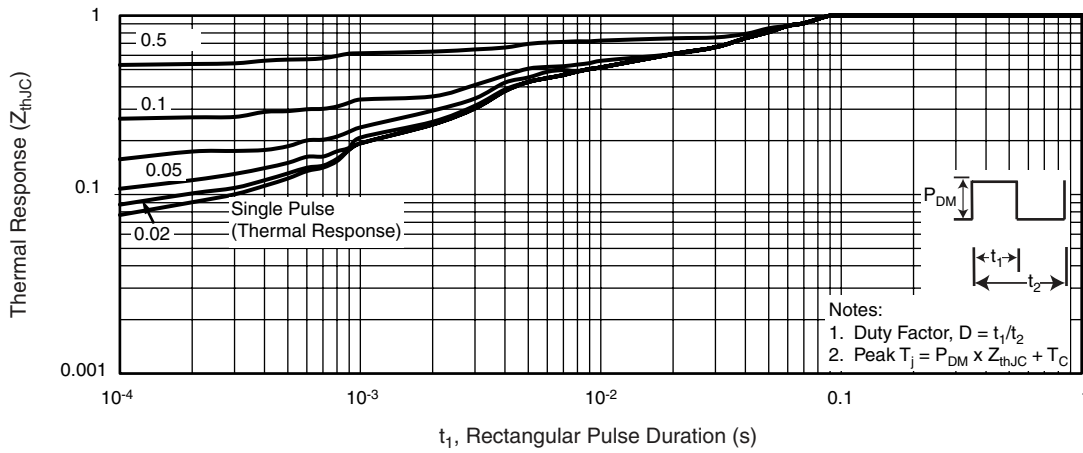
Fig. 9 - Maximum Safe Operating Area (TO-220 FULLPAK)



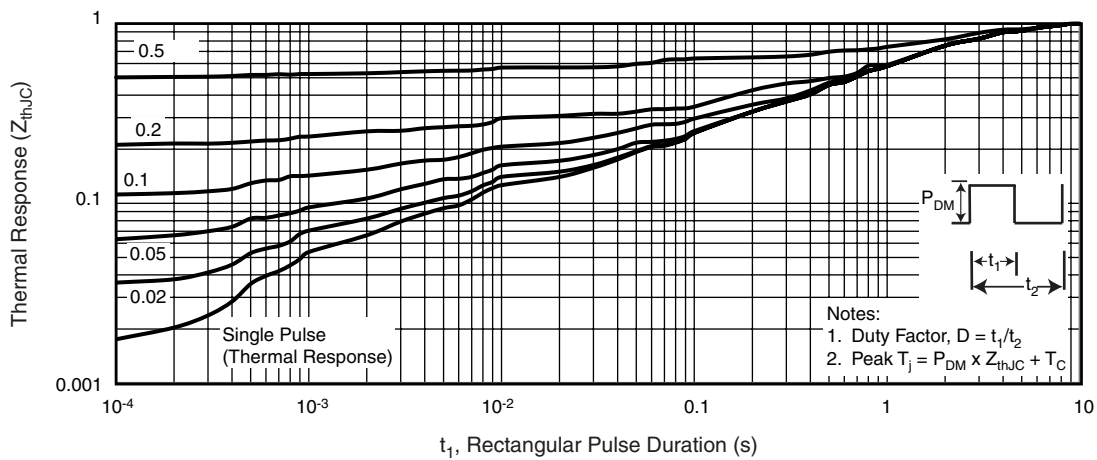
**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220AB, D<sup>2</sup>PAK)**



**Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220 FULLPAK)**

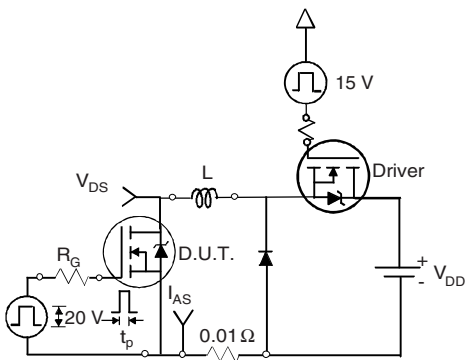


Fig. 13a - Unclamped Inductive Test Circuit

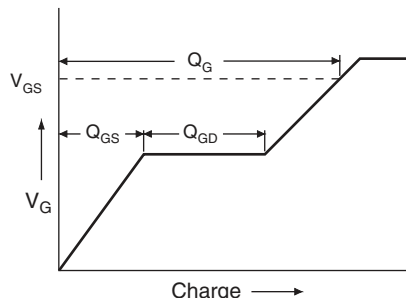


Fig. 14a - Basic Gate Charge Waveform

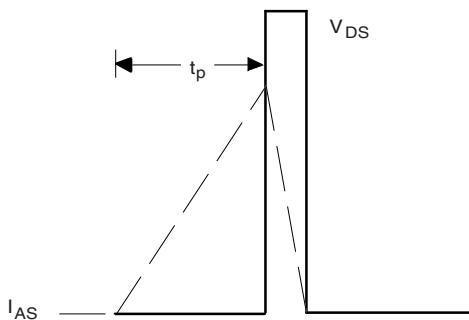


Fig. 13b - Unclamped Inductive Waveforms

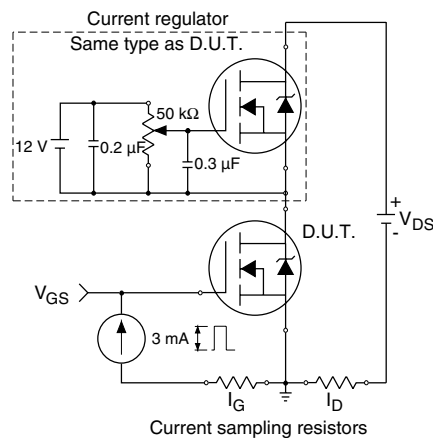
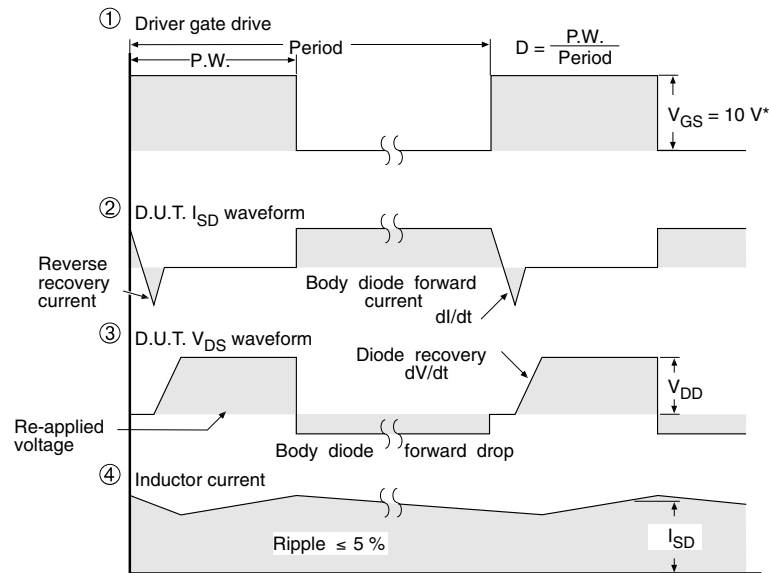
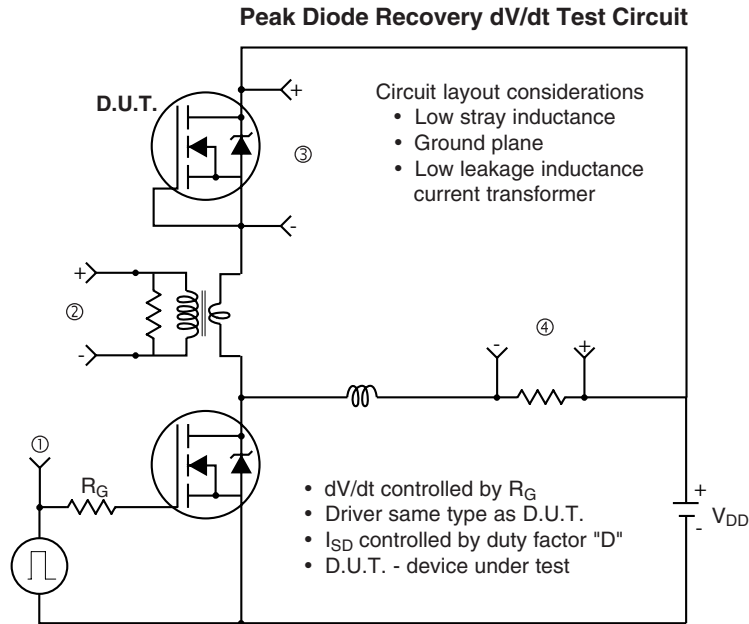


Fig. 14b - Gate Charge Test Circuit



\*  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 15 - For N-Channel**

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## TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
$\varnothing P$	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15  
DWG: 6031

**Note**

- $M^*$  = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

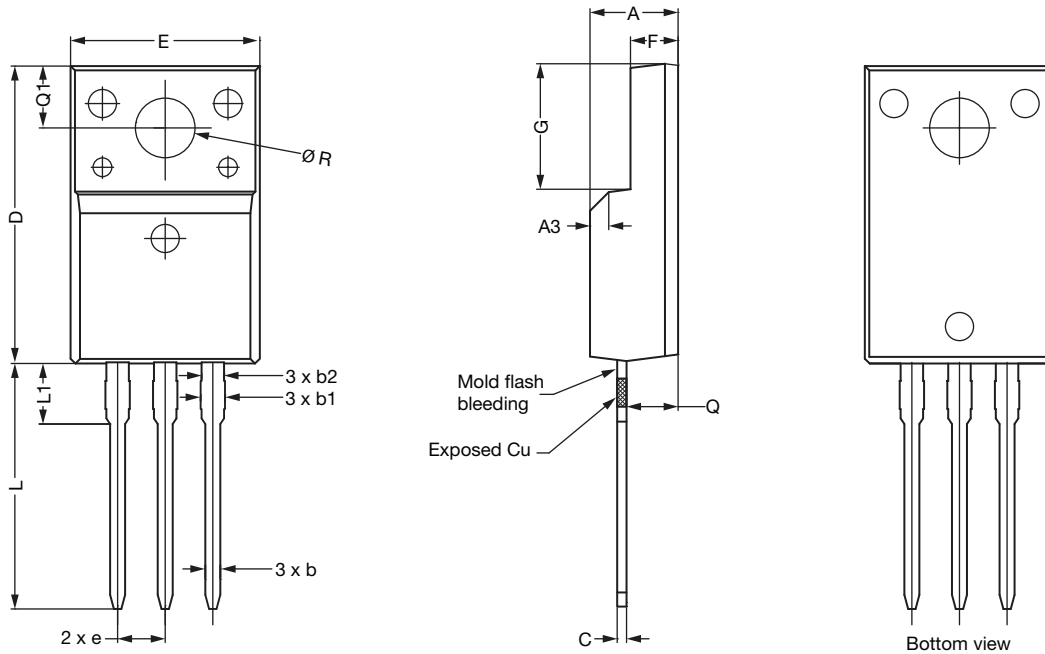






# TO-220 FULLPAK (High Voltage)

## OPTION 1: FACILITY CODE = 9



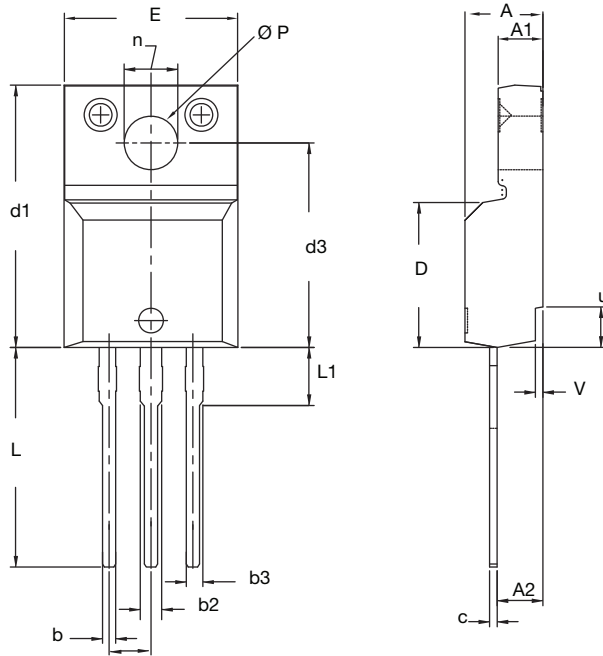
DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
$\varnothing R$	3.08	3.18	3.28

### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking



OPTION 2: FACILITY CODE = Y



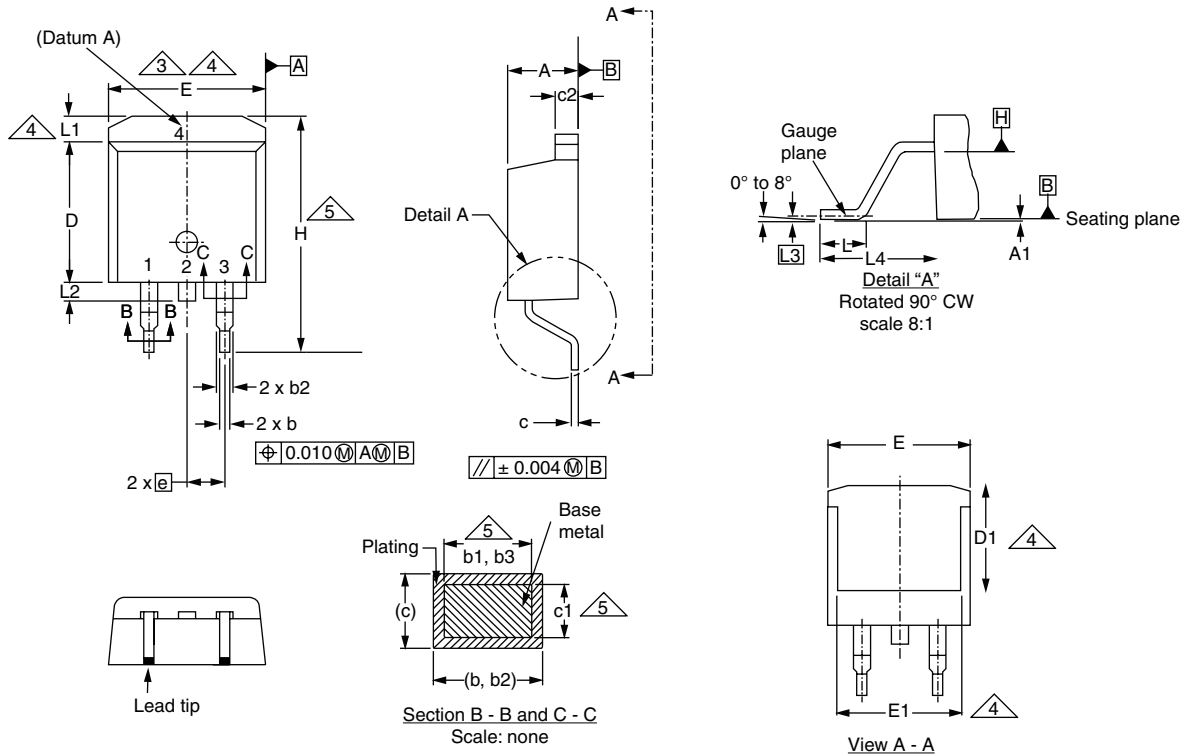
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
DWG: 5972

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking

### TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

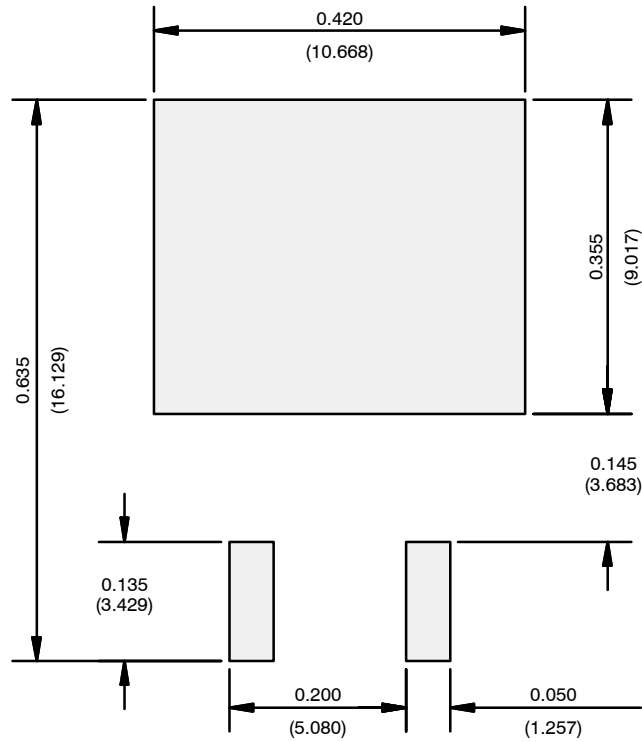
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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