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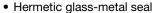
Vishay Semiconductors

# Phase Control Thyristors (Stud Version), 80 A



PRIMARY CHARACTERISTICS				
I <sub>T(AV)</sub>	80 A			
V <sub>DRM</sub> /V <sub>RRM</sub>	400 V, 800 V, 1200 V			
$V_{TM}$	1.60 V			
I <sub>GT</sub>	120 mA			
TJ	-40 °C to +125 °C			
Package	TO-94 (TO-209AC)			
Circuit configuration	Single SCR			

#### **FEATURES**





• International standard case TO-94 (TO-209AC)

Designed and qualified for industrial level

ROHS

 Material categorization: For definitions of compliance please see <a href="https://www.vishav.com/doc?99912">www.vishav.com/doc?99912</a>

#### **TYPICAL APPLICATIONS**

- DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS					
PARAMETER	TEST CONDITIONS	VALUES	UNITS		
1		80	Α		
I <sub>T(AV)</sub>	T <sub>C</sub>	85	°C		
I <sub>T(RMS)</sub>		125			
1	50 Hz	1900	Α		
I <sub>TSM</sub>	60 Hz	1990			
2t	50 Hz	18	kA <sup>2</sup> s		
1-1	60 Hz	16	KA-S		
V <sub>DRM</sub> /V <sub>RRM</sub>		400 to 1200	V		
t <sub>q</sub>	Typical	110	μs		
TJ		-40 to +125	°C		

#### **ELECTRICAL SPECIFICATIONS**

VOLTAGE RATINGS							
TYPE NUMBER	VOLTAGE CODE	V <sub>DRM</sub> /V <sub>RRM</sub> , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I <sub>DRM</sub> /I <sub>RRM</sub> MAXIMUM AT T <sub>J</sub> = 125 °C mA			
\(\alpha\)	40	400	500				
VS-80RIA VS-81RIA	80	800	900	15			
VO 0111111	120	1200	1300				



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PARAMETER	SYMBOL		TEST CON	IDITIONS	VALUES	UNITS
Maximum average on-state current		190° condu	180° conduction, half sine wave		80	Α
at case temperature	I <sub>T(AV)</sub>	160 Condu	Cuon, nan sine w	rave	85	°C
Maximum RMS on-state current	I <sub>T(RMS)</sub>	DC at 75 °C	case temperatu	re	125	
		t = 10 ms	No voltage		1900	
Maximum peak, one-cycle		t = 8.3 ms	reapplied		1990	A kA <sup>2</sup> s
non-repetitive surge current	I <sub>TSM</sub>	t = 10 ms	100 % V <sub>RRM</sub>		1600	
		t = 8.3 ms	reapplied	Sinusoidal half wave,	1675	
Maximum I <sup>2</sup> t for fusing	l <sup>2</sup> t	t = 10 ms	No voltage	initial $T_J = T_J$ maximum	18	
		t = 8.3 ms			16	
		t = 10 ms	100 % V <sub>RRM</sub>		12.7	
		t = 8.3 ms	reapplied		11.7	
Maximum $I^2\sqrt{t}$ for fusing	l²√t	t = 0.1 ms to 10 ms, no voltage reapplied		age reapplied	180.5	kA²√s
Low level value of threshold voltage	V <sub>T(TO)1</sub>	(16.7 % x π	$x I_{T(AV)} < I < \pi x$	$I_{T(AV)}$ ), $T_J = T_J$ maximum	0.99	V
High level value of threshold voltage	V <sub>T(TO)2</sub>	$(I > \pi \times I_{T(AV)})$	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$		1.13	V
Low level value of on-state slope resistance	r <sub>t1</sub>	(16.7 % x $\pi$ x $I_{T(AV)}$ < I < $\pi$ x $I_{T(AV)}$ ), $T_J = T_J$ maximum		2.29	mΩ	
High level value of on-state slope resistance	r <sub>t2</sub>	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$		1.84	11152	
Maximum on-state voltage	$V_{TM}$	$I_{pk} = 250 \text{ A}, T_J = 25 \text{ °C}, t_p = 10 \text{ ms sine pulse}$		10 ms sine pulse	1.60	V
Maximum holding current	I <sub>H</sub>			W registive lead	200	mA
Typical latching current	ΙL	T <sub>J</sub> = 25 °C, anode supply 12 V resistive load		400	] IIIA	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	dl/dt	$T_J$ = 125 °C, $V_d$ = Rated $V_{DRM}$ , $I_{TM}$ = 2 x dl/dt snubber 0.2 μF, 15 $\Omega$ , gate pulse: 20 V, 65 $\Omega$ , $t_p$ = 6 μs, $t_r$ = 0.5 μs Per JEDEC standard RS-397, 5.2.2.6.	300	A/µs
Typical delay time	t <sub>d</sub>	Gate pulse: 10 V, 15 $\Omega$ source, $t_p$ = 6 $\mu$ s, $t_r$ = 0.1 $\mu$ s, $V_d$ = Rated $V_{DRM}$ , $I_{TM}$ = 50 Adc, $T_J$ = 25 °C	1	116
Typical turn-off time	t <sub>q</sub>	$I_{TM}$ = 50 A, $T_J$ = $T_J$ maximum, dl/dt = -5 A/ $\mu$ s, $V_R$ = 50 V, dV/dt = 20 V/ $\mu$ s, gate bias: 0 V 25 $\Omega$ , $t_p$ = 500 $\mu$ s	110	μs

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T <sub>J</sub> = 125 °C exponential to 67 % rated V <sub>DRM</sub>	500	V/µs
Maximum peak reverse and off-state leakage current	I <sub>RRM</sub> , I <sub>DRM</sub>	T <sub>J</sub> = 125 °C rated V <sub>DRM</sub> /V <sub>RRM</sub> applied	15	mA



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TRIGGERING					
PARAMETER	SYMBOL		TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P <sub>GM</sub>	$T_J = T_J \text{ maximum}$	$t_p \le 5 \text{ ms}$	12	W
Maximum average gate power	P <sub>G(AV)</sub>	$T_J = T_J \text{ maximum}$	f = 50 Hz, d% = 50	3	VV
Maximum peak positive gate current	I <sub>GM</sub>			3	Α
Maximum peak positive gate voltage	+ V <sub>GM</sub>	$T_J = T_J \text{ maximum}$	$T_J = T_J$ maximum, $t_p \le 5$ ms		V
Maximum peak negative gate voltage	- V <sub>GM</sub>			10	
	I <sub>GT</sub>	T <sub>J</sub> = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 6 V anode	270	mA V
Maximum DC gate current required to trigger		T <sub>J</sub> = 25 °C		120	
		T <sub>J</sub> = 125 °C		60	
		T <sub>J</sub> = - 40 °C		3.5	
Maximum DC gate voltage required to trigger	V <sub>GT</sub>	T <sub>J</sub> = 25 °C	to cathode applied	2.5	
		T <sub>J</sub> = 125 °C		1.5	
DC gate current not to trigger	$I_{GD}$		Maximum gate current/voltage not to	6	mA
DC gate voltage not to trigger	$V_{GD}$	$T_J = T_J$ maximum trigger is the maximum value which will not trigger any unit with rated $V_{DRM}$ anode to cathode applied		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	TJ		- 40 to 125	°C
Maximum storage temperature range	T <sub>Stg</sub>		- 40 to 150	
Maximum thermal resistance, junction to case	R <sub>thJC</sub>	DC operation	0.30	K/W
Maximum thermal resistance, case to heatsink	R <sub>thCS</sub>	Mounting surface, smooth, flat and greased	0.1	IV/VV
Mounting torque + 10.04		Non-lubricated threads	15.5 (137)	N⋅m
Mounting torque, ± 10 %		Lubricated threads	14 (120)	(lbf·in)
Approximate weight			130	g
Case style		See dimensions - link at the end of datasheet	TO-94 (TO	-209AC)

∆R <sub>thJC</sub> CONDUCTIO	N			
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.042	0.030		
120°	0.050	0.052		
90°	0.064	0.070	$T_J = T_J \text{ maximum}$	K/W
60°	0.095	0.100		
30°	0.164	0.165		

#### Note

• The table above shows the increment of thermal resistance RthJC when devices operate at different conduction angles than DC

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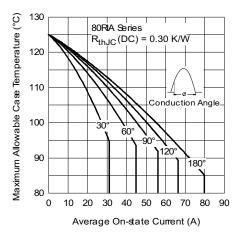


Fig. 1 - Current Ratings Characteristics

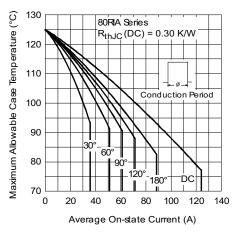


Fig. 2 - Current Ratings Characteristics

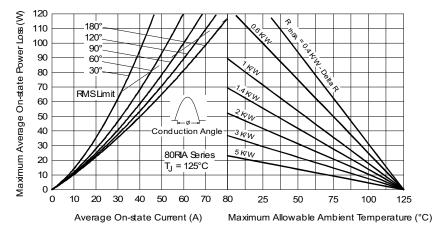


Fig. 3 - On-State Power Loss Characteristics

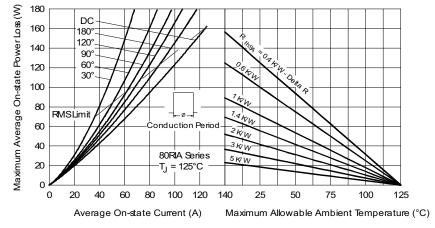


Fig. 4 - On-State Power Loss Characteristics

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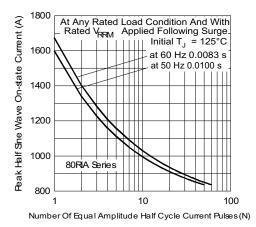


Fig. 5 - Maximum Non-Repetitive Surge Current

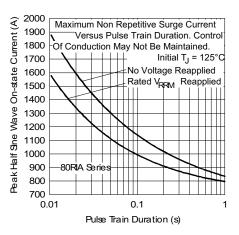


Fig. 6 - Maximum Non-Repetitive Surge Current

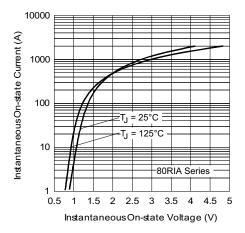


Fig. 7 - On-State Voltage Drop Characteristics

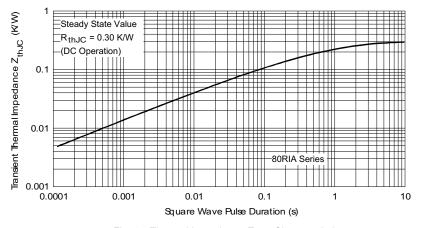


Fig. 8 - Thermal Impedance Z<sub>thJC</sub> Characteristics

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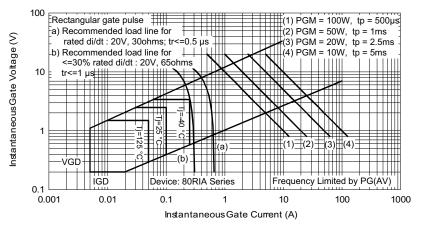
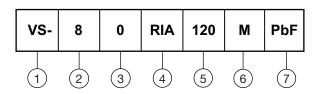


Fig. 9 - Gate Characteristics

#### **ORDERING INFORMATION TABLE**

**Device code** 



- Vishay Semiconductors product
- I<sub>TAV</sub> x 10 A
- 0 = eyelet terminals (gate and auxiliary cathode leads)
  - 1 = fast-on terminals (gate and auxiliary cathode leads)
  - 2 = flag terminals (gate and auxiliary cathode terminals)
- RIA = essential part number
- Voltage code x 100 = V<sub>RRM</sub> (see Voltage Ratings table)
- None = stud base 1/2"-20UNF- 2 A threads
- M = stud base metric threads M12 x 1.75 E 6
- 7 None = standard production
  - PbF = lead (Pb)-free

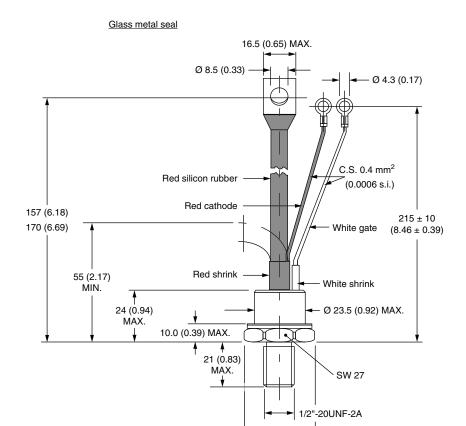
LINKS TO RELAT	ED DOCUMENTS
Dimensions	www.vishay.com/doc?95362



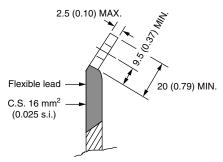
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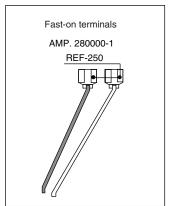
## TO-209AC (TO-94) for 80RIA Series

#### **DIMENSIONS** in millimeters (inches)



29.5 (1.16) MAX.





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