## SQD35N05-26L



**Vishay Siliconix** 

# Automotive N-Channel 55 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	55			
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS}$ = 10 V	0.020			
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS}$ = 4.5 V	0.026			
I <sub>D</sub> (A)	30			
Configuration	Single			

#### 

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21
  Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- AEC-Q101 Qualified<sup>d</sup>
- Compliant to RoHS Directive 2002/95/EC



ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD35N05-26L-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub>	= 25 °C, unles	s otherwise noted	ł)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	55		
Gate-Source Voltage		V <sub>GS</sub> ± 20		V	
Continuous Drain Current	T <sub>C</sub> = 25 °C <sup>a</sup>	- I <sub>D</sub> -	30		
	T <sub>C</sub> = 125 °C		19		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	30	А	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	120		
Single Pulse Avalanche Energy	L = 0.1 mH	I <sub>AS</sub>	20		
Single Pulse Avalanche Current	L = 0.1 mm	E <sub>AS</sub>	20	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	D	50	W	
	T <sub>C</sub> = 125 °C	P <sub>D</sub>	16		
Operating Junction and Storage Temperature Rang	je	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	60	°C/W	
lunction-to-Case (Drain)		R <sub>thJC</sub>	3	C/W	

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%.$
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.

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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	•					-		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$		55	-	-	v	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	: V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	2	2.5	v	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	± 100	nA	
Zero Gate Voltage Drain Current		$V_{GS} = 0 V$	V <sub>DS</sub> = 55 V	-	-	1		
	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS} = 55 \text{ V}, \text{ T}_{\text{J}} = 125 ^{\circ}\text{C}$	-	-	50	μA	
		$V_{GS} = 0 V$	$V_{DS}$ = 55 V, $T_{J}$ = 175 °C	-	-	250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 5 V$	$V_{DS} \geq 5 \ V$	30	-	-	А	
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = 10 V$	I <sub>D</sub> = 20 A	-	0.016	0.020	Ω	
	Brack	$V_{GS} = 10 V$	$I_D = 20 \text{ A}, T_J = 125 ^\circ\text{C}$	-	-	0.035		
	R <sub>DS(on)</sub>	$V_{GS} = 10 V$	$I_D = 20 \text{ A},  \text{T}_\text{J} = 175 \ ^\circ\text{C}$	-	-	0.043		
		$V_{GS} = 4.5 V$	I <sub>D</sub> = 15 A	-	0.021	0.026		
Forward Transconductanceb	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		-	34	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>		V <sub>DS</sub> = 25 V, f = 1 MHz	-	938	1175	pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$		-	203	255		
Reverse Transfer Capacitance	C <sub>rss</sub>			-	86	110		
Total Gate Charge <sup>c</sup>	Qg		$V_{DS} = 25 \text{ V}, \text{ I}_{D} = 35 \text{ A}$	-	12	18		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 5 V$		-	4.1	-	nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	4.8	-		
Gate Resistance	Rg	f = 1 MHz		1.3	2.6	4	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	7	11		
Rise Time <sup>c</sup>	t <sub>r</sub>	V <sub>DD</sub> =	$V_{DD} = 25 \text{ V}, \text{ R}_{\text{I}} = 0.71 \Omega$		10	15	- ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 35$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$		-	18	27		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	5	8		
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>	•			•			
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	120	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 80 A, V <sub>GS</sub> = 0 V			1.2	1.5	V	

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

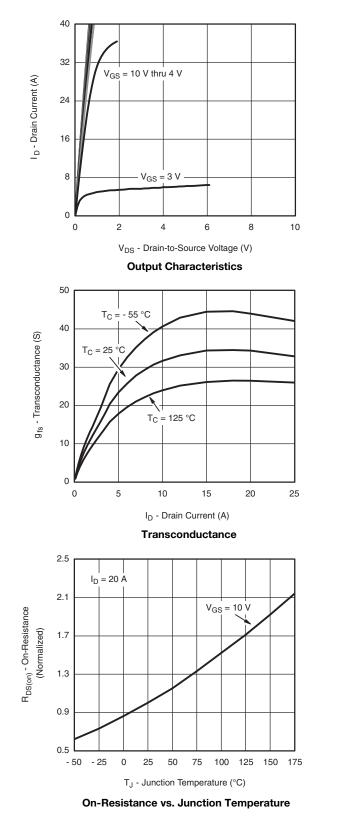
c. Independent of operating temperature.

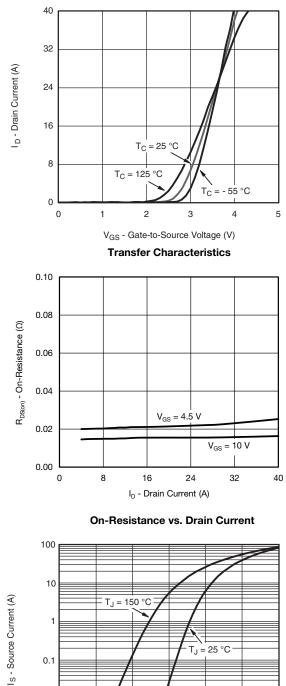
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

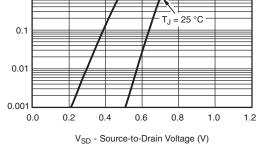


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### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)







Source Drain Diode Forward Voltage

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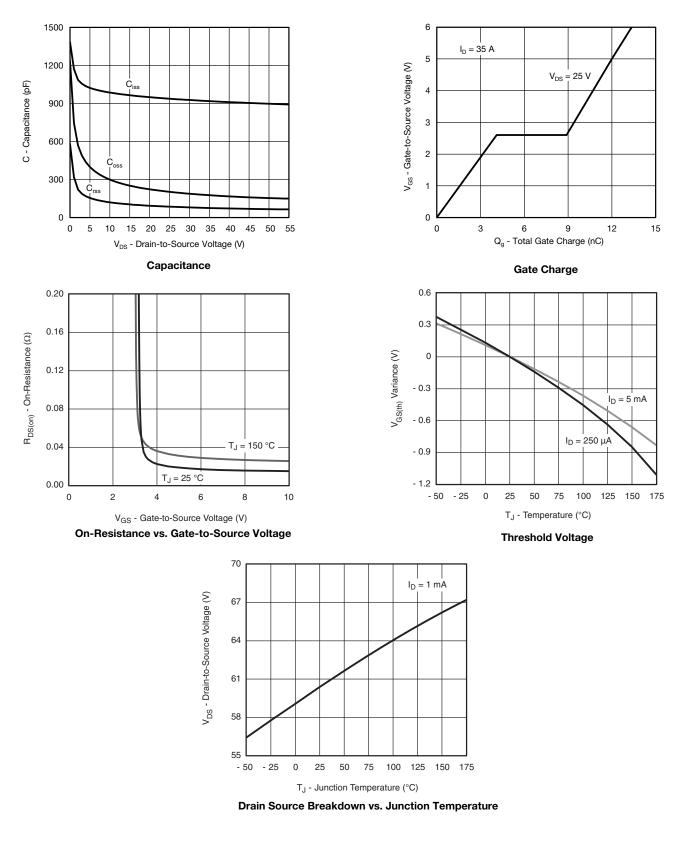
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### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)

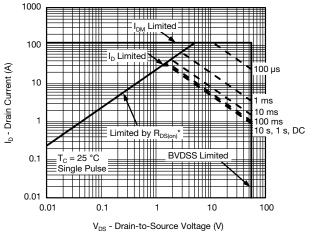


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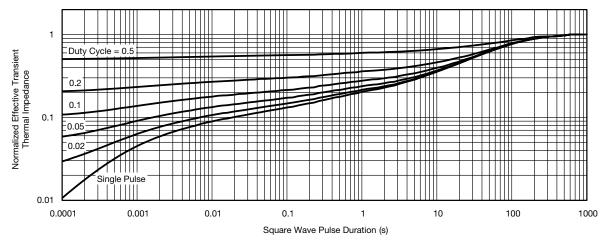
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### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area



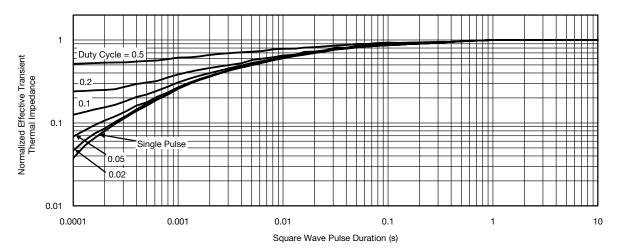
Normalized Thermal Transient Impedance, Junction-to-Ambient



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### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

• The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?68839">www.vishay.com/ppg?68839</a>.

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