




Power MOSFET, 38 A



SOT-227

FEATURES

- Fully isolated package
- Easy to use and parallel
- Low on-resistance
- Dynamic dV/dt rating
- Fully avalanche rated
- Simple drive requirements
- Low drain to case capacitance
- Low internal inductance
- UL approved file E78996 
- Designed for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

PRODUCT SUMMARY	
V_{DSS}	500 V
$R_{DS(on)}$	0.13 Ω
I_D	38 A
Type	Modules - MOSFET
Package	SOT-227

DESCRIPTION

Third Generation Power MOSFETs from Vishay Semiconductors provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-227 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 500 W. The low thermal resistance of the SOT-227 contribute to its wide acceptance throughout the industry.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current at V_{GS} 10 V	I_D	$T_C = 25\text{ }^\circ\text{C}$	38	A
		$T_C = 100\text{ }^\circ\text{C}$	24	
Pulsed drain current	$I_{DM}^{(1)}$		150	
Power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	500	W
Linear derating factor			4.0	W/ $^\circ\text{C}$
Gate to source voltage	V_{GS}		± 20	V
Single pulse avalanche energy	$E_{AS}^{(2)}$		580	mJ
Avalanche current	$I_{AR}^{(1)}$		38	A
Repetitive avalanche energy	$E_{AR}^{(1)}$		50	mJ
Peak diode recovery dV/dt	dV/dt ⁽³⁾		10	V/ns
Operating junction and storage temperature range	T_J, T_{Stg}		- 55 to + 150	$^\circ\text{C}$
Insulation withstand voltage (AC-RMS)	V_{ISO}		2.5	kV
Mounting torque		M4 screw	1.3	Nm

Notes

- (1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- (2) Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.80\text{ mH}$, $R_g = 25\text{ }^\circ\Omega$, $I_{AS} = 38\text{ A}$ (see fig. 12)
- (3) $I_{SD} \leq 38\text{ A}$, $dI/dt \leq 410\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150\text{ }^\circ\text{C}$

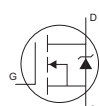


THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Junction and storage temperature range	T_J, T_{Stg}		- 55	-	150	°C
Junction to case	R_{thJC}		-	-	0.25	°C/W
Case to heatsink	R_{thCS}	Flat, greased surface	-	0.05	-	
Weight			-	30	-	g
Mounting torque			-	-	1.3	Nm
Case style		SOT-227				

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ °C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$	500	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to $25\text{ °C}, I_D = 1\text{ mA}$	-	0.66	-	V/°C
Static drain to source on-resistance	$R_{DS(on)}^{(1)}$	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}$	-	-	0.13	Ω
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Forward transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 23\text{ A}$	22	-	-	S
Drain to source leakage current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	-	500	
Gate to source forward leakage	I_{GSS}	$V_{GS} = 20\text{ V}$	-	-	200	nA
Gate to source reverse leakage		$V_{GS} = -20\text{ V}$	-	-	- 200	
Total gate charge	Q_g	$I_D = 38\text{ A}$ $V_{DS} = 400\text{ V}$ $V_{GS} = 10\text{ V}$; see fig. 6 and 13 ⁽¹⁾	-	280	420	nC
Gate to source charge	Q_{gs}		-	37	55	
Gate to drain ("Miller") charge	Q_{gd}		-	150	220	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$ $I_D = 38\text{ A}$ $R_g = 10\text{ }\Omega$ (interval) $R_D = 8\text{ }\Omega$, see fig. 10 ⁽¹⁾	-	42	-	ns
Rise time	t_r		-	340	-	
Turn-off delay time	$t_{d(off)}$		-	200	-	
Fall time	t_f		-	330	-	
Internal source inductance	L_S	Between lead, and center of die contact	-	5.0	-	nH
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$, see fig. 5	-	6900	-	pF
Output capacitance	C_{oss}		-	1600	-	
Reverse transfer capacitance	C_{rss}		-	580	-	

Note

⁽¹⁾ Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

SOURCE-DRAIN RATINGS AND CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous source current (body diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	38	A
Pulsed source current (body diode)	$I_{SM}^{(1)}$		-	-	150	
Diode forward voltage	$V_{SD}^{(2)}$	$T_J = 25\text{ °C}, I_S = 38\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ °C}, I_F = 38\text{ A}; di/dt = 100\text{ A}/\mu\text{s}^{(2)}$	-	830	1300	ns
Reverse recovery charge	Q_{rr}		-	15	22	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes

⁽¹⁾ Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

⁽²⁾ Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

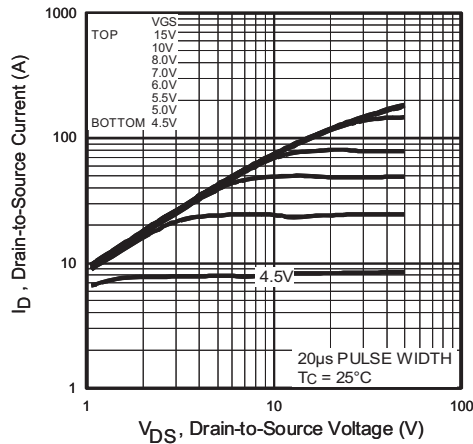


Fig. 1 - Typical Output Characteristics

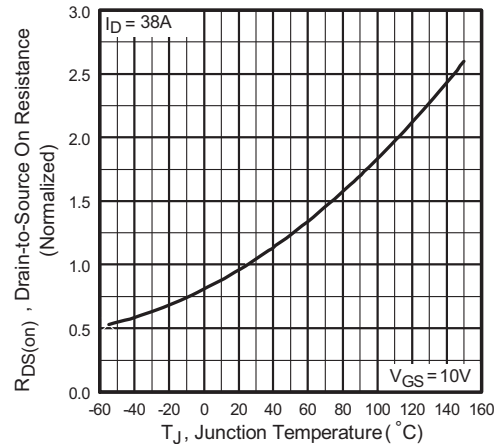


Fig. 4 - Normalized On-Resistance vs. Temperature

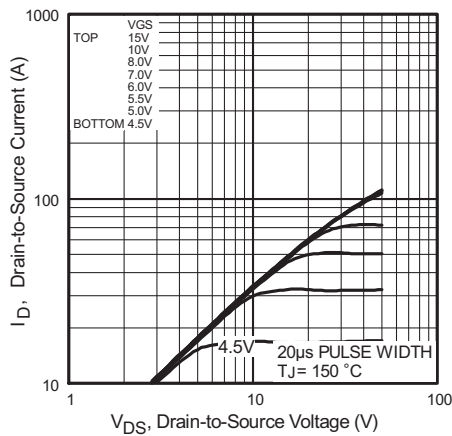


Fig. 2 - Typical Output Characteristics

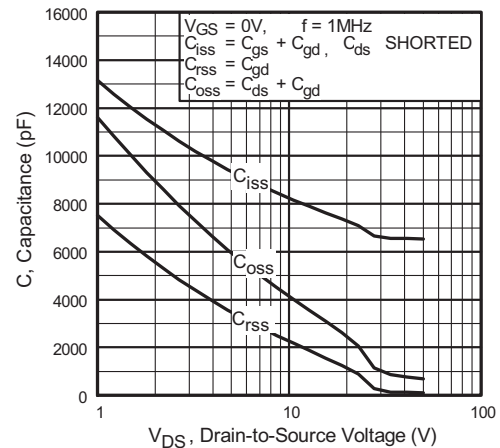


Fig. 5 - Typical Capacitance vs. Drain to Source Voltage

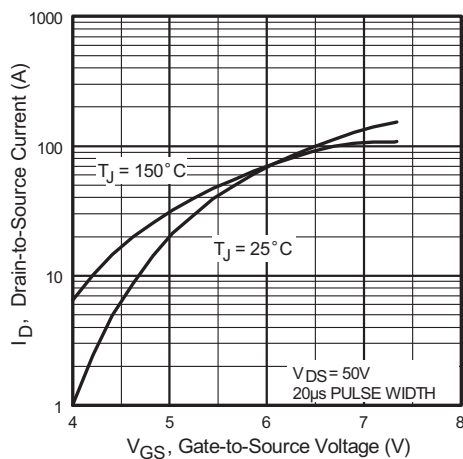


Fig. 3 - Typical Transfer Characteristics

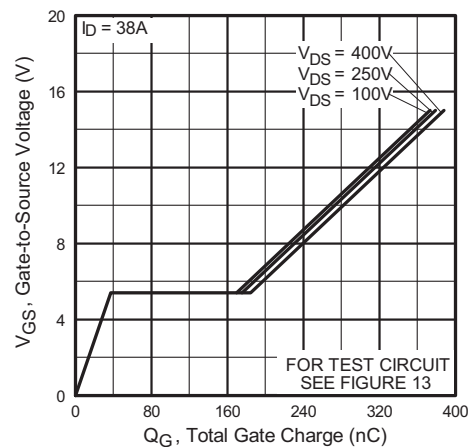


Fig. 6 - Typical Gate Charge vs. Gate to Source Voltage

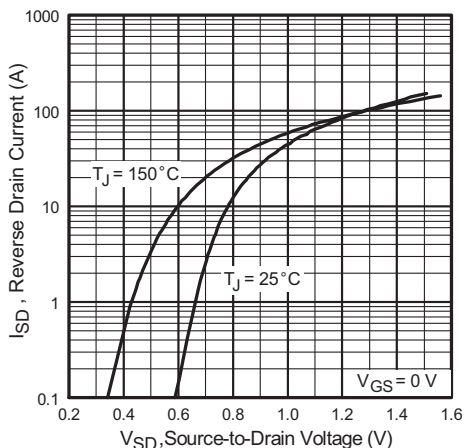


Fig. 7 - Typical Source Drain Diode Forward Voltage

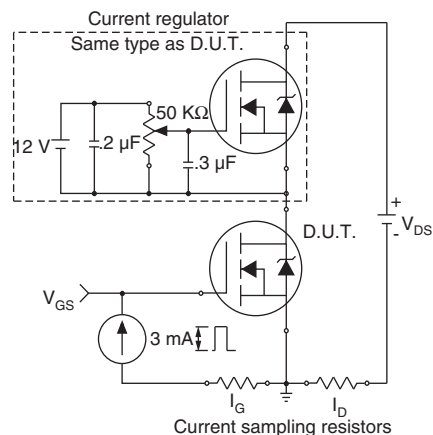


Fig. 10 - Gate Charge Test Circuit

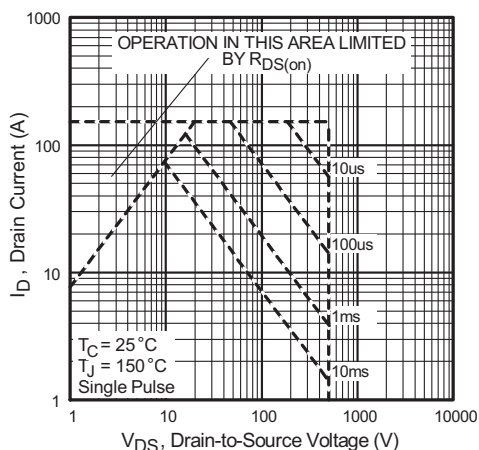


Fig. 8 - Maximum Safe Operating Area

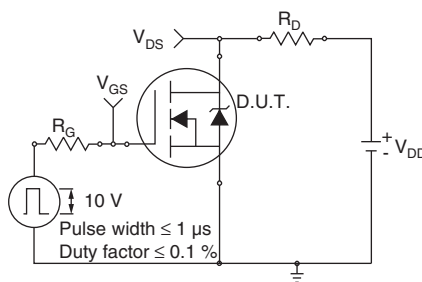


Fig. 11 - Switching Time Test Circuit

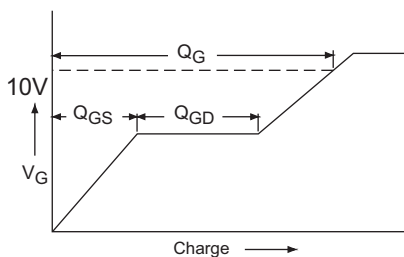


Fig. 9 - Basic Gate Charge Waveform

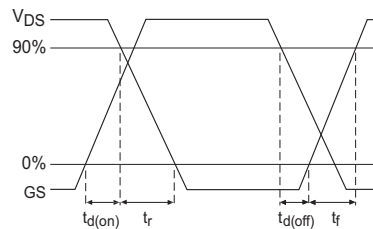


Fig. 12 - Switching Time Waveforms

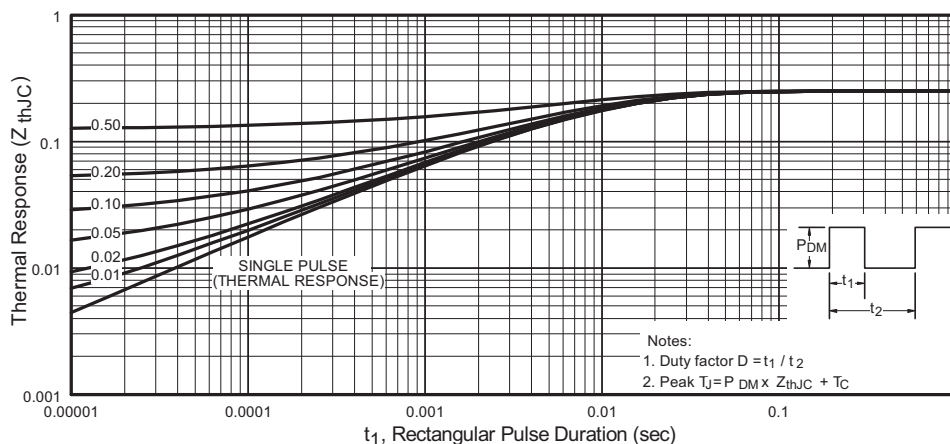


Fig. 13 - Maximum Effective Transient Thermal Impedance, Junction to Case

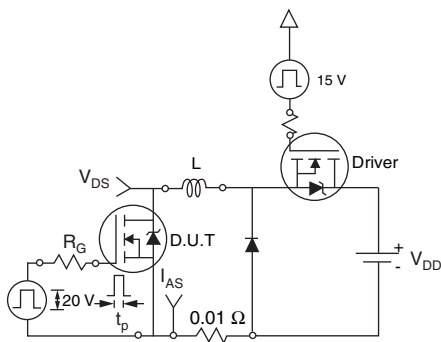


Fig. 14 - Unclamped Inductive Test Circuit

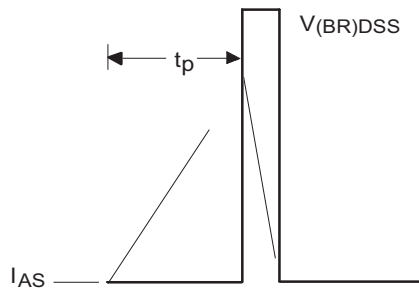


Fig. 15 - Unclamped Inductive Waveforms

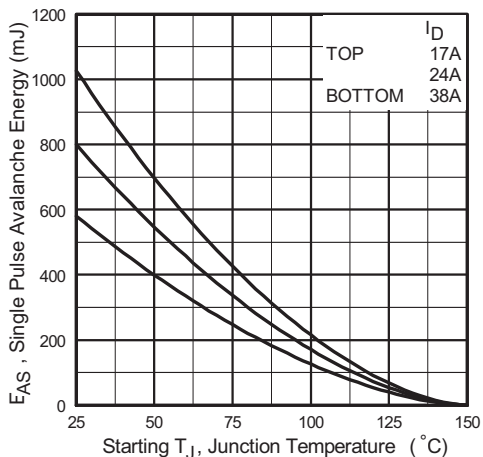


Fig. 16 - Maximum Avalanche Energy vs. Drain Current

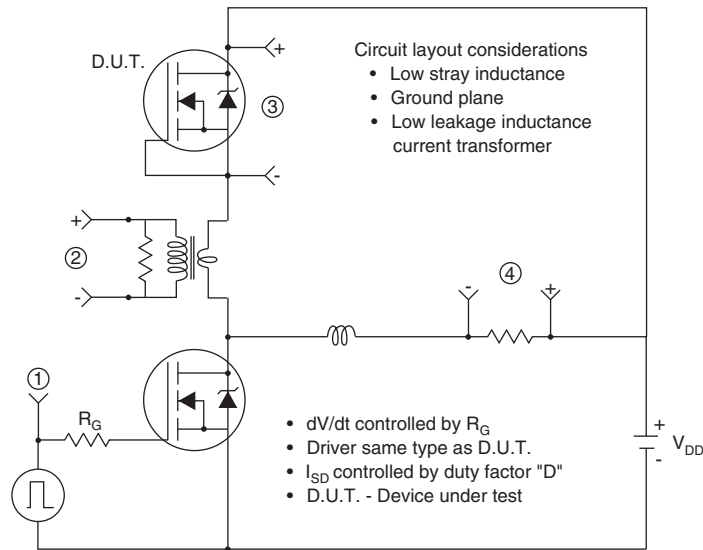
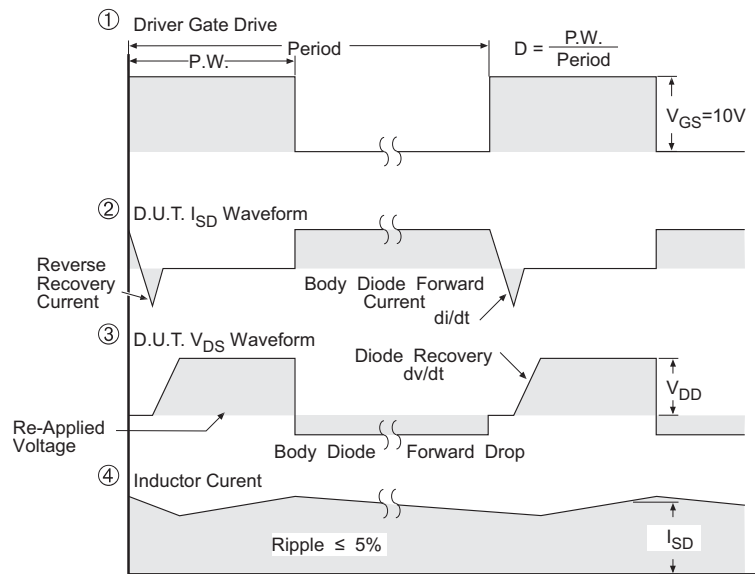


Fig. 17 - Peak Diode Recovery dv/dt Test Circuit

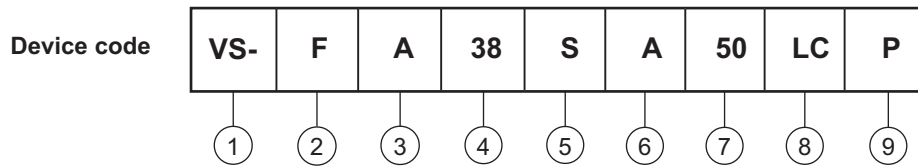


* $V_{GS} = 5V$ for Logic Level Devices

Fig. 18 - For N-Channel Power MOSFETs



ORDERING INFORMATION TABLE



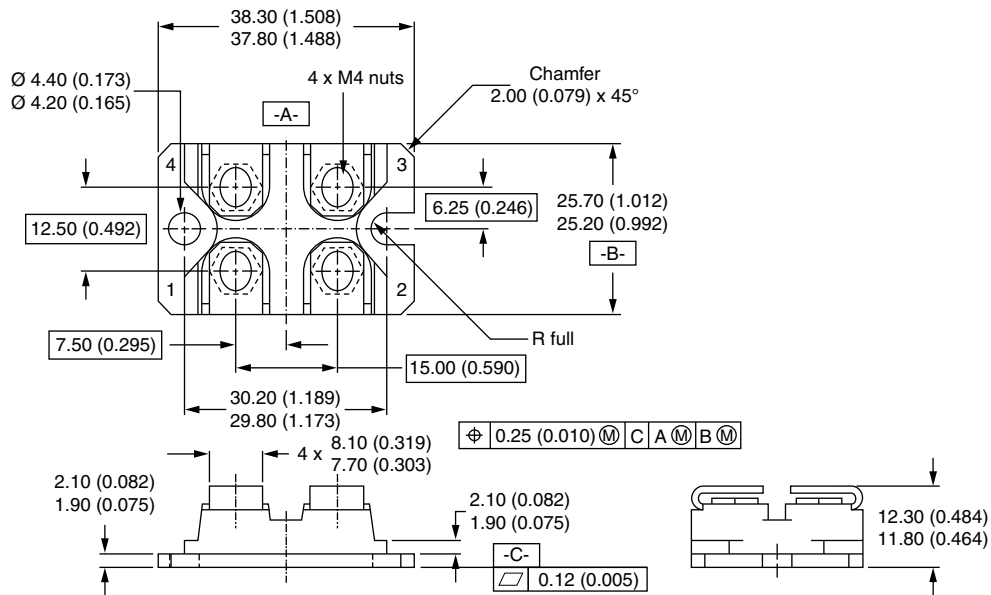
- 1** - Vishay Semiconductors product
- 2** - Power MOSFET
- 3** - Generation 3, MOSFET silicon, DBC construction
- 4** - Current rating (38 = 38 A)
- 5** - Single switch (see Circuit Configuration table)
- 6** - SOT-227
- 7** - Voltage rating (50 = 500 V)
- 8** - Low charge
- 9** - P = Lead (Pb)-free

CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Single switch no diode	S	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95036
Packaging information	www.vishay.com/doc?95037

SOT-227

DIMENSIONS in millimeters (inches)



Notes

- Dimensioning and tolerancing per ANSI Y14.5M-1982
- Controlling dimension: millimeter



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