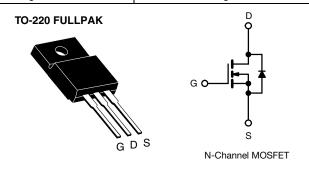


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Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	600			
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	0.75		
Q _g max. (nC)	49			
Q _{gs} (nC)	13			
Q _{gd} (nC)	20			
Configuration	Single			



FEATURES

 \bullet Low gate charge \mathbf{Q}_g results in simple drive requirement



Improved gate, avalanche and dynamic dV/dt ruggedness

RoHS*

- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- · High speed power switching
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s, f = 60 Hz)

TYPICAL SMPS TOPOLOGIES

- Single transistor forward
- · Active clamped forward

ORDERING INFORMATION			
Package	TO-220 FULLPAK		
Lead (Pb)-free	IRFIB6N60APbF		
	SiHFIB6N60A-E3		
SnPb	IRFIB6N60A		
	SiHFIB6N60A		

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	600	V	
Gate-Source Voltage			V_{GS}	± 30	V	
Continuous Drain Current	V _{GS} at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$		5.5		
	VGS at 10 V	T _C = 100 °C	I _D	3.5		
Pulsed Drain Current ^a			I _{DM}	37		
Linear Derating Factor				0.48	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	290	mJ	
Repetitive Avalanche Current ^a			I _{AR}	9.2	А	
Repetitive Avalanche Energy ^a			E _{AR}	6.0	mJ	
Maximum Power Dissipation	T _C =	25 °C	P_{D}	60	W	
Peak Diode Recovery dV/dt ^c			dV/dt	5.0	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	00	
Soldering Recommendations (Peak temperature) d	for 10 s		-	300	°C	
Mounting Torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Starting T_J = 25 °C, L = 6.8 mH, R_G = 25 Ω , I_{AS} = 9.2 A (see fig. 12).
- c. $I_{SD} \le 9.2$ A, $dI/dt \le 50$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.
- d. 1.6 mm from case.



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.1	G/ VV	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	600	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I _D = 1 mA ^d		-	660	-	mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} :	V _{DS} = V _{GS} , I _D = 250 μA		-	4.0	V
Gate-Source Leakage	I _{GSS}		$V_{GS} = \pm 30 \text{ V}$		-	± 100	nA
Zero Gate Voltage Drain Current	less	V _{DS} = 600 V, V _{GS} = 0 V		ı	-	25	μA
Zero date voltage Drain Gurrent	I _{DSS}	V _{DS} = 480 \	/, V _{GS} = 0 V, T _J = 125 °C	-	-	250	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	$I_D = 3.3 \text{ A}^{\text{ b}}$	ı	-	0.75	Ω
Forward Transconductance	9 _{fs}	V_{DS}	V _{DS} = 25 V, I _D = 5.5 A		-	-	S
Dynamic							
Input Capacitance	C_{iss}	V _{GS} = 0 V,		ı	1400	-	
Output Capacitance	C_{oss}		$V_{DS} = 25 \text{ V},$		180	-	
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz, see fig. 5		-	7.1	-	
Output Capacitance	0		$V_{DS} = 1.0 \text{ V}, f = 1.0 \text{ MHz}$	ı	1957	-	pF
Output Oapacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = 480 \text{ V}, f = 1.0 \text{ MHz}$	-	49	-	
Effective Output Capacitance	Coss eff.		$V_{DS} = 0 \text{ V to } 480 \text{ V}^{\text{ c}}$	-	96	-	
Total Gate Charge	Q_g		$V_{GS} = 10 \text{ V}$ $I_D = 9.2 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 b	ı	-	49	nC
Gate-Source Charge	Q_gs	V _{GS} = 10 V		-	-	13	
Gate-Drain Charge	Q_{gd}			-	-	20	
Turn-On Delay Time	t _{d(on)}			-	13	-	
Rise Time	t _r	V_{DD} = 300 V, I_{D} = 9.2 A, R_{G} = 9.1 Ω , R_{D} = 35.5 Ω , see fig. 10 b		-	25	-	ns
Turn-Off Delay Time	t _{d(off)}			-	30	-	
Fall Time	t _f			-	22	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain		0.5	-	3.2	Ω
Drain-Source Body Diode Characteristic	es						
Continuous Source-Drain Diode Current	Is	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.5	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	37	- A
Body Diode Voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 9.2 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	$T_{\rm J} = 25~{\rm ^{\circ}C}, I_{\rm F} = 9.2~{\rm A}, dI/dt = 100~{\rm A/\mu s}^{\rm b}$		-	530	800	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	3.0	4.4	μC
Forward Turn-On Time	t _{on}	Intrinsic tu	n-on is dominated by L _S and L _D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%.$
- c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
- d. t = 60 s, f = 60 Hz.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

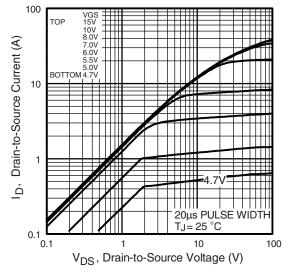


Fig. 1 - Typical Output Characteristics

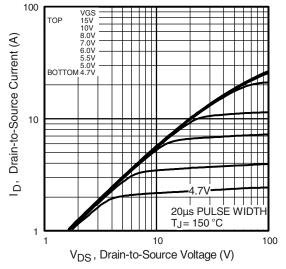


Fig. 2 - Typical Output Characteristics

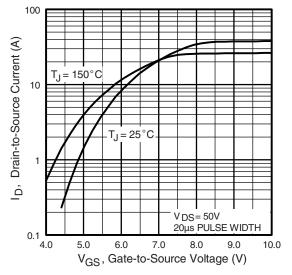


Fig. 3 - Typical Transfer Characteristics

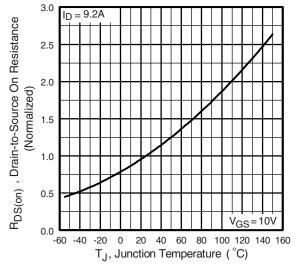


Fig. 4 - Normalized On-Resistance vs. Temperature



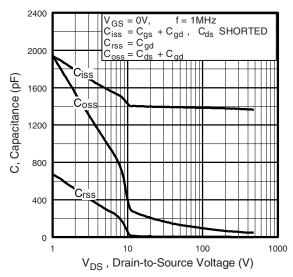


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

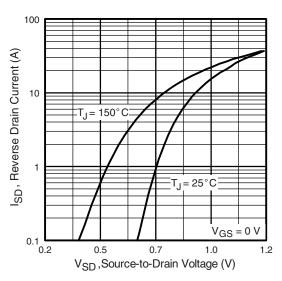


Fig. 7 - Typical Source-Drain Diode Forward Voltage

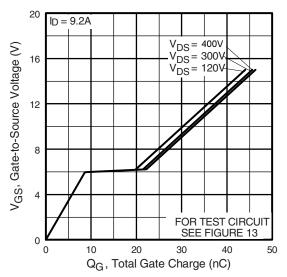


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

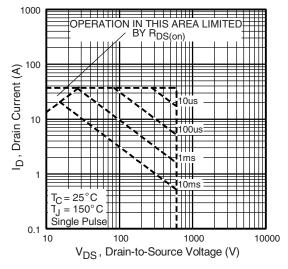


Fig. 8 - Maximum Safe Operating Area

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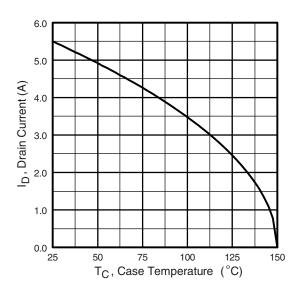


Fig. 9 - Maximum Drain Current vs. Case Temperature

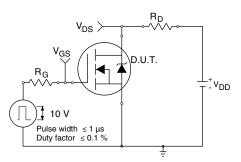


Fig. 10a - Switching Time Test Circuit

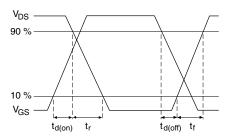


Fig. 10b - Switching Time Waveforms

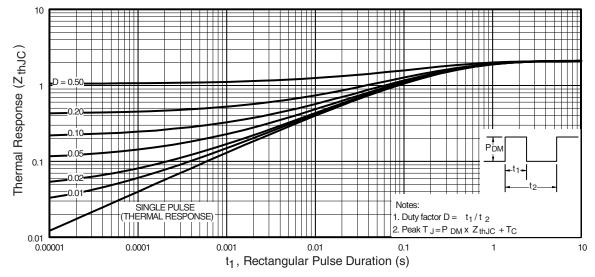


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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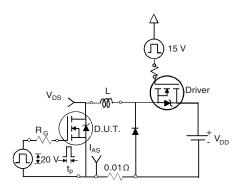


Fig. 12a - Unclamped Inductive Test Circuit

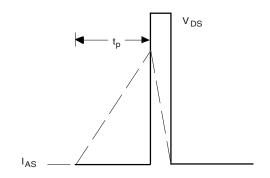


Fig. 12b - Unclamped Inductive Waveforms

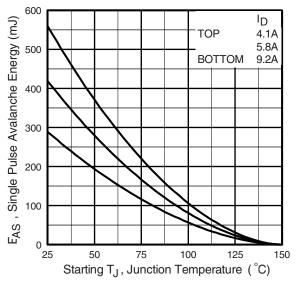


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

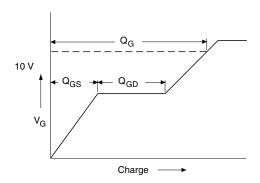


Fig. 13a - Basic Gate Charge Waveform

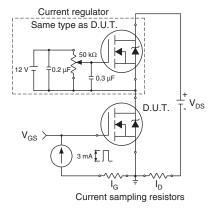
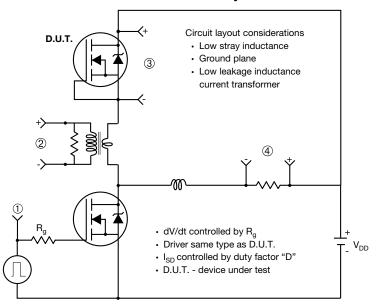


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



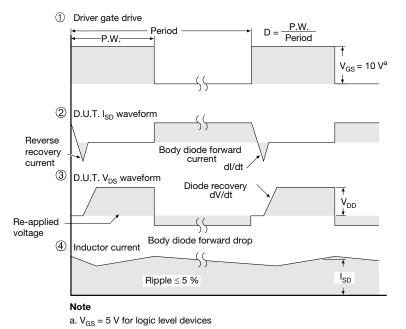


Fig. 14 - For N-Channel

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