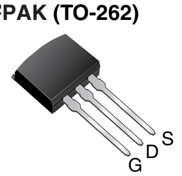
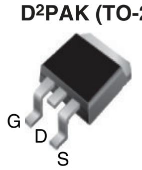
Power MOSFET

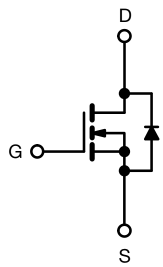
PRODUCT SUMMARY		
V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.18
Q_g max. (nC)	70	
Q_{gs} (nC)	13	
Q_{gd} (nC)	39	
Configuration	Single	

I[2]PAK (TO-262)



D[2]PAK (TO-263)





N-Channel MOSFET

FEATURES

- Surface mount
- Low-profile through-hole
- Available in tape and reel
- Dynamic dV/dt rating
- 150 °C operating temperature
- Fast switching
- Fully avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available
HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combinations of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The D[2]PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the last lowest possible on-resistance in any existing surface mount package. The D[2]PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (SiHF640L) is available for low-profile applications.

ORDERING INFORMATION				
Package	D[2]PAK (TO-263)	D[2]PAK (TO-263)	D[2]PAK (TO-263)	I[2]PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF640S-GE3	SiHF640STRL-GE3 [a]	SiHF640STRR-GE3 [a]	SiHF640L-GE3
Lead (Pb)-free	IRF640SPbF	IRF640STRLPbF [a]	IRF640STRRPbF [a]	-

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	18	A
		T_C = 100 °C		11	
Pulsed Drain Current [a, e]			I_{DM}	72	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy [b, e]			E_{AS}	580	mJ
Avalanche Current [a]			I_{AR}	18	A
Repetitive Avalanche Energy [a]			E_{AR}	13	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	130	W
	T_A = 25 °C			3.1	
Peak Diode Recovery dV/dt [c, e]			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) [d]	for 10 s			300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.7 mH, R_g = 25 Ω, I_{AS} = 18 A (see fig. 12).
c. $I_{SD} \leq 18$ A, dI/dt ≤ 150 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
d. 1.6 mm from case.
e. Uses IRF640, SiHF640 data and test conditions.

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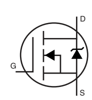
THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient (PCB mounted, steady-state) [a]	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA [c]		-	0.29	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 11 A [b]	-	-	0.18	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 11 A [d]		6.7	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5 [d]		-	1300	-	pF
Output Capacitance	C_{oss}			-	430	-	
Reverse Transfer Capacitance	C_{rss}			-	130	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 18 A, V_{DS} = 160 V, see fig. 6 and 13 [b, c]	-	-	70	nC
Gate-Source Charge	Q_{gs}			-	-	13	
Gate-Drain Charge	Q_{gd}			-	-	39	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 18 A, R_g = 9.1 Ω, R_D = 5.4 Ω, see fig. 10 [b, c]		-	14	-	ns
Rise Time	t_r			-	51	-	
Turn-Off Delay Time	$t_{d(off)}$			-	45	-	
Fall Time	t_f			-	36	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain		0.5	-	3.6	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	18	A
Pulsed Diode Forward Current [a]	I_{SM}			-	-	72	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 18 A, V_{GS} = 0 V [b]		-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 18 A, dI/dt = 100 A/µs [b, c]		-	300	610	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.4	7.1	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

c. Uses IRF640/SiHF640 data and test conditions.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

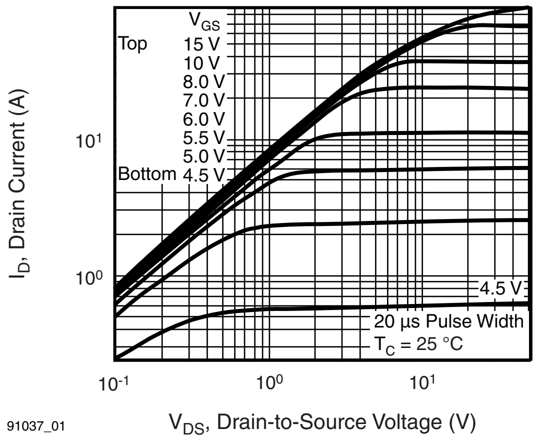

Fig. 1 - Typical Output Characteristics, T_J = 25 °C

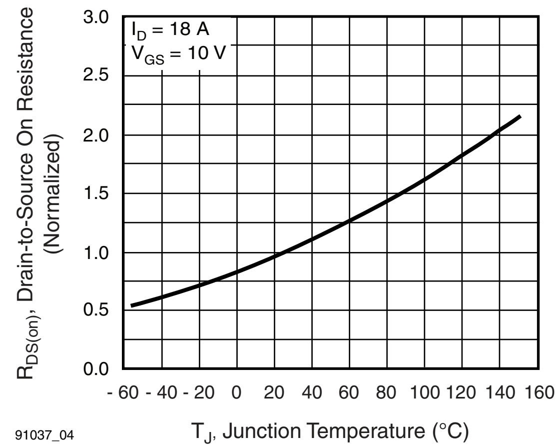

Fig. 4 - Normalized On-Resistance vs. Temperature

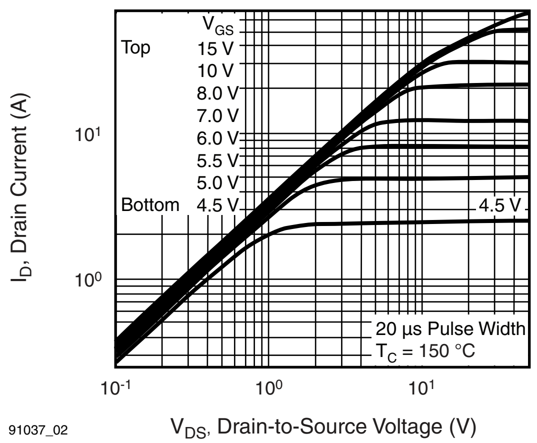

Fig. 2 - Typical Output Characteristics, T_J = 175 °C

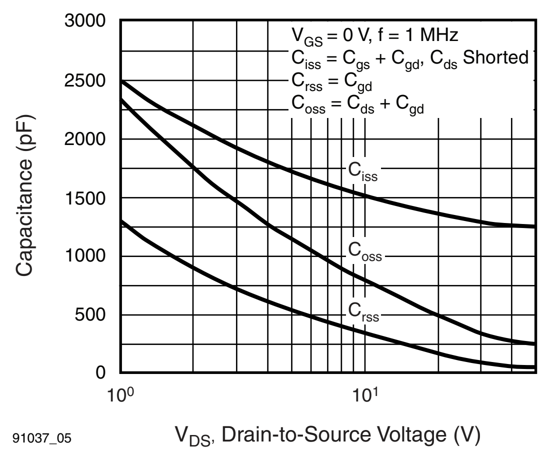

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

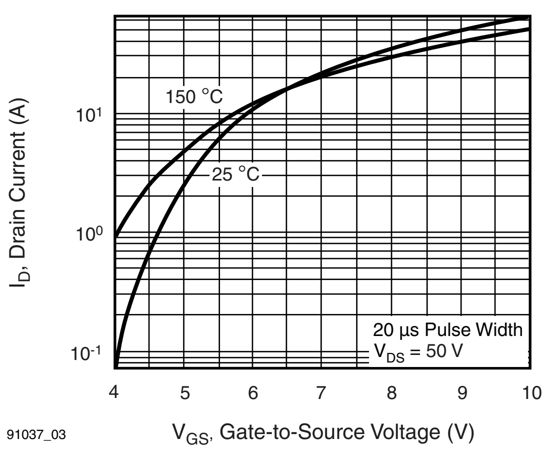

Fig. 3 - Typical Transfer Characteristics

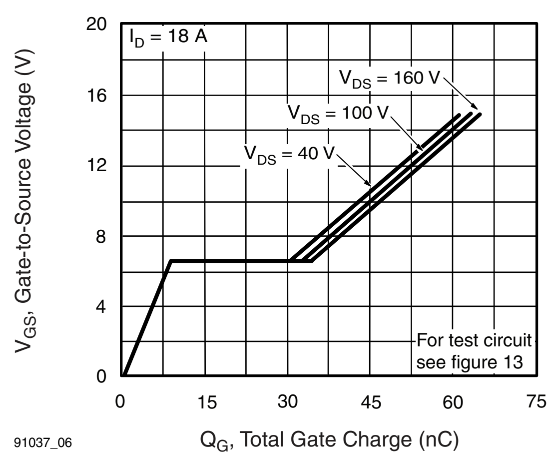

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

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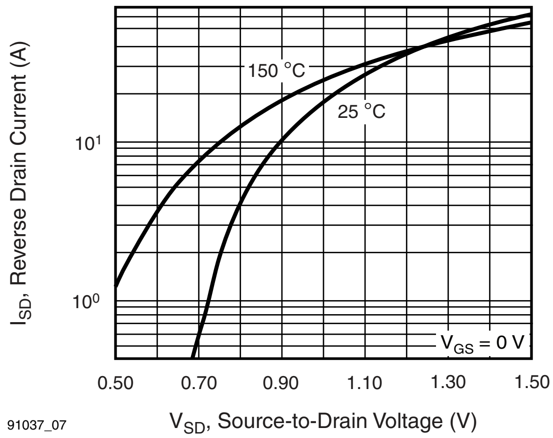

Fig. 7 - Typical Source-Drain Diode Forward Voltage

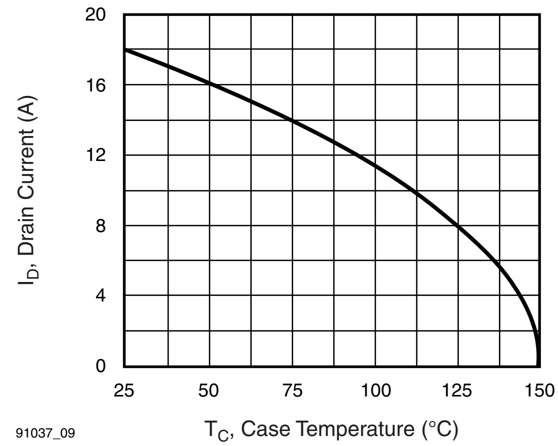

Fig. 9 - Maximum Drain Current vs. Case Temperature

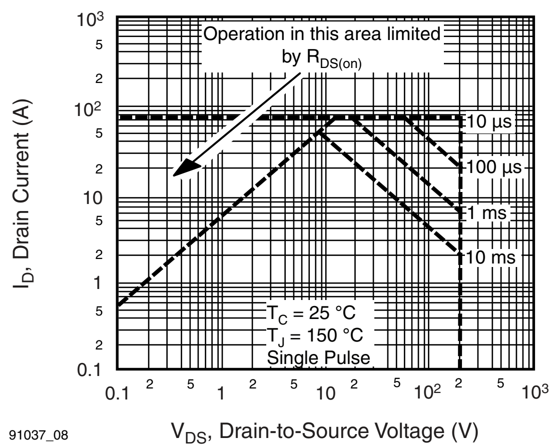

Fig. 8 - Maximum Safe Operating Area

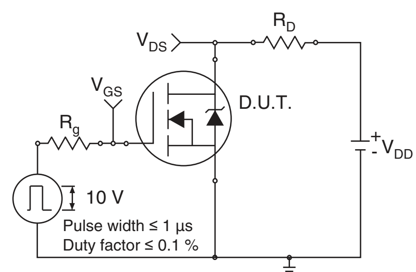

Fig. 10a - Switching Time Test Circuit

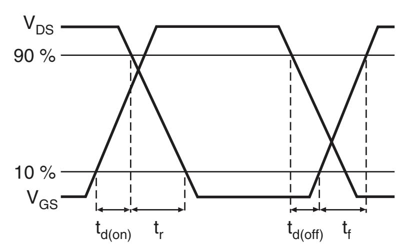

Fig. 10b - Switching Time Waveforms

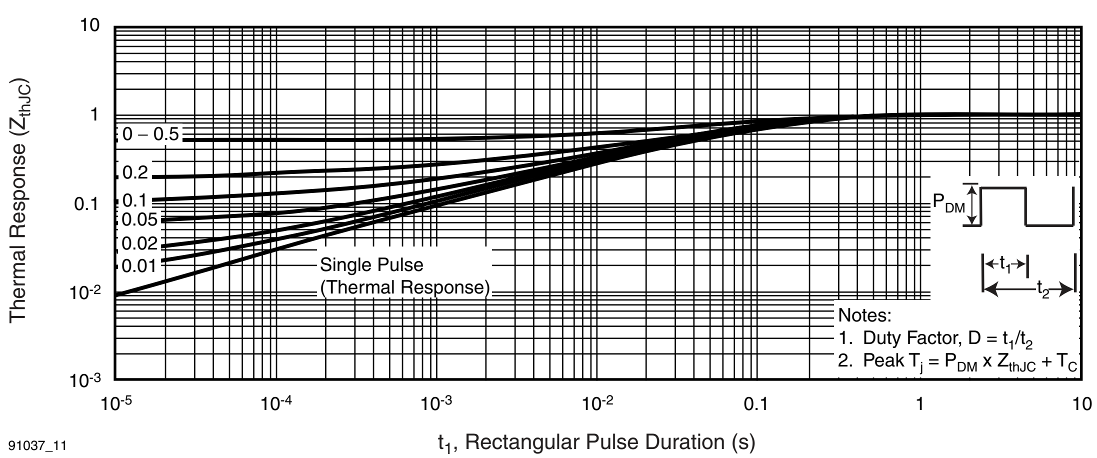

Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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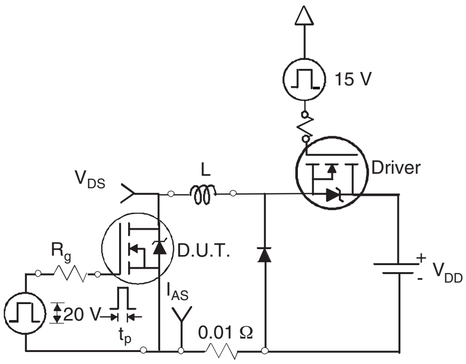

Fig. 12a - Unclamped Inductive Test Circuit

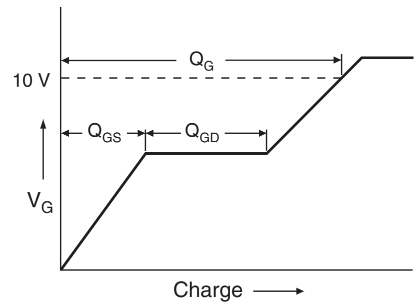

Fig. 13a - Basic Gate Charge Waveform

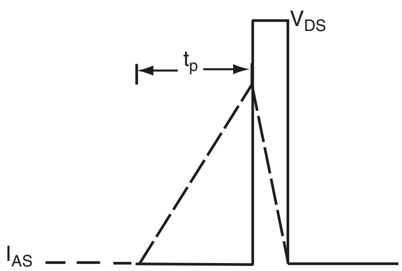

Fig. 12b - Unclamped Inductive Waveforms

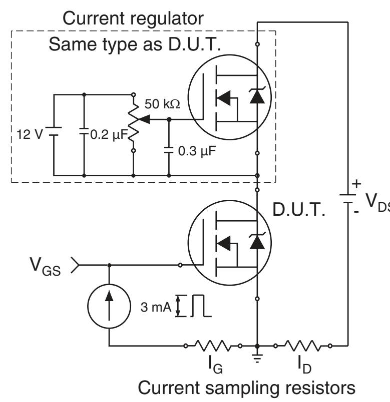

Fig. 13b - Gate Charge Test Circuit

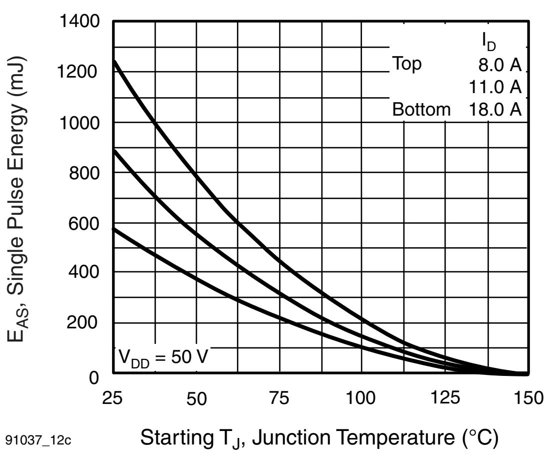

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

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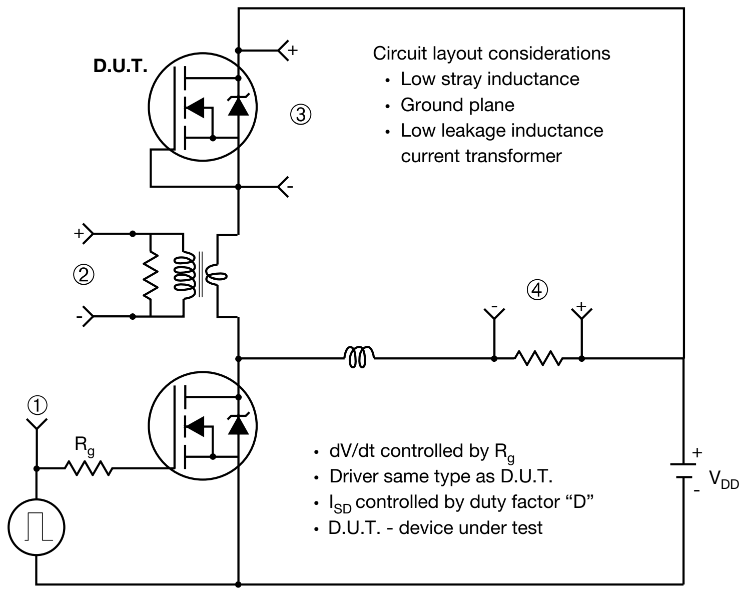
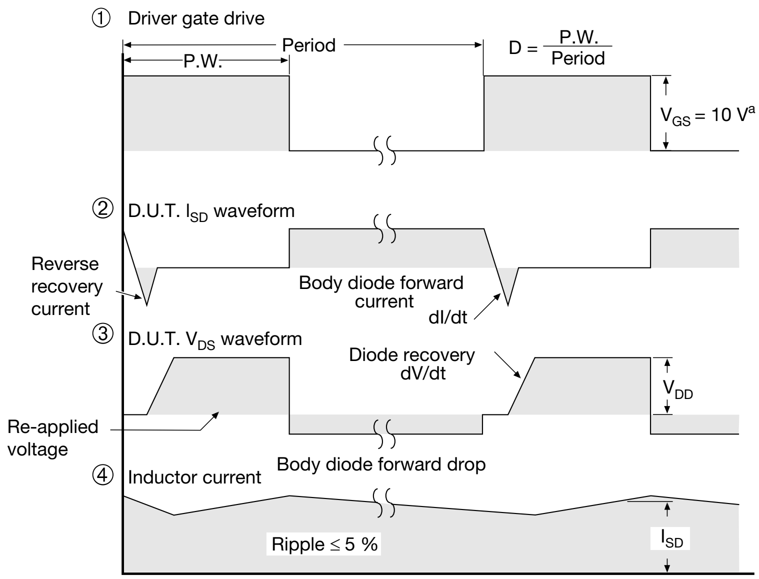
Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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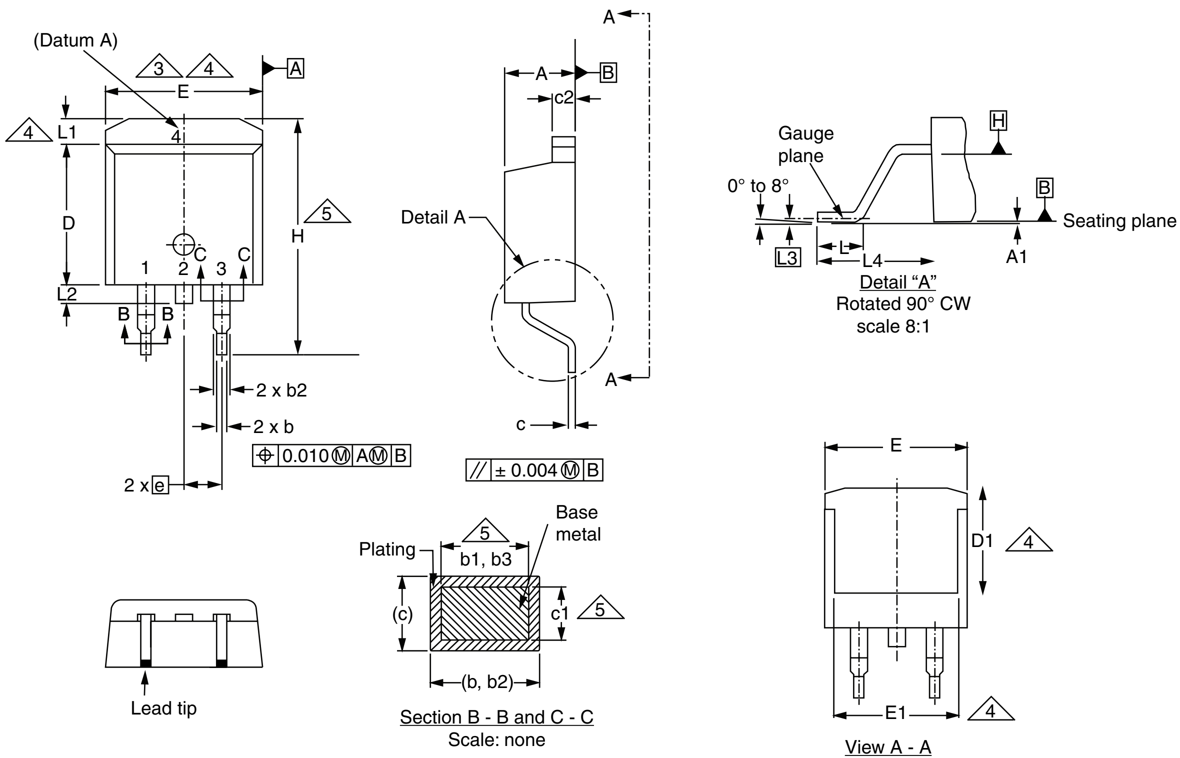
TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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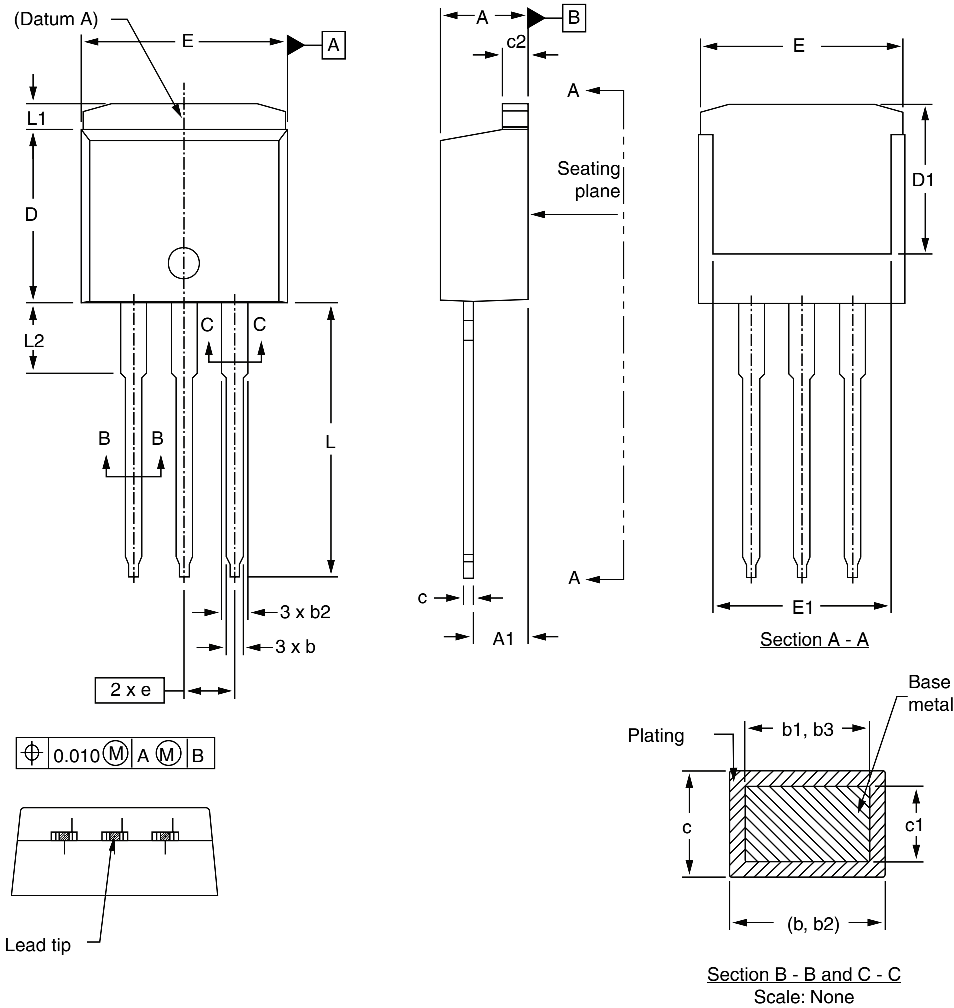
I^2PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

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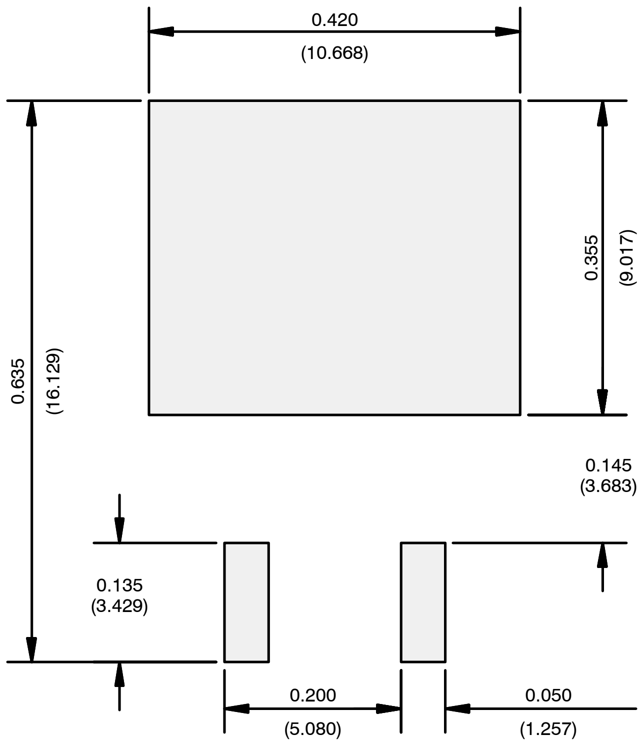
RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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