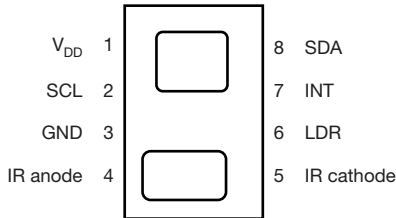


# Fully Integrated Proximity and Ambient Light Sensor With Infrared Emitter, I<sup>2</sup>C Interface, and Interrupt Function (with multiple slave addresses)



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## DESCRIPTION

VCNL4030X01 integrates a proximity sensor (PS), ambient light sensor (ALS), and a high power IRED into one small package. It incorporates photodiodes, amplifiers, and analog to digital converting circuits into a single chip by CMOS process. The 16-bit high resolution ALS for excellent sensing capabilities with sufficient selections to fulfill most applications whether dark or high transparency lens design. Both ALS and PS offer a programmable interrupt with individual high and low thresholds offers the power savings on the microcontroller.

The proximity sensor features an intelligent cancellation scheme, so that cross talk is eliminated effectively. The proximity's smart persistence feature prevents the misjudgment of proximity sensing with a fast response time. Active force mode, one time trigger by one instruction, offers more design flexibility to fulfill different kinds of applications with more power savings.

The adoption of patented Filtron™ technology achieves the closest ambient light spectral sensitivity to real human eye responses and offers the best background light cancellation capability (including sunlight) without utilizing the microcontrollers' resources. VCNL4030X01 provides an excellent temperature compensation capability for keeping the output stable over temperature. ALS and PS functions are easily operated via the simple command format of I<sup>2</sup>C (SMBus compatible) interface protocol. Operating voltage ranges from 2.5 V to 3.6 V. VCNL4030X01 is packaged in a lead-free 8-pin QFN package, which offers the best market-proven reliability quality.

## FEATURES

- Package type: surface-mount
- Dimensions (L x W x H in mm): 4.0 x 2.36 x 0.75
- AEC-Q101 qualified
- Integrated modules: infrared emitter (IRED), ambient light sensor (ALS), proximity sensor (PS), and signal conditioning IC
- Operates ALS and PS in parallel structure
- Filtron™ technology adoption for robust background light cancellation
- Low power consumption I<sup>2</sup>C (SMBus compatible) interface
- Orderable in four different slave addresses
- Output type: I<sup>2</sup>C bus (ALS / PS)
- Operation voltage: 2.5 V to 3.6 V
- Floor life: 168 h, MSL 3, according to J-STD-020
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

AUTOMOTIVE GRADE


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**  
**GREEN**  
 (5-2008)

## PROXIMITY FUNCTION

- Immunity to red glow (940 nm IRED)
- Programmable IRED sink current
- Intelligent cancellation to reduce cross talk phenomenon
- Smart persistence scheme to reduce PS response time
- Selectable for 12- / 16-bit PS output data

## AMBIENT LIGHT FUNCTION

- High accuracy of ALS ± 10 %
- Fluorescent light flicker immunity
- Spectrum close to real human eye responses

## INTERRUPT

- Programmable interrupt function for ALS and PS with upper and lower thresholds
- Adjustable persistence to prevent false triggers for ALS and PS

## APPLICATIONS

- Proximity sensor for
  - Mobile devices (e.g. smart phones, tablets) for touch screen locking, power saving etc.
  - Automotive for presence detection
- Integrated ambient light function for display / keypad contrast control and dimming of mobile devices
- Collision detection in robots and toys
- Proximity / optical switch for consumer, computing, automotive and industrial devices, and displays (like notebooks, tablet PCs, and automotive touch panels)
- Dimming control for consumer, computing, industrial, and automotive displays

**PRODUCT SUMMARY**

| PART NUMBER | OPERATING RANGE (mm) | OPERATING VOLTAGE RANGE (V) | I <sup>2</sup> C BUS VOLTAGE RANGE (V) | IRED PULSE CURRENT (mA) <sup>(1)</sup> | AMBIENT LIGHT RANGE (lx) | AMBIENT LIGHT RESOLUTION (lx) | OUTPUT CODE              | ADC RESOLUTION PROXIMITY / AMBIENT LIGHT |
|-------------|----------------------|-----------------------------|--|--|--------------------------|-------------------------------|--------------------------|--|
| VCNL4030X01 | 0 to 300             | 2.5 to 3.6                  | 1.8 to 5.5                             | 200                                    | 0.004 to 16 768          | 0.004                         | 16 bit, I <sup>2</sup> C | 16 bit / 16 bit                          |

**Note**<sup>(1)</sup> Adjustable through I<sup>2</sup>C interface**ORDERING INFORMATION**

| ORDERING CODE     | PACKAGING     | VOLUME <sup>(1)</sup> | REMARKS                    |
|-------------------|---------------|-----------------------|----------------------------|
| VCNL4030X01-GS08  | Tape and reel | MOQ: 3300 pcs         | 4.0 mm x 2.36 mm x 0.75 mm |
| VCNL4030X01-GS18  |               | MOQ: 13 000 pcs       |                            |
| VCNL40301X01-GS08 |               | MOQ: 3300 pcs         |                            |
| VCNL40301X01-GS18 |               | MOQ: 13 000 pcs       |                            |
| VCNL40302X01-GS08 |               | MOQ: 3300 pcs         |                            |
| VCNL40302X01-GS18 |               | MOQ: 13 000 pcs       |                            |
| VCNL40303X01-GS08 |               | MOQ: 3300 pcs         |                            |
| VCNL40303X01-GS18 |               | MOQ: 13 000 pcs       |                            |

**Note**<sup>(1)</sup> MOQ: minimum order quantity**SLAVE ADDRESS OPTIONS**

| ORDERING CODE     | SLAVE ADDRESS (7 bit) |
|-------------------|-----------------------|
| VCNL4030X01-GS08  | 0x60                  |
| VCNL4030X01-GS18  |                       |
| VCNL40301X01-GS08 | 0x51                  |
| VCNL40301X01-GS18 |                       |
| VCNL40302X01-GS08 | 0x40                  |
| VCNL40302X01-GS18 |                       |
| VCNL40303X01-GS08 | 0x41                  |
| VCNL40303X01-GS18 |                       |

**ABSOLUTE MAXIMUM RATINGS** (T<sub>amb</sub> = 25 °C, unless otherwise specified)

| PARAMETER                   | TEST CONDITION | SYMBOL           | MIN. | MAX. | UNIT |
|-----------------------------|----------------|------------------|------|------|------|
| Supply voltage              |                | V <sub>DD</sub>  | 2.5  | 3.6  | V    |
| Operation temperature range |                | T <sub>amb</sub> | -40  | +105 | °C   |
| Storage temperature range   |                | T <sub>stg</sub> | -40  | +110 | °C   |

**RECOMMENDED OPERATING CONDITIONS** (T<sub>amb</sub> = 25 °C, unless otherwise specified)

| PARAMETER                                | TEST CONDITION | SYMBOL                | MIN. | MAX. | UNIT |
|--|----------------|-----------------------|------|------|------|
| Supply voltage                           |                | V <sub>DD</sub>       | 2.5  | 3.6  | V    |
| Operation temperature range              |                | T <sub>amb</sub>      | -40  | +105 | °C   |
| I <sup>2</sup> C bus operating frequency |                | f <sub>(I2CCLK)</sub> | 10   | 400  | kHz  |

| PIN DESCRIPTIONS |                 |                    |   |
|------------------|-----------------|--------------------|---|
| PIN ASSIGNMENT   | SYMBOL          | TYPE               | FUNCTION                                      |
| 1                | V <sub>DD</sub> | -                  | Power supply input                            |
| 2                | SCL             | I                  | I <sup>2</sup> C digital bus clock input      |
| 3                | GND             | -                  | Ground  |
| 4                | IR ANODE        | I                  | Anode for IRED                                |
| 5                | IR CATHODE      | I                  | Cathode (IRED) connection                     |
| 6                | LDR             | I                  | IRED driver input                             |
| 7                | INT             | O                  | Interrupt pin                                 |
| 8                | SDA             | I / O (open drain) | I <sup>2</sup> C data bus data input / output |

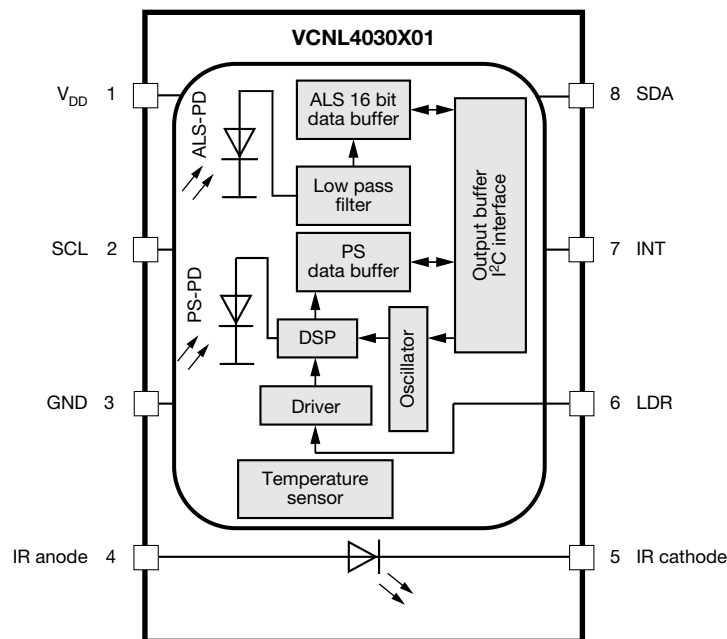
**BLOCK DIAGRAM**


Fig. 1 - Detailed Block Diagram

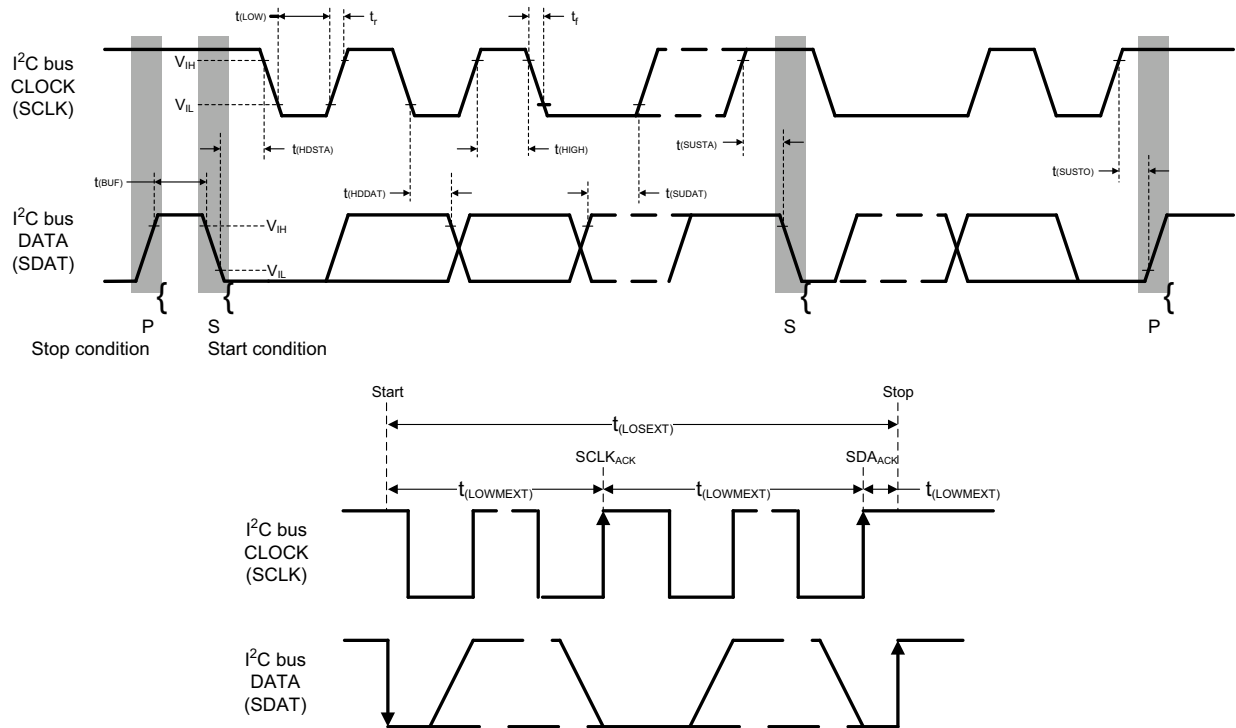


| <b>BASIC CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified) |   |   |          |        |               |                    |   |
|---|---|---|----------|--------|---------------|--------------------|---|
| PARAMETER   | TEST CONDITION                                    | SYMBOL  | MIN.     | TYP.   | MAX.          | UNIT               |   |
| Supply voltage  |   | $V_{DD}$                                      | 2.5      | -      | 3.6           | V                  |   |
| Supply current  | Excluded LED driving                              | $I_{DD}$                                      | -        | 300    | -             | $\mu\text{A}$      |   |
|   | Light condition = dark, $V_{DD} = 3.3\text{ V}$   | $I_{DD}(\text{SD})$                           | -        | 0.2    | -             | $\mu\text{A}$      |   |
| I <sup>2</sup> C supply voltage   |   | $V_{PULL\ UP}$                                | 1.8      | -      | 5.5           | V                  |   |
| ALS shut down   | ALS disable, PS enable                            | $I_{ALSSD}$                                   | -        | 200    | -             | $\mu\text{A}$      |   |
| PS shut down  | ALS enable, PS disable                            | $I_{PSSD}$                                    | -        | 260    | -             | $\mu\text{A}$      |   |
| I <sup>2</sup> C signal input   | Logic high  | $V_{DD} = 3.3\text{ V}$                       | $V_{IH}$ | 1.55   | -             | -                  | V |
|   | Logic low   |   | $V_{IL}$ | -      | -             | 0.4                |   |
|   | Logic high  | $V_{DD} = 2.6\text{ V}$                       | $V_{IH}$ | 1.4    | -             | -                  | V |
|   | Logic low   |   | $V_{IL}$ | -      | -             | 0.4                |   |
| Peak sensitivity wavelength of ALS  |   | $\lambda_p$                                   | -        | 550    | -             | nm                 |   |
| Peak sensitivity wavelength of PS   |   | $\lambda_p$                                   | -        | 850    | -             | nm                 |   |
| Full ALS counts   | 16-bit resolution                                 |   | -        | -      | 65 535        | steps              |   |
| Full PS counts  | 12-bit / 16-bit resolution                        |   | -        | -      | 4096 / 65 535 | steps              |   |
| ALS sensing tolerance   | White LED light source                            |   | -        | -      | $\pm 10$      | %                  |   |
| Detectable intensity  | Minimum   | ALS_IT = 800 ms, 1 step <sup>(1)(2)</sup>     | -        | 0.004  | -             | lx                 |   |
|   | Maximum   | ALS_IT = 50 ms, 65 535 step <sup>(1)(2)</sup> | -        | 16 768 | -             |                    |   |
| ALS dark offset   | ALS_IT = 50 ms, normal sensitivity <sup>(1)</sup> |   | 0        | -      | 3             | steps              |   |
| PS detection range  | Kodak gray card                                   |   | 0        | -      | 300           | mm                 |   |
| Operating temperature range   |   | $T_{amb}$                                     | -40      | -      | +105          | $^{\circ}\text{C}$ |   |
| LED_Anode voltage   |   |   | -        | -      | 5.5           | V                  |   |
| IRED driving current  | <sup>(3)</sup>                                    |   | -        | 200    | -             | mA                 |   |

**Notes**

- <sup>(1)</sup> Test condition:  $V_{DD} = 3.3\text{ V}$ , temperature:  $25\text{ }^{\circ}\text{C}$
- <sup>(2)</sup> Maximum detection range to ambient light can be determined by ALS refresh time adjustment and two sensitivity bits (ALS\_HD and ALS\_NS). Refer to table "ALS Resolution and Maximum Detection Range"
- <sup>(3)</sup> Programmable between 50 mA and 200 mA; based on IRED on / off duty ratio = 1/40, 1/80, 1/160, and 1/320

| <b>I<sup>2</sup>C BUS TIMING CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified) |                |               |      |           |      |               |
|---|----------------|---------------|------|-----------|------|---------------|
| PARAMETER   | SYMBOL         | STANDARD MODE |      | FAST MODE |      | UNIT          |
|   |                | MIN.          | MAX. | MIN.      | MAX. |               |
| Clock frequency   | $f_{(I2CCLK)}$ | 10            | 100  | 10        | 400  | kHz           |
| Bus free time between start and stop condition  | $t_{(BUF)}$    | 4.7           | -    | 1.3       | -    | $\mu\text{s}$ |
| Hold time after (repeated) start condition;<br>after this period, the first clock is generated                          | $t_{(HDSTA)}$  | 4.0           | -    | 0.6       | -    | $\mu\text{s}$ |
| Repeated start condition setup time   | $t_{(SUSTA)}$  | 4.7           | -    | 0.6       | -    | $\mu\text{s}$ |
| Stop condition setup time   | $t_{(SUSTO)}$  | 4.0           | -    | 0.6       | -    | $\mu\text{s}$ |
| Data hold time  | $t_{(HDDAT)}$  | -             | 3450 | -         | 900  | ns            |
| Data setup time   | $t_{(SUDAT)}$  | 250           | -    | 100       | -    | ns            |
| I <sup>2</sup> C clock (SCK) low period   | $t_{(LOW)}$    | 4.7           | -    | 1.3       | -    | $\mu\text{s}$ |
| I <sup>2</sup> C clock (SCK) high period  | $t_{(HIGH)}$   | 4.0           | -    | 0.6       | -    | $\mu\text{s}$ |
| Clock / data fall time  | $t_f$          | -             | 300  | -         | 300  | ns            |
| Clock / data rise time  | $t_r$          | -             | 1000 | -         | 300  | ns            |


 Fig. 2 - I<sup>2</sup>C Bus Timing Diagram

**PARAMETER TIMING INFORMATION**

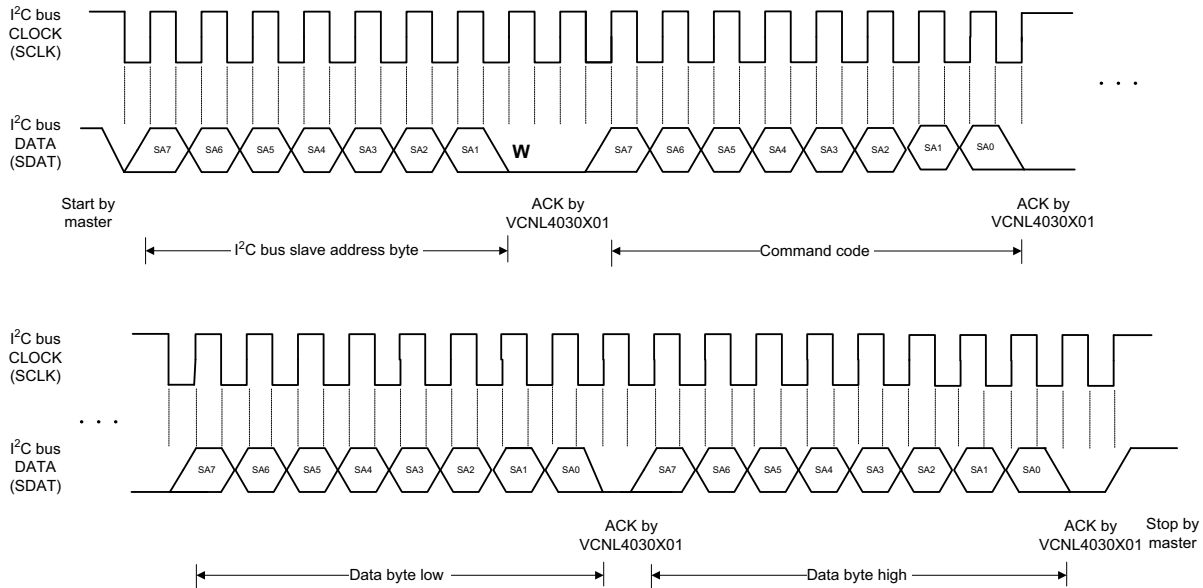


Fig. 3 - I<sup>2</sup>C Bus Timing for Sending Word Command Format

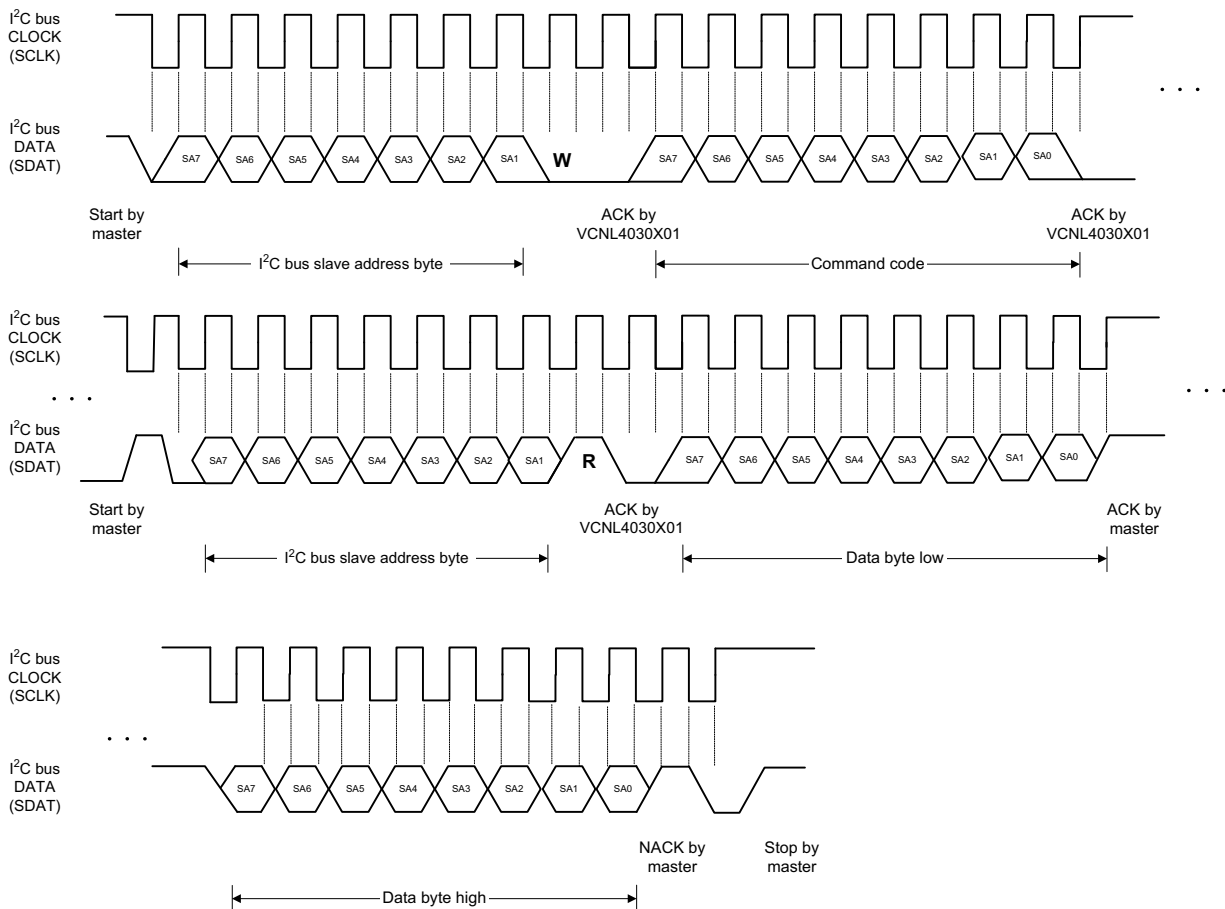


Fig. 4 - I<sup>2</sup>C Bus Timing for Receiving Word Command Format

**TYPICAL PERFORMANCE CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

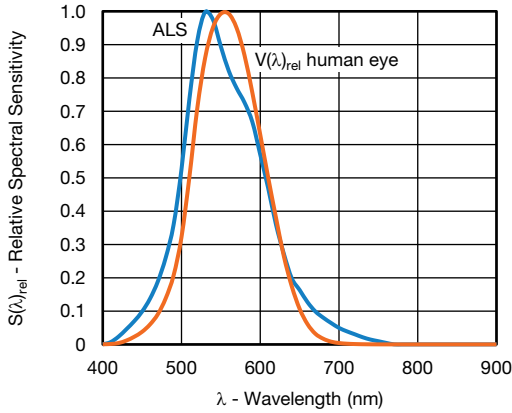


Fig. 5 - Normalized Spectral Response (ALS channel)

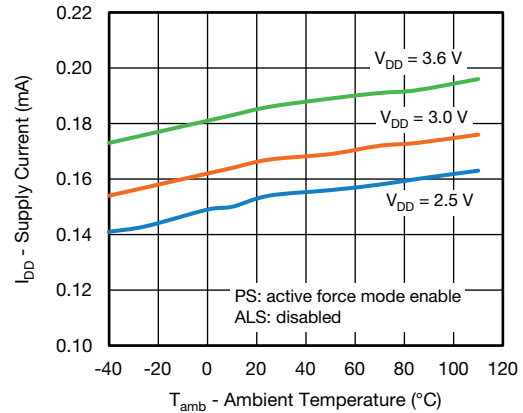


Fig. 8 - Supply Current vs. Ambient Temperature With Only PS = Active

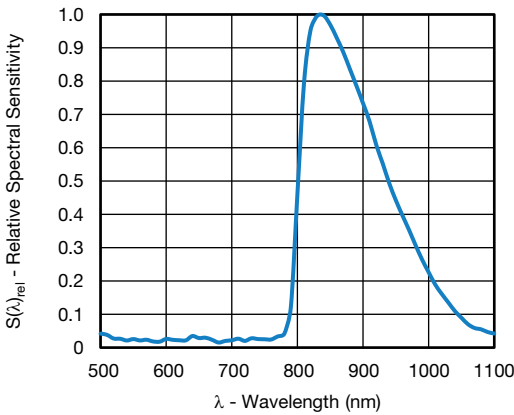


Fig. 6 - Normalized Spectral Response (PS channel)

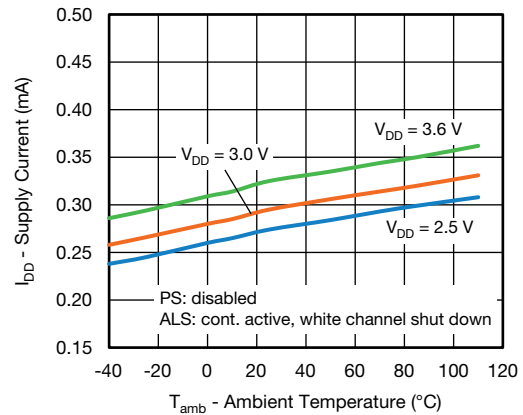


Fig. 9 - Supply Current vs. Ambient Temperature With Only ALS = Active

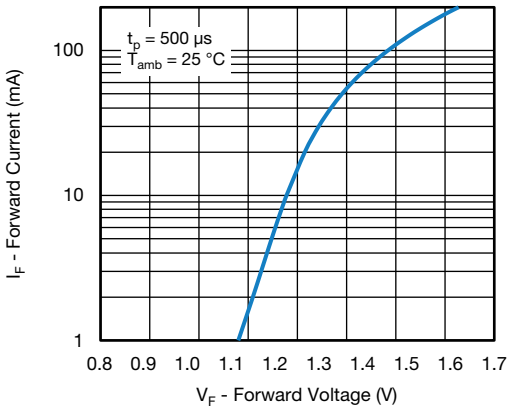


Fig. 7 - Forward Current  $I_F = f(V_F)$  for LED

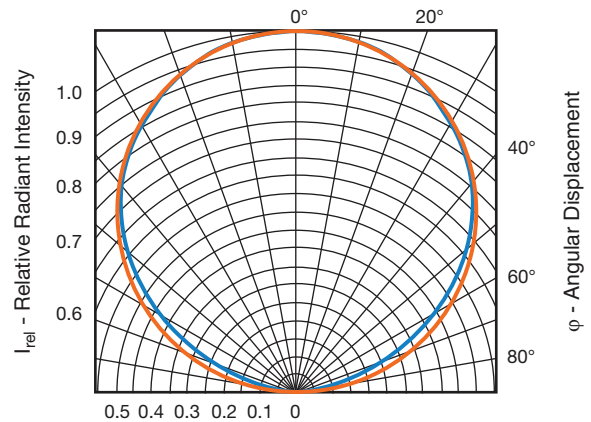


Fig. 10 - Relative Radiant Intensity Emitter vs. Angular Displacement

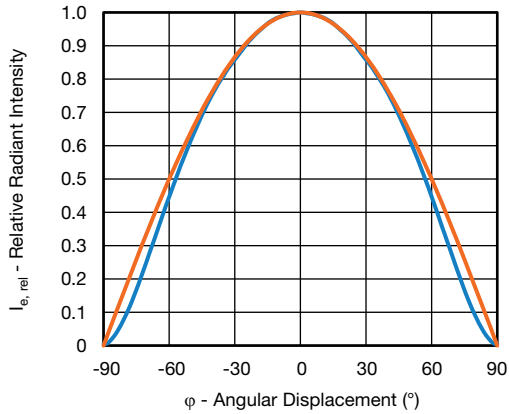


Fig. 11 - Relative Radiant Intensity Emitter vs. Angular Displacement

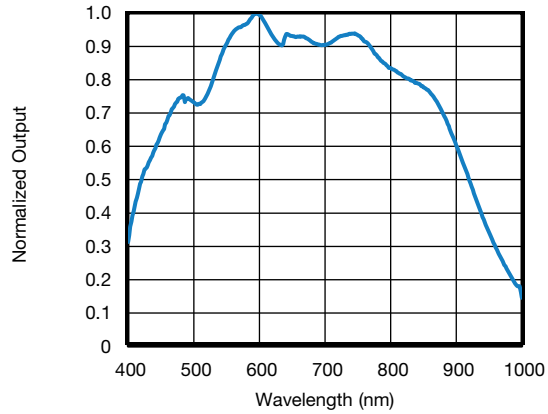


Fig. 14 - White Channel Spectral Response

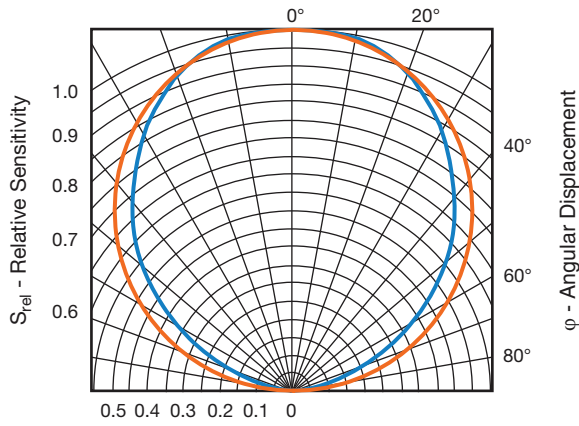


Fig. 12 - Relative Sensitivity vs. Angular Displacement (ALS)

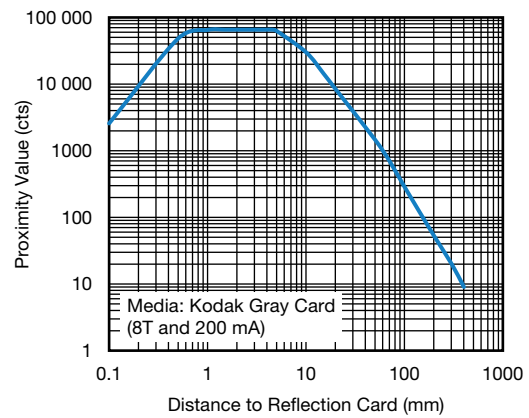


Fig. 15 - Proximity Value vs. Distance to Reflecting Card

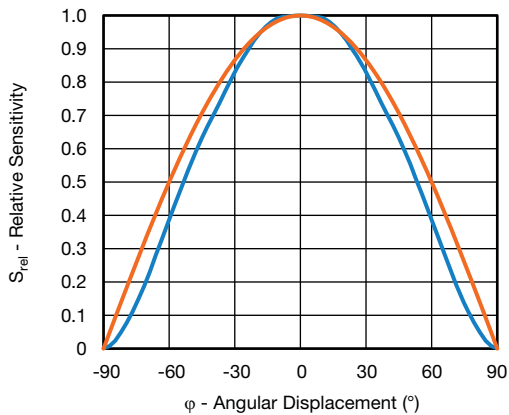


Fig. 13 - Relative Sensitivity vs. Angular Displacement



## APPLICATION INFORMATION

### Pin Connection with the Host

VCNL4030X01 integrates proximity sensor, ambient light Sensor, and IRED all together with I<sup>2</sup>C interface. It is very easy for the baseband (CPU) to access PS and ALS output data via I<sup>2</sup>C interface without extra software algorithms. The hardware schematic is shown in the following diagram.

Two additional capacitors in the circuit can be used for the following purposes: (1) the 0.1  $\mu$ F capacitor near the V<sub>DD</sub> pin is used for power supply noise rejection, (2) the 2.2  $\mu$ F capacitor - connected to the anode - is used to prevent the IRED voltage from instantly dropping when the IRED is turned on, and (3) 2.2 k $\Omega$  is suitable for the pull up resistor of I<sup>2</sup>C except for the 8.2 k $\Omega$  applied on the INT pin.

### Note

- IR cathode and LDR: pins need to be connected together externally

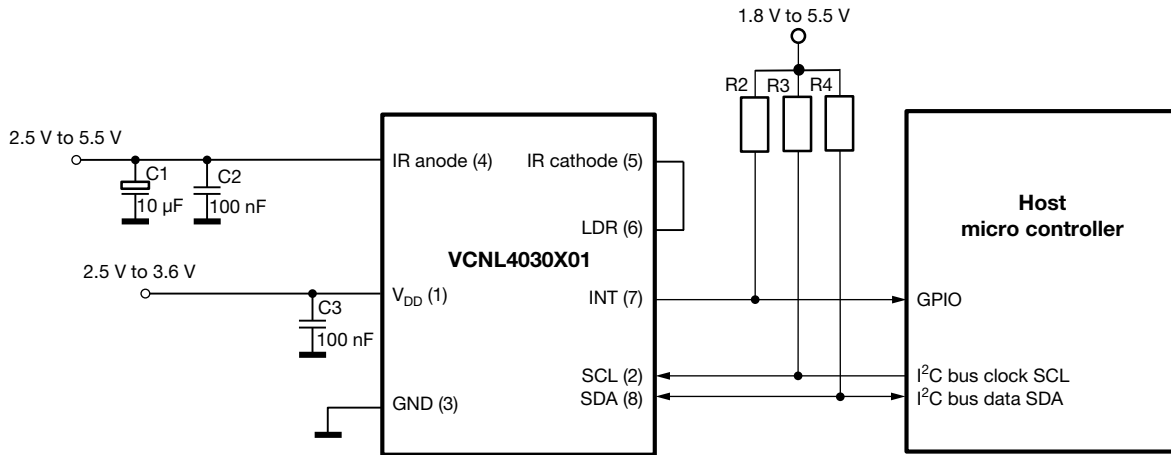


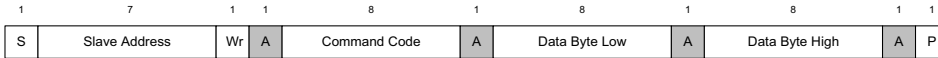
Fig. 16 - Circuitry with Two Separate Power Supply Sources



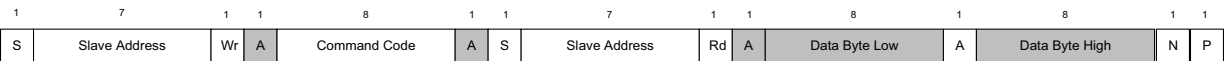
Digital Interface

VCNL4030X01 is available in four different salve addresses (0x60, 0x51, 0x40, and 0x41). Please refer to the table "Salve Address Options" at the beginning of the datasheet for an overview of the corresponding ordering codes. All operations can be controlled by the command register. The simple command structure helps users easily program the operation setting and latch the light data from VCNL4030X01. As Fig. 17 shows, VCNL4030X01's I2C command format is simple for read and write operations between VCNL4030X01 and the host. The white sections indicate host activity and the gray sections indicate VCNL4030X01's acknowledgement of the host access activity. Write word and read word protocol is suitable for accessing registers particularly for 16-bit data ALS and 12-bit / 16-bit PS data. Interrupt can be cleared by reading data out from register: INT\_Flag. All command codes should follow read word and write word protocols.

Send Byte → Write Command to VCNL4030X01



Receive Byte → Read Data from VCNL4030X01



- S = start condition
- P = stop condition
- A = acknowledge
- N = no acknowledge
- Shaded area = VCNL4030X01 acknowledge

Fig. 17 - Write Word and Read Word Protocol

Function Description

VCNL4030X01 applies a 16-bit high resolution ALS that provides the best ambient light sensing capability down to 0.004 lux/step which works well under a low transmittance lens design (dark lens). A flexible interrupt function of ALS (register: ALS\_CONF) is also supported. The INT signal will not be asserted by VCNL4030X01 if the ALS value is not over high INT threshold window level, or lower than low INT threshold window level of ALS. As long as the ALS INT is asserted, the host can read the data from VCNL4030X01. VCNL4030X01 detects different light sources such as fluorescent light, incandescent light, sunlight, and white LED with high accuracy ALS data output after detecting algorithm is implemented.

For proximity sensor function, VCNL4030X01 supports different kinds of mechanical designs to achieve the best proximity detection performance for any color of object with more flexibility. The basic PS function settings, such as duty ratio, integration time, interrupt, and PS enable / disable, and persistence, are handled by the register: PS\_CONF1. Duty ratio controls the PS response time. Integration time represents the duration of the energy being received. The interrupt is asserted when the PS detection levels over the high threshold level setting (register: PS\_THDH) or lower than low threshold (register: PS\_THDL). If the interrupt function is enabled, the host reads the PS output data from VCNL4030X01 that saves host loading from periodically reading PS data. More than that, INT flag (register: INT\_Flag) indicates the behavior of INT triggered under different conditions. PS persistence (PS\_PERS) sets up the PS INT asserted conditions as long as the PS output value continually exceeds the threshold level. The intelligent cancellation level can be set on register: PS\_CANC to reduce the cross talk phenomenon.

VCNL4030X01 also supports an easy use of proximity detection logic output mode that outputs just high / low levels saving loading from the host. Normal operation mode or proximity detection logic output mode can be selected on the register: PS\_MS. A smart persistence is provided to get faster PS response time and prevent false trigger for PS. Descriptions of each slave address operation are shown in table 1



| TABLE 1 - COMMAND CODE AND REGISTER DESCRIPTION |                      |               |       |               |  |
|---|----------------------|---------------|-------|---------------|--|
| COMMAND CODE                                    | DATE BYTE LOW / HIGH | REGISTER NAME | R / W | DEFAULT VALUE | FUNCTION DESCRIPTION   |
| 0x00  | L                    | ALS_CONF1     | R / W | 0x01          | ALS integration time, ALS dynamic range, persistence, interrupt, and function enable / disable   |
|   | H                    | ALS_CONF2     | R / W | 0x01          | ALS sensitivity, white channel enable / disable  |
| 0x01  | L                    | ALS_THDH_L    | R / W | 0x00          | ALS high interrupt threshold LSB byte  |
|   | H                    | ALS_THDH_M    | R / W | 0x00          | ALS high interrupt threshold MSB byte  |
| 0x02  | L                    | ALS_THDL_L    | R / W | 0x00          | ALS low interrupt threshold LSB byte   |
|   | H                    | ALS_THDL_M    | R / W | 0x00          | ALS low interrupt threshold MSB byte   |
| 0x03  | L                    | PS_CONF1      | R / W | 0x01          | PS duty ratio, integration time, persistence, and PS enable / disable  |
|   | H                    | PS_CONF2      | R / W | 0x00          | PS gain, PS output resolution, PS interrupt trigger  |
| 0x04  | L                    | PS_CONF3      | R / W | 0x00          | PS smart persistence, active force mode  |
|   | H                    | PS_MS         | R / W | 0x00          | LED current selection  |
| 0x05  | L                    | PS_CANC_L     | R / W | 0x00          | PS cancellation level setting  |
|   | H                    | PS_CANC_M     | R / W | 0x00          | PS cancellation level setting  |
| 0x06  | L                    | PS_THDL_L     | R / W | 0x00          | PS low interrupt threshold setting LSB byte  |
|   | H                    | PS_THDL_M     | R / W | 0x00          | PS low interrupt threshold setting MSB byte  |
| 0x07  | L                    | PS_THDH_L     | R / W | 0x00          | PS high interrupt threshold setting LSB byte   |
|   | H                    | PS_THDH_M     | R / W | 0x00          | PS high interrupt threshold setting MSB byte   |
| 0x08  | L                    | PS_Data_L     | R     | 0x00          | PS LSB output data   |
|   | H                    | PS_Data_M     | R     | 0x00          | PS MSB output data   |
| 0x09  | L                    | Reserved      | R     | 0x00          | Reserved   |
|   | H                    | Reserved      | R     | 0x00          | Reserved   |
| 0x0A  | L                    | Reserved      | R     | 0x00          | Reserved   |
|   | H                    | Reserved      | R     | 0x00          | Reserved   |
| 0x0B  | L                    | ALS_Data_L    | R     | 0x00          | ALS LSB output data  |
|   | H                    | ALS_Data_M    | R     | 0x00          | ALS MSB output data  |
| 0x0C  | L                    | White_Data_L  | R     | 0x00          | White LSB output data  |
|   | H                    | White_Data_M  | R     | 0x00          | White MSB output data  |
| 0x0D  | L                    | Reserved      | R     | 0x00          | Reserved   |
|   | H                    | INT_Flag      | R     | 0x00          | ALS, PS interrupt flags, PS sunlight protection mode flag  |
| 0x0E  | L                    | ID_L          | R     | 0x80          | Device ID LSB  |
|   | H                    | ID_M          | R     | 0x00          | For version with 0x60 as device address; 0x10 for version with 0x51, 0x20 for version with 0x40 and 0x30 for version with 0x41 as device address |

**Note**

- All of reserved register are used for internal test. Please keep as default setting

**Command Register Format**

VCNL4030X01 provides an 8-bit command register for ALS and PS controlling independently. The description of each command format is shown in following tables.

| TABLE 2 - REGISTER: ALS_CONF1 DESCRIPTION |       |  |   |   |   |   |   |   |   |
|---|-------|--|---|---|---|---|---|---|---|
| REGISTER NAME                             |       | COMMAND CODE: 0x00_L (0x00 DATA BYTE LOW)  |   |   |   |   |   |   |   |
| Command                                   | Bit   | 7  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|   |       | COMMAND CODE: 0x00_L (0x00 DATA BYTE LOW)  |   |   |   |   |   |   |   |
| Command                                   | Bit   | Description  |   |   |   |   |   |   |   |
| ALS_IT                                    | 7 : 5 | (0 : 0 : 0) = 50 ms; (0 : 0 : 1) = 100 ms; (0 : 1 : 0) = 200 ms; (0 : 1 : 1) = 400 ms; (1 : 0 : 0) to (1 : 1 : 1) = 800 ms<br>ALS integration time setting, longer integration time has higher sensitivity |   |   |   |   |   |   |   |
| ALS_HD                                    | 4     | 0 = typical dynamic range x 1, 1 = typical dynamic range x 2   |   |   |   |   |   |   |   |
| ALS_PERS                                  | 3 : 2 | (0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 4, (1 : 1) = 8<br>ALS interrupt persistence setting  |   |   |   |   |   |   |   |
| ALS_INT_EN                                | 1     | 0 = ALS interrupt disable, 1 = ALS interrupt enable  |   |   |   |   |   |   |   |
| ALS_SD                                    | 0     | 0 = ALS power on, 1 = ALS shut down, default = 1   |   |   |   |   |   |   |   |

**TABLE 3 - REGISTER: ALS\_CONF2 DESCRIPTION**

| COMMAND CODE: 0x00_H (0x00 DATA BYTE HIGH) |       |  |
|--|-------|--|
| Command                                    | Bit   | Description  |
| Reserved                                   | 7 : 2 | Default = (0 : 0 : 0 : 0 : 0 : 0)                                    |
| ALS_NS                                     | 1     | 0 = typical sensitivity x 2, 1 = typical sensitivity x 1             |
| WHITE_SD                                   | 0     | 0 = WHITE channel power on, 1 = WHITE channel shut down, default = 1 |

**TABLE 4 - REGISTER ALS\_THDH\_L AND ALS\_THDH\_M DESCRIPTION**

| COMMAND CODE: 0x01_L (0x01 DATA BYTE LOW) OR 0x01_H (0x01 DATA BYTE HIGH) |       |   |
|---|-------|---|
| Register  | Bit   | Description   |
| ALS_THDH_L  | 7 : 0 | 0x00 to 0xFF, ALS high interrupt threshold LSB byte |
| ALS_THDH_M  | 7 : 0 | 0x00 to 0xFF, ALS high interrupt threshold MSB byte |

**TABLE 5 - REGISTER: ALS\_THDL\_L AND ALS\_THDL\_M DESCRIPTION**

| COMMAND CODE: 0x02_L (0x02 DATA BYTE LOW) AND 0x02_H (0x02 DATA BYTE HIGH) |       |  |
|--|-------|--|
| Register   | Bit   | Description  |
| ALS_THDL_L   | 7 : 0 | 0x00 to 0xFF, ALS low interrupt threshold LSB byte |
| ALS_THDL_M   | 7 : 0 | 0x00 to 0xFF, ALS low interrupt threshold MSB byte |

**TABLE 6 - REGISTER: PS\_CONF1 DESCRIPTION**

| REGISTER: PS_CONF1 |       |  | COMMAND CODE: 0x03_L (0x03 DATA BYTE LOW) |  |  |
|--------------------|-------|--|---|--|--|
| Command            | Bit   | Description  |   |  |  |
| PS_Duty            | 7 : 6 | (0 : 0) = 1/40, (0 : 1) = 1/80, (1 : 0) = 1/160, (1 : 1) = 1/320<br>PS IRED on / off duty ratio setting  |   |  |  |
| PS_PERS            | 5 : 4 | (0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 3, (1 : 1) = 4<br>PS interrupt persistence setting   |   |  |  |
| PS_IT              | 3 : 1 | (0 : 0 : 0) = 1T, (0 : 0 : 1) = 1.5T, (0 : 1 : 0) = 2T, (0 : 1 : 1) = 2.5T, (1 : 0 : 0) = 3T, (1 : 0 : 1) = 3.5T,<br>(1 : 1 : 0) = 4T, (1 : 1 : 1) = 8T, PS integration time setting |   |  |  |
| PS_SD              | 0     | 0 = PS power on, 1 = PS shut down, default = 1   |   |  |  |

**TABLE 7 - REGISTER: PS\_CONF2 DESCRIPTION**

| REGISTER: PS_CONF2 |       |  | COMMAND CODE: 0x03_H (0x03 DATA BYTE HIGH) |  |  |
|--------------------|-------|--|--|--|--|
| Command            | Bit   | Description  |  |  |  |
| Reserved           | 7 : 6 | (0 : 0), reserved  |  |  |  |
| PS_Gain            | 5 : 4 | (0 : 0) and (0 : 1) = two step mode, (1 : 0) = single mode x 8, (1 : 1) = single mode x 1                                      |  |  |  |
| PS_HD              | 3     | 0 = PS output is 12 bits, 1 = PS output is 16 bits   |  |  |  |
| PS_NS              | 2     | 0 = typical sensitivity (two step mode x 4), 1 = typical sensitivity mode (two step mode)                                      |  |  |  |
| PS_INT             | 1 : 0 | (0 : 0) = interrupt disable, (0 : 1) = trigger by closing, (1 : 0) = trigger by away,<br>(1 : 1) = trigger by closing and away |  |  |  |

**TABLE 8 - REGISTER: PS\_CONF3 DESCRIPTION**

| REGISTER: PS_CONF3 |       | COMMAND CODE: 0x04_L (0x04 DATA BYTE LOW)   |
|--------------------|-------|---|
| Command            | Bit   | Description   |
| LED_I_LOW          | 7     | 0 = disabled = normal current, 1 = enabled = 1/10 of normal current, with that the current is accordingly: 5 mA, 7.5 mA, 10 mA, 12 mA, 14 mA, 16 mA, 18 mA, 20 mA                     |
| Reserved           | 6 : 5 | (0 : 0)   |
| PS_SMART_PERS      | 4     | 0 = disable; 1 = enable PS smart persistence  |
| PS_AF              | 3     | 0 = active force mode disable (normal mode), 1 = active force mode enable   |
| PS_TRIG            | 2     | 0 = no PS active force mode trigger, 1 = trigger one time cycle<br>VCNL4030X01 output one cycle data every time host writes in '1' to sensor. The state returns to '0' automatically. |
| PS_MS              | 1     | 0 = proximity normal operation with interrupt function, 1 = proximity detection logic output mode enable  |
| PS_SC_EN           | 0     | 0 = turn off sunlight cancel; 1 = turn on sunlight cancel<br>PS sunlight cancel function enable setting   |

**TABLE 9 - REGISTER: PS\_MS DESCRIPTION**

| REGISTER: PS_MS |       | COMMAND CODE: 0x04_H (0x04 DATA BYTE HIGH)  |
|-----------------|-------|---|
| Command         | Bit   | Description   |
| Reserved        | 7     | 0   |
| PS_SC_CUR       | 6 : 5 | (0 : 0) = 1 x typical sunlight cancel current, (0 : 1) = 2 x typical sunlight cancel current, (1 : 0) = 4 x typical sunlight cancel current, (1 : 1) = 8 x typical sunlight cancel current                      |
| PS_SP           | 4     | 0 = typical sunlight capability, 1 = 1.5 x typical sunlight capability  |
| PS_SPO          | 3     | 0 = output is 00h in sunlight protect mode, 1 = output is FFh in sunlight protect mode,   |
| LED_I           | 2 : 0 | (0 : 0 : 0) = 50 mA; (0 : 0 : 1) = 75 mA; (0 : 1 : 0) = 100 mA; (0 : 1 : 1) = 120 mA<br>(1 : 0 : 0) = 140 mA; (1 : 0 : 1) = 160 mA; (1 : 1 : 0) = 180 mA; (1 : 1 : 1) = 200 mA<br>LED current selection setting |

**TABLE 10 - REGISTER PS\_CANC\_L AND PS\_CANC\_M DESCRIPTION**

|           |       | COMMAND CODE: 0x05_L (0x05 DATA BYTE LOW) AND 0x05_H (0x05 DATA BYTE HIGH) |
|-----------|-------|--|
| Register  | Bit   | Description  |
| PS_CANC_L | 7 : 0 | 0x00 to 0xFF, PS cancellation level setting_LSB byte                       |
| PS_CANC_M | 7 : 0 | 0x00 to 0xFF, PS cancellation level setting_MSB byte                       |

**TABLE 11 - REGISTER: PS\_THDL\_L AND PS\_THDL\_M DESCRIPTION**

|           |       | COMMAND CODE: 0x06_L (0x06 DATA BYTE LOW) AND 0x06_H (0x06 DATA BYTE HIGH) |
|-----------|-------|--|
| Register  | Bit   | Description  |
| PS_THDL_L | 7 : 0 | 0x00 to 0xFF, PS interrupt low threshold setting_LSB byte                  |
| PS_THDL_M | 7 : 0 | 0x00 to 0xFF, PS interrupt low threshold setting_MSB byte                  |

**TABLE 12 - REGISTER: PS\_THDH\_L AND PS\_THDH\_M DESCRIPTION**

|           |       | COMMAND CODE: 0x07_L (0x07 DATA BYTE LOW) AND 0x07_H (0x07 DATA BYTE HIGH) |
|-----------|-------|--|
| Register  | Bit   | Description  |
| PS_THDH_L | 7 : 0 | 0x00 to 0xFF, PS interrupt high threshold setting_LSB byte                 |
| PS_THDH_M | 7 : 0 | 0x00 to 0xFF, PS interrupt high threshold setting_MSB byte                 |

**TABLE 13 - READ OUT REGISTER DESCRIPTION**

| Register     | Command Code                 | Bit                                  | Description   |
|--------------|------------------------------|--------------------------------------|---|
| PS_Data_L    | 0x08_L (0x08 data byte low)  | 7 : 0                                | 0x00 to 0xFF, PS1 LSB output data   |
| PS_Data_M    | 0x08_H (0x08 data byte high) | 7 : 0                                | 0x00 to 0xFF, PS1 MSB output data   |
| Reserved     | 0x09_L (0x09 data byte low)  | 7 : 0                                | Reserved  |
| Reserved     | 0x09_H (0x09 data byte high) | 7 : 0                                | Reserved  |
| Reserved     | 0x0A_L (0x0A data byte low)  | 7 : 0                                | Reserved  |
| Reserved     | 0x0A_H (0x0A data byte high) | 7 : 0                                | Reserved  |
| ALS_Data_L   | 0x0B_L (0x0B data byte low)  | 7 : 0                                | 0x00 to 0xFF, ALS LSB output data   |
| ALS_Data_M   | 0x0B_H (0x0B data byte high) | 7 : 0                                | 0x00 to 0xFF, ALS MSB output data   |
| White_Data_L | 0x0C_L (0x0C data byte low)  | 7 : 0                                | 0x00 to 0xFF, white LSB output data   |
| White_Data_M | 0x0C_H (0x0C data byte high) | 7 : 0                                | 0x00 to 0xFF, white MSB output data   |
| Reserved     | 0x0D_L (0x0D data byte low)  | 7 : 0                                | Default = 0x00  |
| INT_Flag     | 0x0D_H (0x0D data byte high) | 7<br>6<br>5<br>4<br>3<br>2<br>1<br>0 | Reserved<br>Reserved<br>ALS_IF_L, ALS crossing low THD INT trigger event<br>ALS_IF_H, ALS crossing high THD INT trigger event<br>Reserved<br>PS_SPFLAG, PS entering sunlight protection mode<br>PS_IF_CLOSE, PS rises above PS_THDH INT trigger event<br>PS_IF_AWAY, PS drops below PS_THDL INT trigger event |
| ID_L         | 0x0E_L (0x0E data byte low)  | 7 : 0                                | 0x80  |
| ID_M         | 0x0E_H (0x0E data byte high) | 7 : 6<br>5 : 4<br>3 : 0              | (0 : 0)<br>(0:0) = slave address = 0x60 (7-bit)<br>(0:1) = slave address = 0x51 (7-bit)<br>(1:0) = slave address = 0x40 (7-bit)<br>(1:1) = slave address = 0x41 (7-bit)<br>Version code (0 : 0 : 0 : 0)   |

**Adjustable Sampling Time**

VCNL4030X01's embedded LED driver drives the internal IRED with the "LDR" pin by a pulsed duty cycle. The IRED on / off duty ratio is programmable by I<sup>2</sup>C command at register: PS\_Duty which is related to the current consumption and PS response time. The higher the duty ratio adopted, the faster response time achieved with higher power consumption. For example, PS\_Duty = 1/320, peak IRED current = 100 mA, averaged current consumption is 100 mA/320 = 0.3125 mA.

**Initialization**

VCNL4030X01 includes default values for each register. As long as power is on, it is ready to be controlled by host via I<sup>2</sup>C bus.



Threshold Window Setting

- ALS Threshold Window Setting (Applying ALS INT)

Register: ALS\_THDH\_L and ALS\_THDH\_M defines 16-bit ALS high threshold data for LSB byte and MSB byte. Register: ALS\_THDL\_L and ALS\_THDL\_M defines 16-bit ALS low threshold data for LSB byte and MSB byte. As long as ALS INT function is enabled, INT will be asserted once the ALS data exceeds ALS\_THDH or goes below ALS\_THDL. To easily define the threshold range, multiply the value of the resolution (lux/step) by the threshold level (refer to table 14).

| TABLE 14 - ALS RESOLUTION AND MAXIMUM DETECTION RANGE |                         |                |                         |
|---|-------------------------|----------------|-------------------------|
| ALS_IT  |                         | SENSITIVITY    | MAXIMUM DETECTION RANGE |
| ALS_IT (7 : 5)  | INTEGRATION TIME (typ.) | UNIT (lx/step) | UNIT (lx)               |
| (0, 0, 0)   | 50 ms                   | 0.064          | 4192                    |
| (0, 0, 1)   | 100 ms                  | 0.032          | 2096                    |
| (0, 1, 0)   | 200 ms                  | 0.016          | 1048                    |
| (0, 1, 1)   | 400 ms                  | 0.008          | 524                     |
| (1, 0, 0) to (1, 1, 1)                                | 800 ms                  | 0.004          | 262                     |

- ALS HD and ALS\_NS

These two options enhance the dynamic range by a factor of two each.

With this the sensitivity shown within table 14 will be reduced by the factor 2, but the maximum possible detection range will be doubled for both options. With this the max. detection range goes up to 4192 lx x 2 x 2 = 16 768 lx

- ALS Persistence

The ALS INT is asserted as long as the ALS value is higher or lower than the threshold window when ALS\_PERS (1, 2, 4, 8 times) is set to one time. If ALS\_PERS is set to four times, then the ALS INT will not be asserted if the ALS value is not over (or lower) than the threshold window for four continued refresh times (integration time)

- Programmable PS Threshold

VCNL4030X01 provides both high and low thresholds for PS (register: PS\_THDL, PS\_THDH)

- PS Persistence

The PS persistence function (PS\_PERS, 1, 2, 3, 4) helps to avoid false trigger of the PS INT. For example, if PS\_PERS = 3 times, the PS INT will not be asserted unless the PS value is greater than the PS threshold (PS\_THDH) value for three periods of time continuously

- PS Active Force mode

An extreme power saving way to use PS is to apply PS active force (register: PS\_CONF3 command: PS\_FOR = 1) mode. Anytime host would like to read out just one of PS data, write in '1' at register: PS\_CONF3 command: PS\_FOR\_Trig. Without commands placed, there is no PS data output. VCNL4030X01 stays in standby mode constantly

- PS detection object

Any color of object is detectable by VCNL4030X01

Data Access

All of VCNL4030X01 command registers are readable. To access 16-bit high resolution ALS output data, it is suitable to use read word protocol to read out data by just one command at register: ALS\_DataL and ALS\_DataM. To represent the 16-bit data of ALS, it has to apply two bytes. One byte is for LSB, and the other byte is for MSB as shown in table 18. In terms of reading out 8-bit PS data, it is also very convenient to read PS at register: PS\_Data.

| TABLE 15 - 16-BIT ALS DATA FORMAT |             |    |    |    |    |    |   |   |           |   |   |   |   |   |   |   |
|-----------------------------------|-------------|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|---|
|                                   | VCNL4030X01 |    |    |    |    |    |   |   |           |   |   |   |   |   |   |   |
| Bit                               | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register                          | ALS_DataM   |    |    |    |    |    |   |   | ALS_DataL |   |   |   |   |   |   |   |

### Intelligent Cancellation

VCNL4030X01 provides an intelligent cancellation method to reduce cross talk phenomenon for the proximity sensor. The output data will be subtracted by the input value on register: PS\_CANC.

### Interruption (INT)

VCNL4030X01 has ALS and PS interrupt feature operated by a single pin "INT". The purpose of the interrupt feature is to actively inform the host once INT has been asserted. With the interrupt function applied, the host does not need to be constantly pulling data from the sensor, but to read data from the sensor while receiving interrupt request from the sensor. As long as the host enables ALS interrupt (register: ALS\_INT\_EN) or PS interrupt (register: PS\_INT) function, the level of INT pin (pin 7) is pulled low once INT asserted. All registers are accessible even if INT is asserted.

ALS INT asserted when ALS value cross over the value set by register: ALS\_THDH or lower than the value set by register: ALS\_THDL. To effectively adopt PS INT function, it is recommended to use PS detection mechanism at register: PS\_INTT = 1 for the best PS detection performance which can be adjusted by high / low THD level of PS. PS INT trigger way is defined by register: PS\_INT.

### Interruption Flag

Register: INT\_Flag represents all of interrupt trigger status for ALS and PS. Any flag value changes from '0' to '1' state, the level of INT pin will be pulled low. As long as host reads INT\_Flag data, the bit will change from '1' state to '0' state after reading out, the INT level will be returned to high afterwards.

### PROXIMITY DETECTION LOGIC OUTPUT MODE

VCNL4030X01 provides a proximity detection logic output mode that uses INT pin (pin 7) as a proximity detection logic high / low output (register: PS\_MS). When this mode is selected, the PS output (pin 7; INT/P<sub>out</sub>) is pulled low when an object is closing to be detected and returned to level high when the object moves away. Register: PS\_THDH / PS\_THDL defines how sensitive PS detection is.

One thing to be stated is that whenever proximity detection logic mode applied, INT pin is only used as a logic high / low output. If host would like to use ALS with INT function, register: PS\_MS has to be selected to normal operation mode (PS\_MS = 0). Meanwhile, host has to simulate the GPIO pin as an INT pin function. If not, host needs to periodically reading the state of INT at this GPIO pin.

### PROXIMITY DETECTION HYSTERESIS

A PS detection hysteresis is important that keeps PS state in a certain range of detection distance. For example, PS INT asserts when PS value over PS\_THDH. Host switches off panel backlight and then clears INT. When PS value is less than PS\_THDL, host switches on panel backlight. Any PS value lower than PS\_THDH or higher than PS\_THDL, PS INT will not be asserted. Host does keep the same state.

### APPLICATION CIRCUIT BLOCK REFERENCE

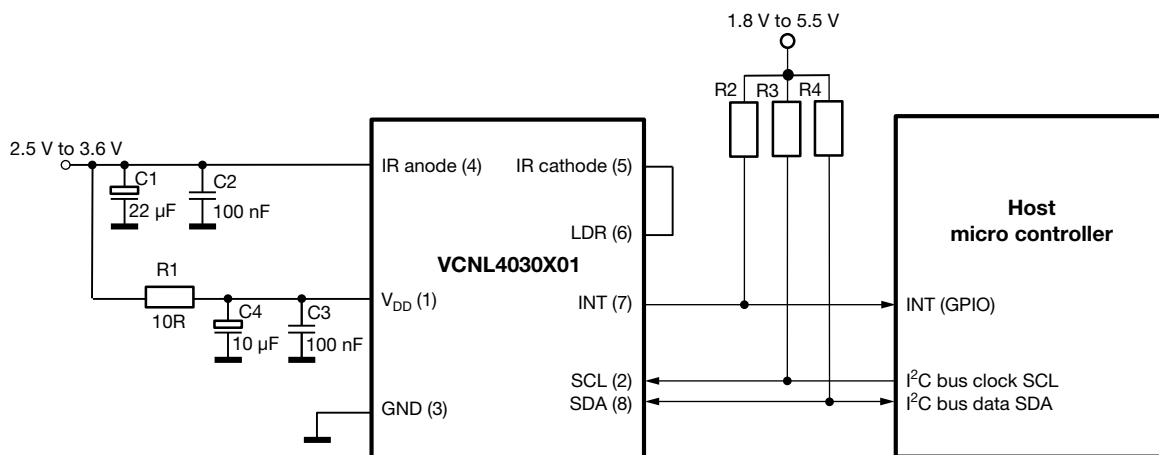
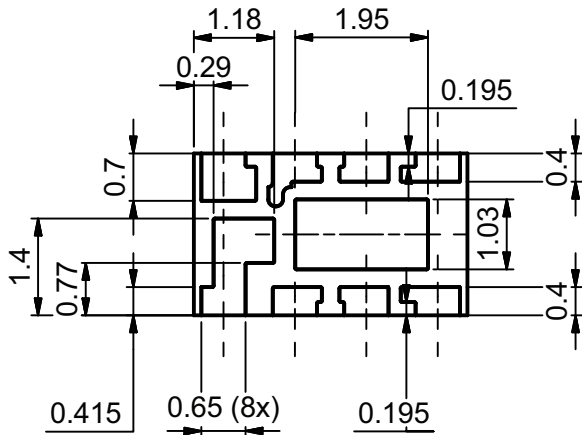


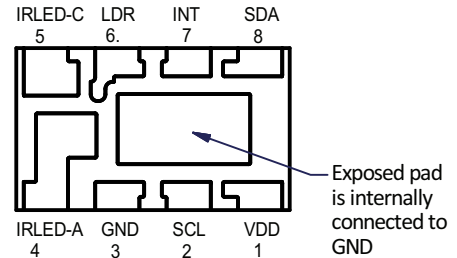
Fig. 18 - Circuitry with Just One Common Power Supply Source



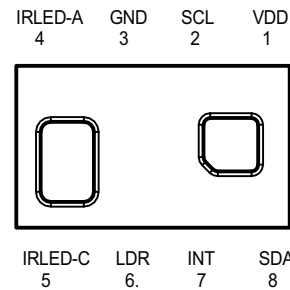
**PACKAGE DIMENSIONS** in millimeters



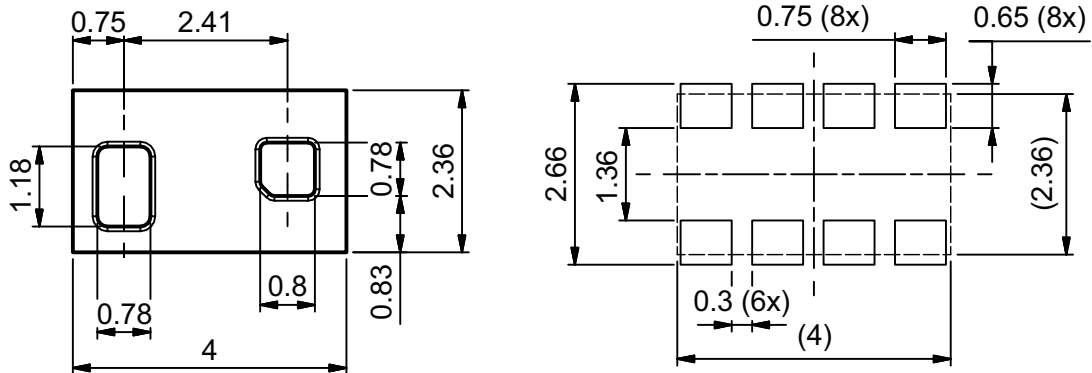
Pinning Bottom View



Pinning Top View

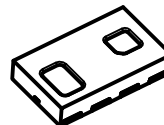


Recommended solder foot print



Drawing No.: 6.550-5326.01-4  
Issue: 1, 21.07.2017

Not indicated tolerances  $\pm 0.1$  mm



Technical drawings according to DIN specification.

**TAPE AND REEL DIMENSIONS** in millimeters

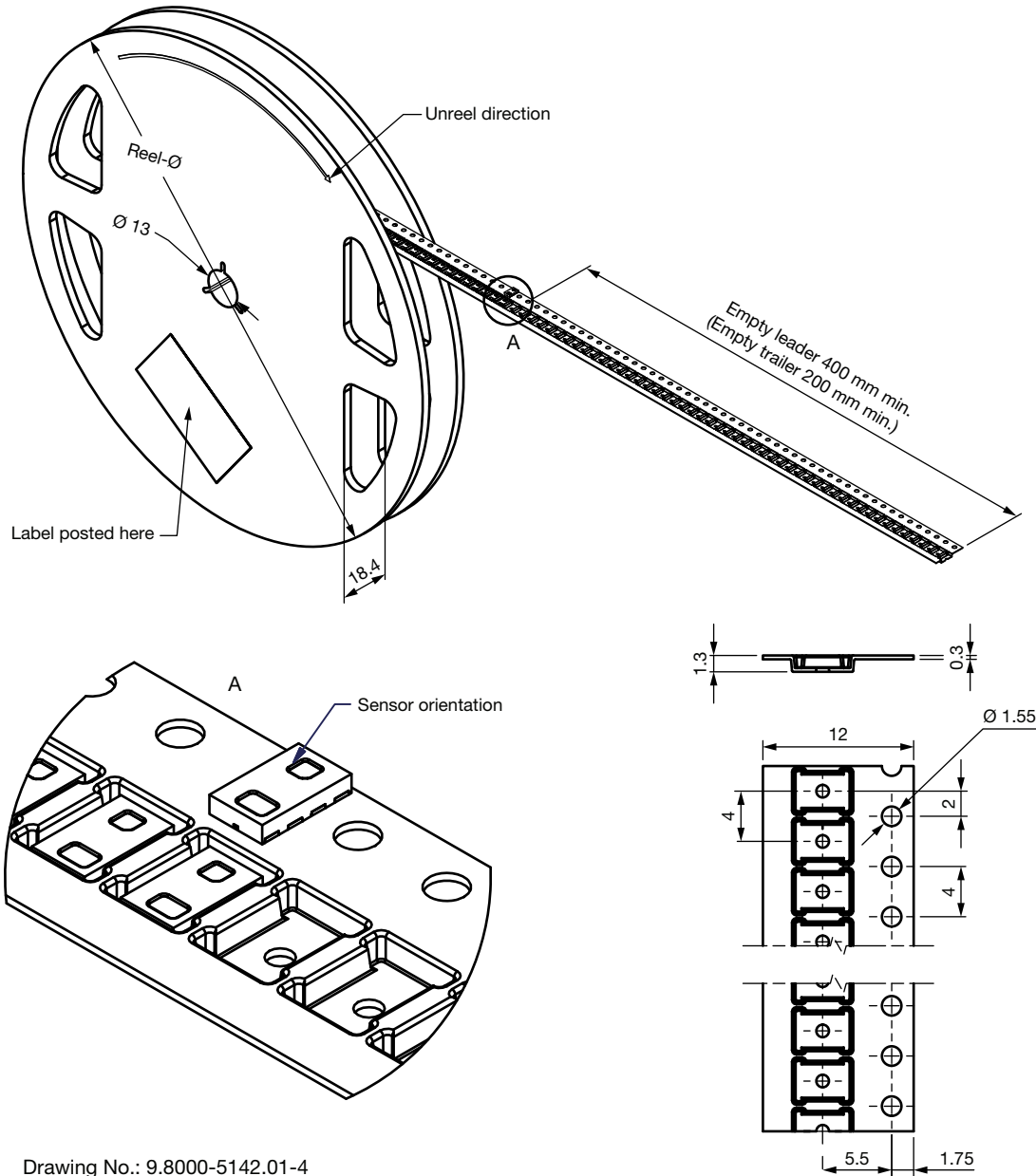
Reel-Size:

GS 08:  $\varnothing$  180 mm  $\pm$  2 mm = 3300 pcs.

GS 18:  $\varnothing$  330 mm  $\pm$  2 mm = 13 000 pcs.

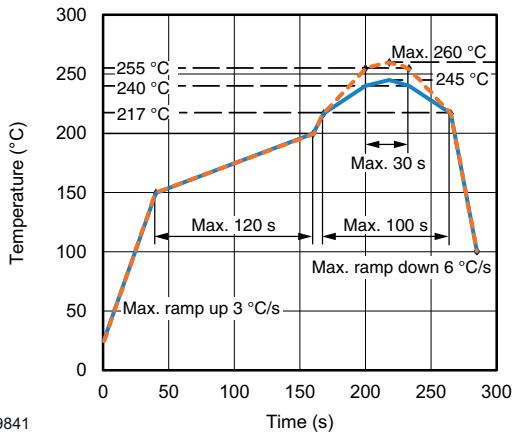
Reel-design is representative for different types

Non tolerated dimensions  $\pm$  0.1 mm



Drawing No.: 9.8000-5142.01-4  
Issue: 1, 07.06.2017

**SOLDER PROFILE**



19841

Fig. 19 - Lead (Pb)-free Reflow Solder Profile According to J-STD-020

**DRYPACK**

Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.

**FLOOR LIFE**

Floor life (time between soldering and removing from MBB) must not exceed the time indicated on MBB label:

Floor life: 168 h

Conditions:  $T_{amb} < 30\text{ °C}$ ,  $RH < 60\%$

Moisture sensitivity level 3, according to J-STD-020.

**DRYING**

In case of moisture absorption devices should be baked before soldering. Conditions see J-STD-020 or label. Devices taped on reel dry using recommended conditions 192 h at  $40\text{ °C} (+ 5\text{ °C})$ ,  $RH < 5\%$ .



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