Dual N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
Channel 1	30	0.0153 at V_{GS} = 10 V	8[e]	8.4
		0.0184 at V_{GS} = 4.5 V	8[e]	
Channel 2	30	0.0280 at V_{GS} = 10 V	8	3.6
		0.0340 at V_{GS} = 4.5 V	7.1	

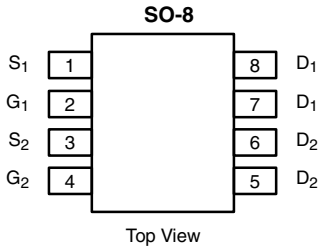
FEATURES

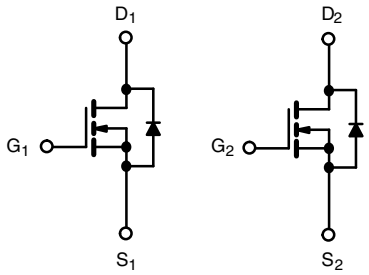
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT

APPLICATIONS

- DC/DC for Notebook PC





Ordering Information: Si4276DY-T1-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		**Symbol**	**Channel 1**	**Channel 2**	**Unit**
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	8[e]	8	A
	T_C = 70 °C		8[e]	6.4	
	T_A = 25 °C		8[b, c, e]	6.8[b, c]	
	T_A = 70 °C		7.6[b, c]	5.5[b, c]	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	50	30	
Source-Drain Current Diode Current	T_C = 25 °C	I_S	3.0	2.3	
	T_A = 25 °C		1.7[b, c]	1.7[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	20	10	
Avalanche Energy		E_{AS}	20	5	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	3.6	2.8	W
	T_C = 70 °C		2.3	1.8	
	T_A = 25 °C		2.1[b, c]	2.0[b, c]	
	T_A = 70 °C		1.3[b, c]	1.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS							
			Channel 1		Channel 2		
Parameter		**Symbol**	**Typical**	**Maximum**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	47	60	58	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady	R_{thJF}	30	35	38	45	

Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under steady state conditions is 107 °C/W (Ch 1) and 110 °C/W (Ch 2).
e. Package limited.

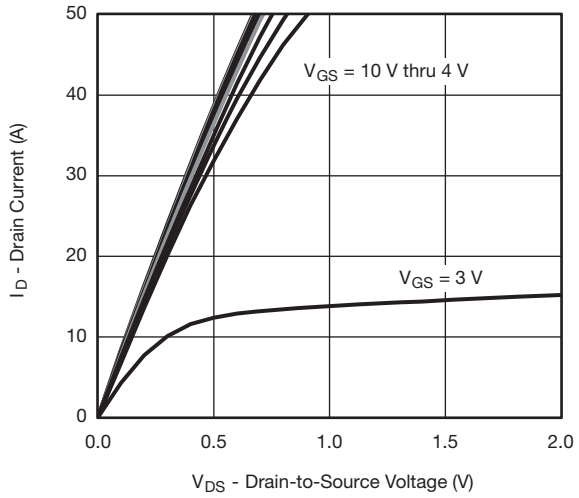
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.[a]**	**Max.**	**Unit**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	Ch 1	30			V
		V_{GS} = 0 V, I_D = 250 µA	Ch 2	30			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	Ch 1		29		mV/°C
		I_D = 250 µA	Ch 2		30		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	Ch 1		- 5.2		
		I_D = 250 µA	Ch 2		- 4.4		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch 1	1.2		2.5	V
		V_{DS} = V_{GS}, I_D = 250 µA	Ch 2	1.2		2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	Ch 1			100	nA
			Ch 2			100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	Ch 1			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V	Ch 2			1	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch 1			10	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch 2			10	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	Ch 1	10			A
		V_{DS} = 5 V, V_{GS} = 10 V	Ch 2	10			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 9.5 A	Ch 1		0.0127	0.0153	Ω
		V_{GS} = 10 V, I_D = 6.8 A	Ch 2		0.0230	0.0280	
		V_{GS} = 4.5 V, I_D = 8.7 A	Ch 1		0.0146	0.0184	
		V_{GS} = 4.5 V, I_D = 6.1 A	Ch 2		0.0280	0.0340	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 9.5 A	Ch 1		43		S
		V_{DS} = 15 V, I_D = 6.8 A	Ch 2		17		
Dynamic[a]							
Input Capacitance	C_{iss}	Channel 1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz Channel 2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch 1		1000		pF
			Ch 2		366		
Output Capacitance	C_{oss}		Ch 1		215		
			Ch 2		82		
Reverse Transfer Capacitance	C_{rss}		Ch 1		85		
			Ch 2		45		
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 9.5 A	Ch 1		17.2	26	nC
		V_{DS} = 15 V, V_{GS} = 10 V, I_D = 6.8 A	Ch 2		7.3	15	
		Channel 1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 9.5 A Channel 2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 6.8 A	Ch 1		8.4	17	
			Ch 2		3.6	8	
Gate-Source Charge	Q_{gs}		Ch 1		3		
			Ch 2		1.1		
Gate-Drain Charge	Q_{gd}		Ch 1		2.6		
			Ch 2		1.3		
Gate Resistance	R_g	f = 1 MHz	Ch 1	0.6	3.1	6.2	Ω
			Ch 2	0.5	2.6	5.2	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**[a]	**Max.**	**Unit**
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	Channel 1 V_{DD} = 15 V, R_L = 2 Ω I_D ≅ 7.6 A, V_{GEN} = 10 V, R_g = 1 Ω Channel 2 V_{DD} = 15 V, R_L = 2.7 Ω I_D ≅ 5.5 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch 1		8	16	ns
			Ch 2		4	8	
Rise Time	t_r		Ch 1		10	20	
			Ch 2		8	16	
Turn-Off DelayTime	$t_{d(off)}$		Ch 1		20	30	
			Ch 2		11	20	
Fall Time	t_f		Ch 1		7	14	
			Ch 2		7	14	
Turn-On Delay Time	$t_{d(on)}$	Channel 1 V_{DD} = 15 V, R_L = 2 Ω I_D ≅ 7.6 A, V_{GEN} = 4.5 V, R_g = 1 Ω Channel 2 V_{DD} = 15 V, R_L = 2.7 Ω I_D ≅ 5.5 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch 1		14	21	
			Ch 2		8	16	
Rise Time	t_r		Ch 1		11	20	
			Ch 2		10	20	
Turn-Off Delay Time	$t_{d(off)}$		Ch 1		18	27	
			Ch 2		10	20	
Fall Time	t_f		Ch 1		7	14	
			Ch 2		7	14	
Drain-Source Body Diode Characteristics							
Continous Source-Drain Diode Current	I_S	T_C = 25 °C	Ch 1			3	A
			Ch 2			2.3	
Pulse Diode Forward Current[a]	I_{SM}		Ch 1			50	
			Ch 2			30	
Body Diode Voltage	V_{SD}	I_S = 7.6 A	Ch 1		0.82	1.2	V
		I_S = 5.5 A	Ch 2		0.85	1.2	
Body Diode Reverse Recovery Time	t_{rr}	Channel 1 I_F = 7.7 A, dI/dt = 100 A/µs, T_J = 25 °C Channel 2 I_F = 5.5 A, dI/dt = 100 A/µs, T_J = 25 °C	Ch 1		20	30	ns
			Ch 2		13	20	
Body Diode Reverse Recovery Charge	Q_{rr}		Ch 1		12	20	nC
			Ch 2		6	12	
Reverse Recovery Fall Time	t_a		Ch 1		11		ns
			Ch 2		7		
Reverse Recovery Rise Time	t_b		Ch 1		9		
			Ch 2		6		

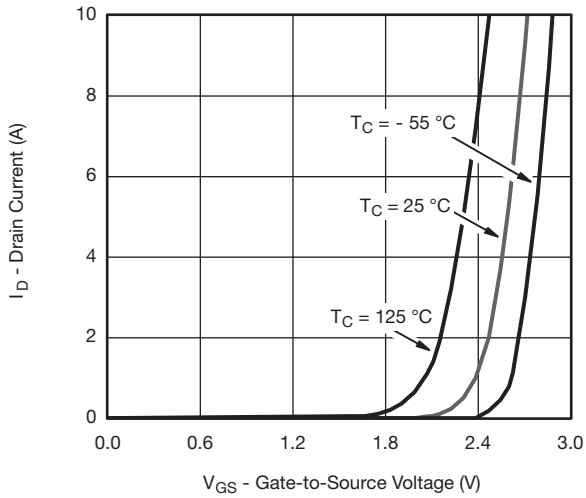
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

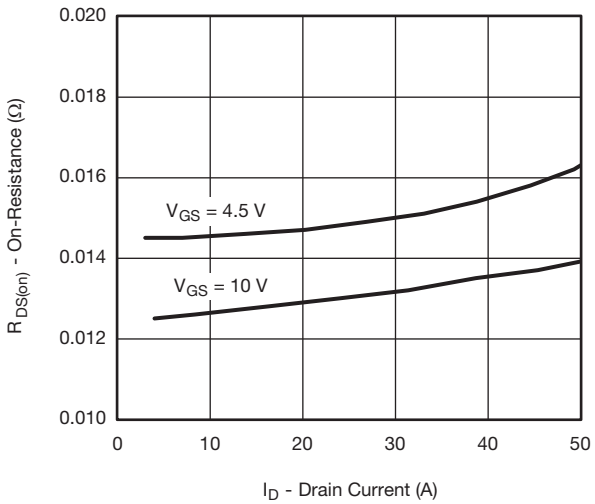
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



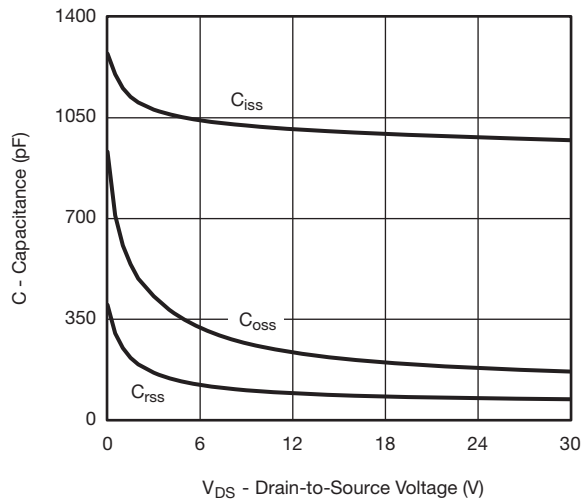
Output Characteristics



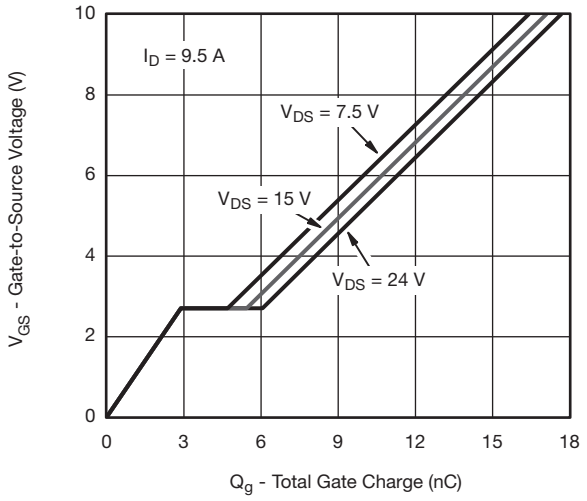
Transfer Characteristics



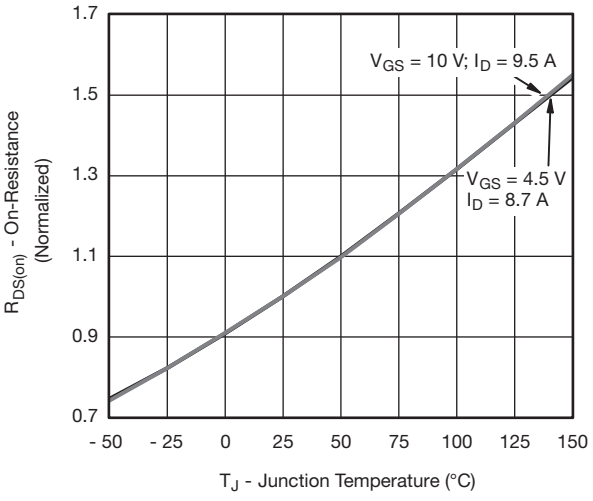
On-Resistance vs. Drain Current



Capacitance

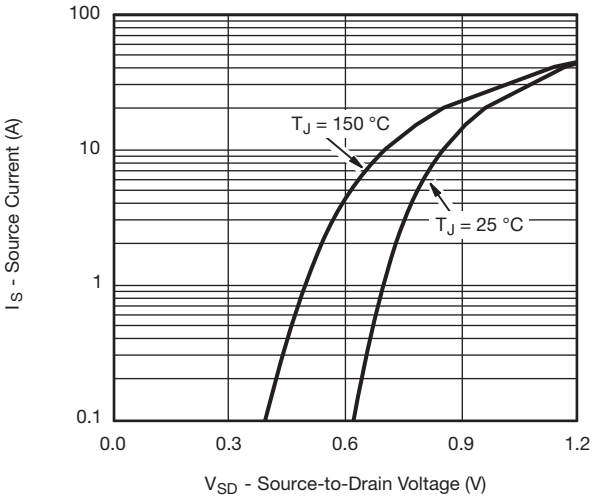


Gate Charge

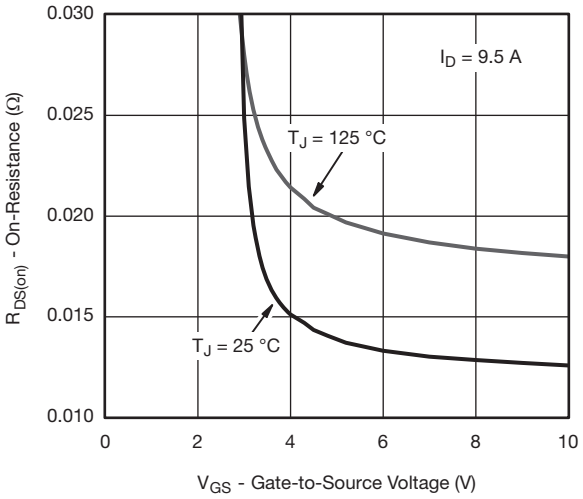


On-Resistance vs. Junction Temperature

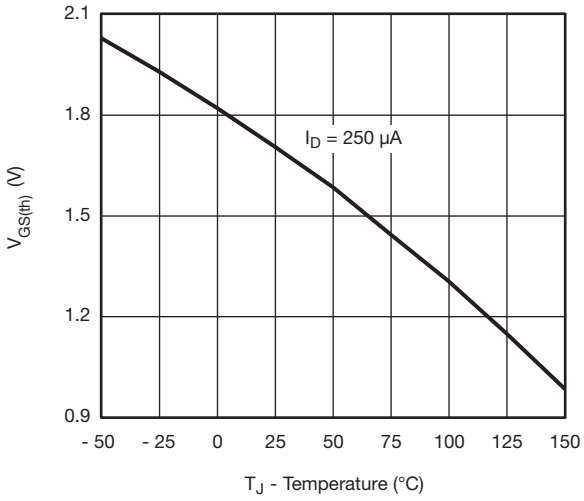
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



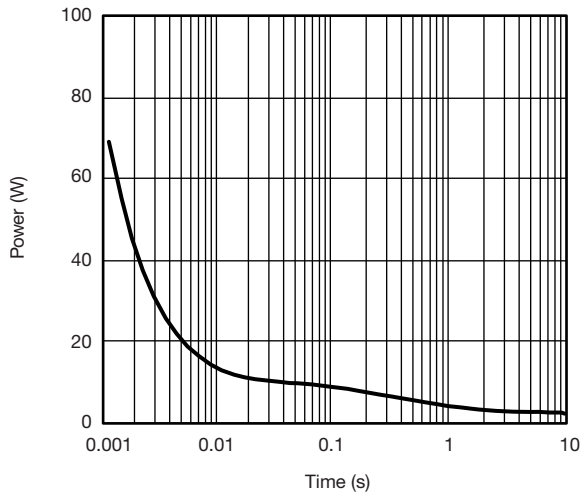
Source-Drain Diode Forward Voltage



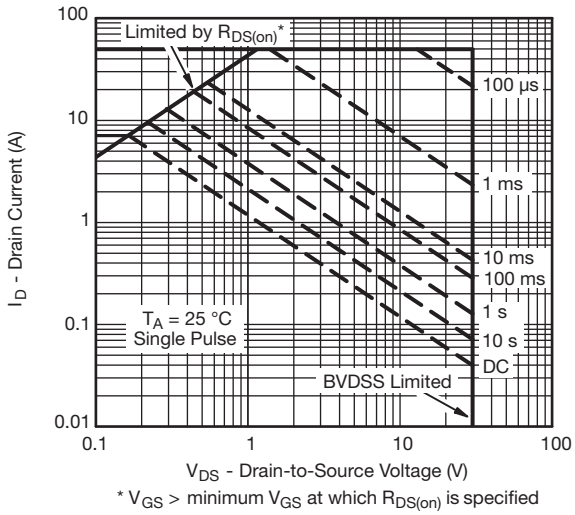
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



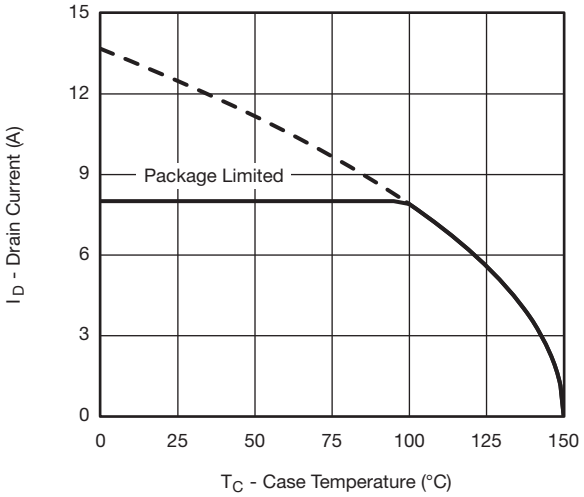
Single Pulse Power, Junction-to-Ambient



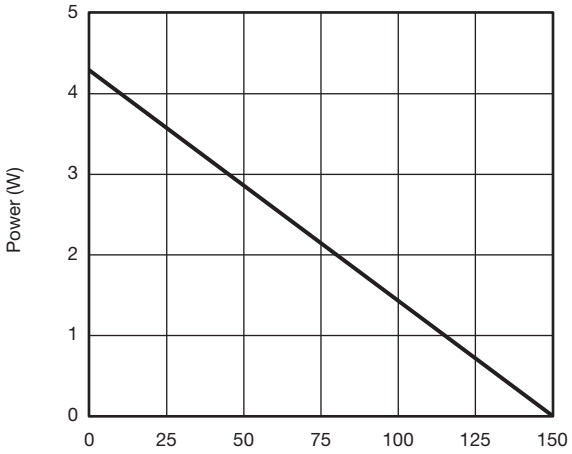
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

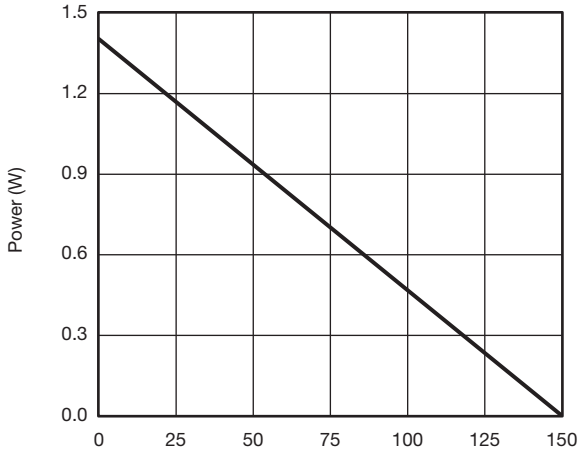
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



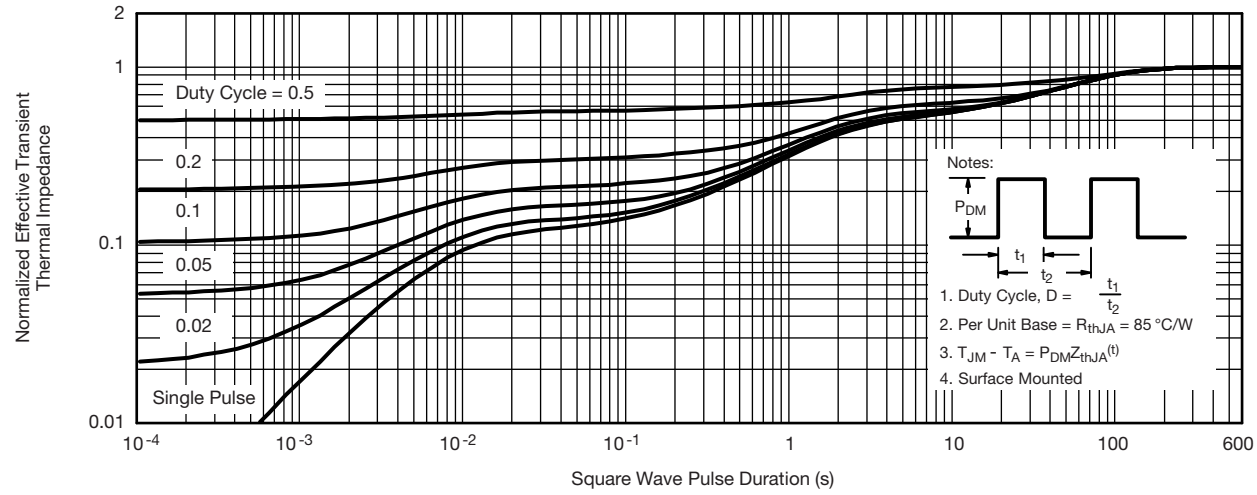
Power Derating, Junction-to-Foot



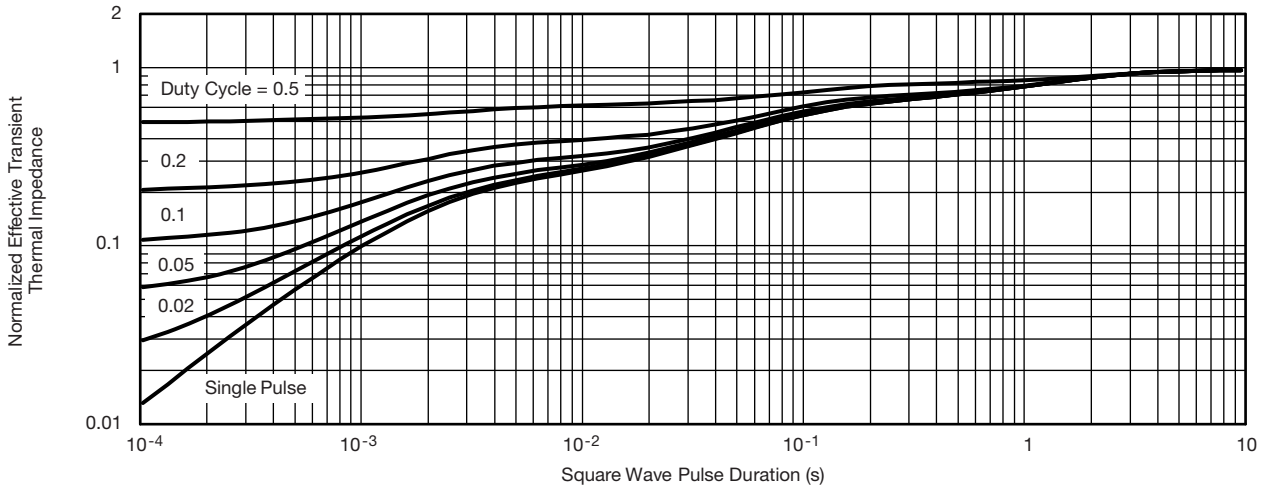
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

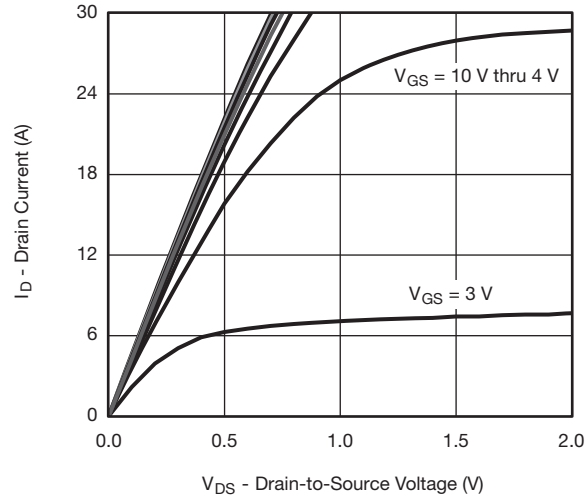


Normalized Thermal Transient Impedance, Junction-to-Ambient

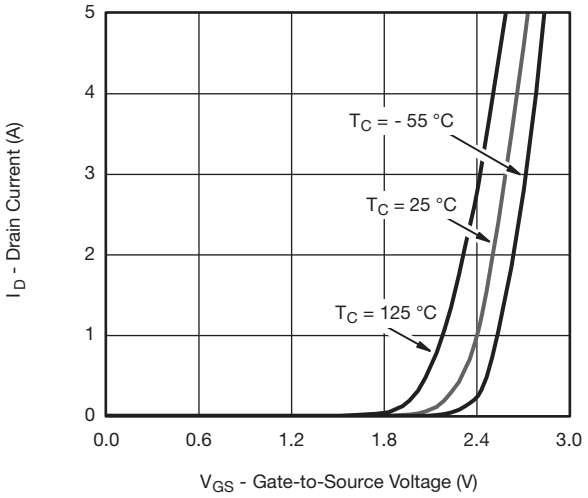


Normalized Thermal Transient Impedance, Junction-to-Foot

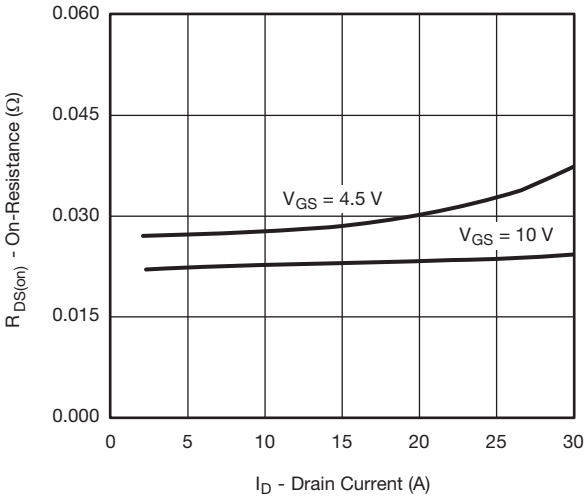
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



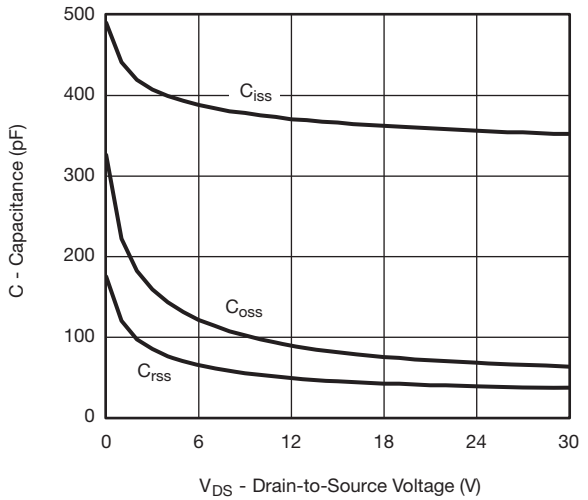
Output Characteristics



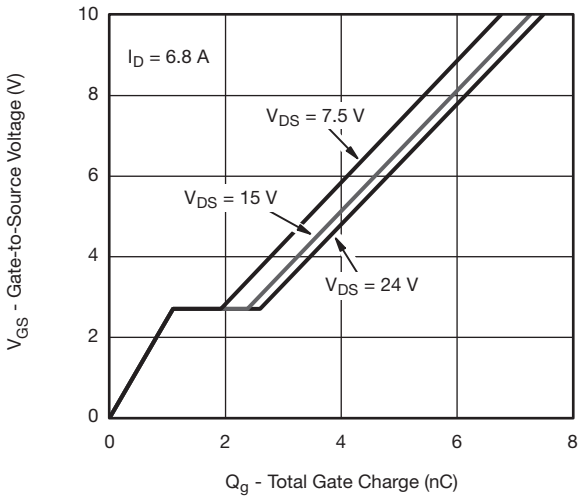
Transfer Characteristics



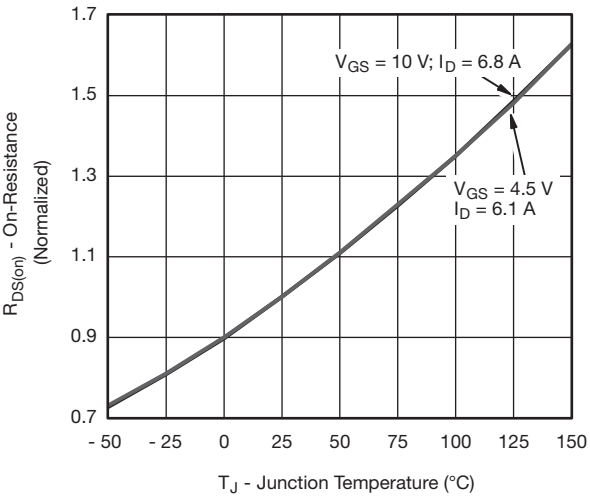
On-Resistance vs. Drain Current



Capacitance

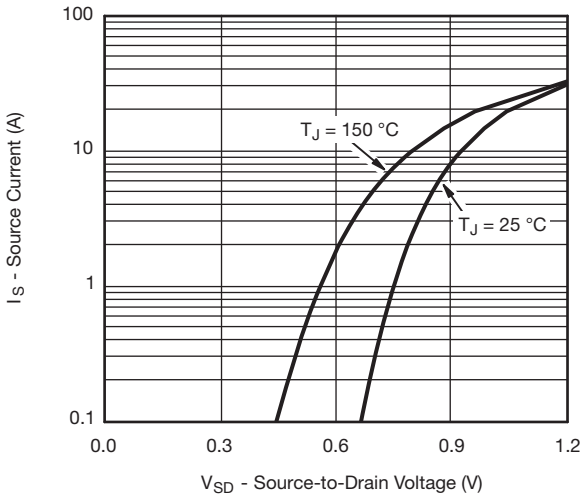


Gate Charge

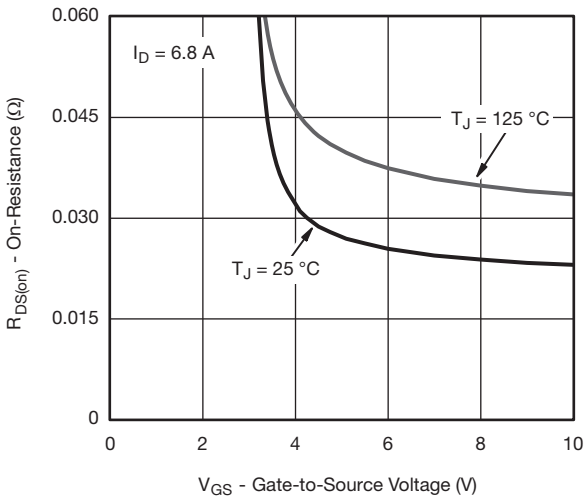


On-Resistance vs. Junction Temperature

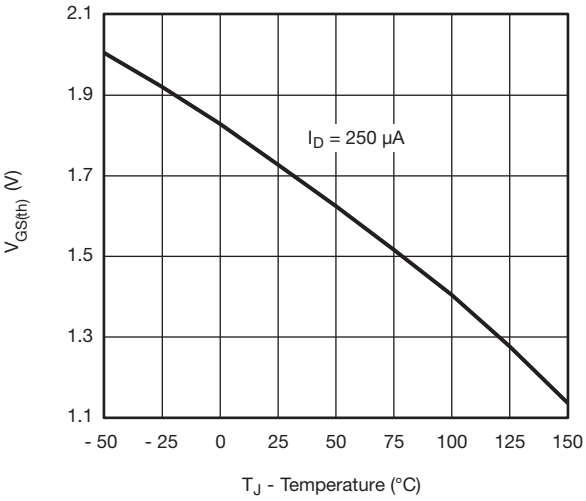
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



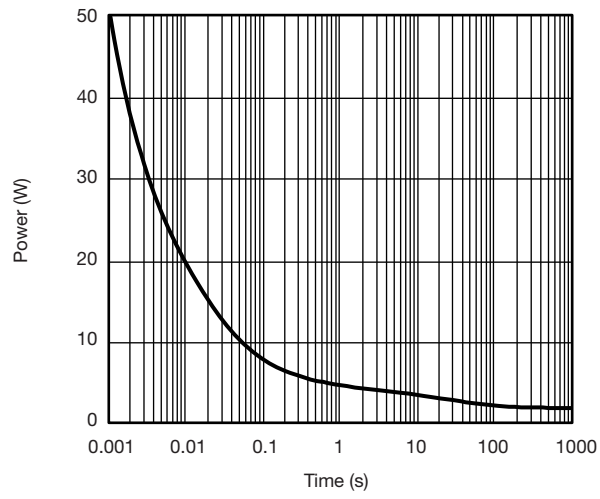
Source-Drain Diode Forward Voltage



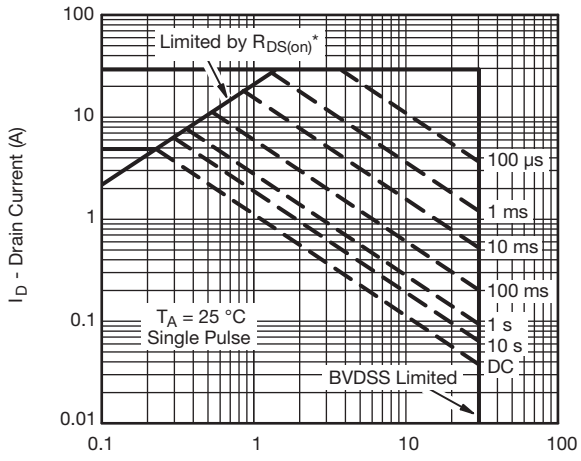
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



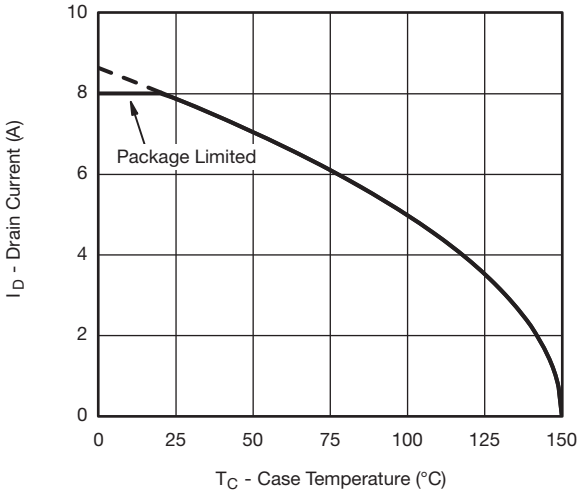
Single Pulse Power, Junction-to-Ambient



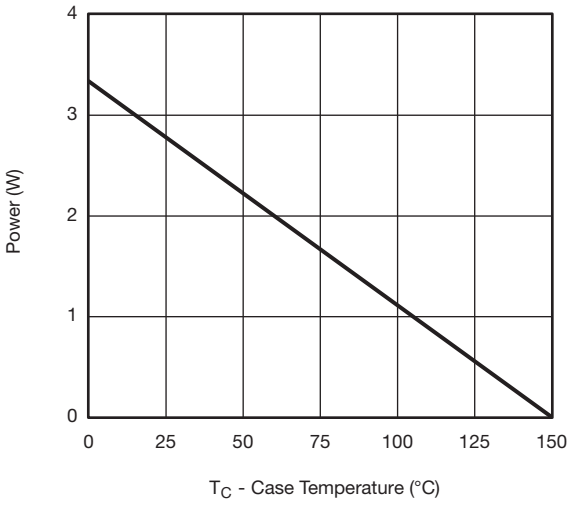
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

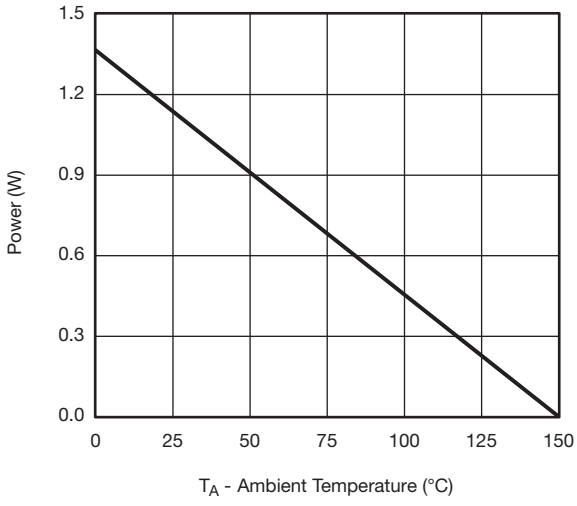
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



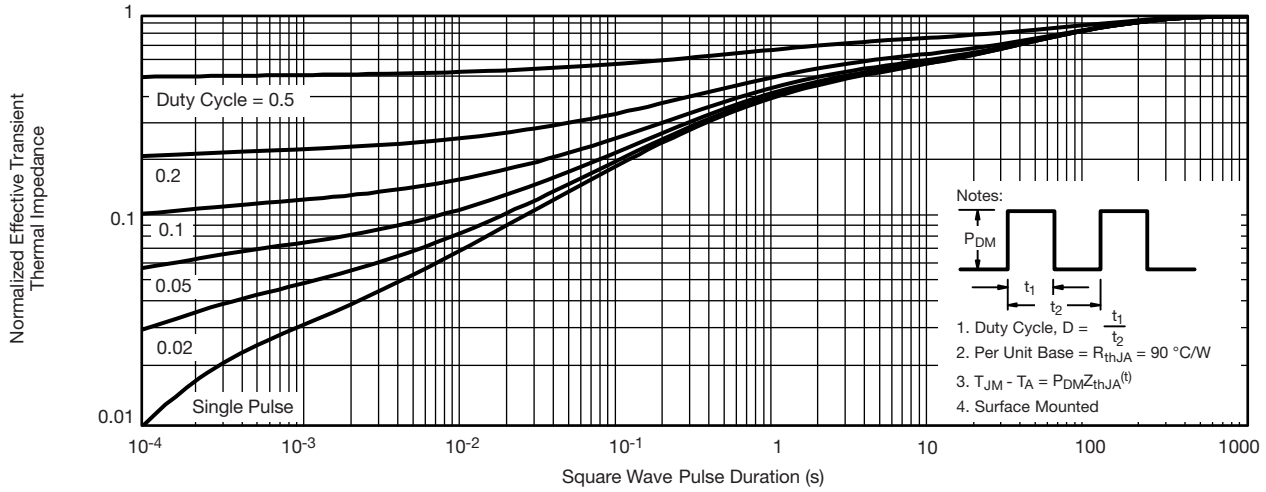
Power Derating, Junction-to-Foot



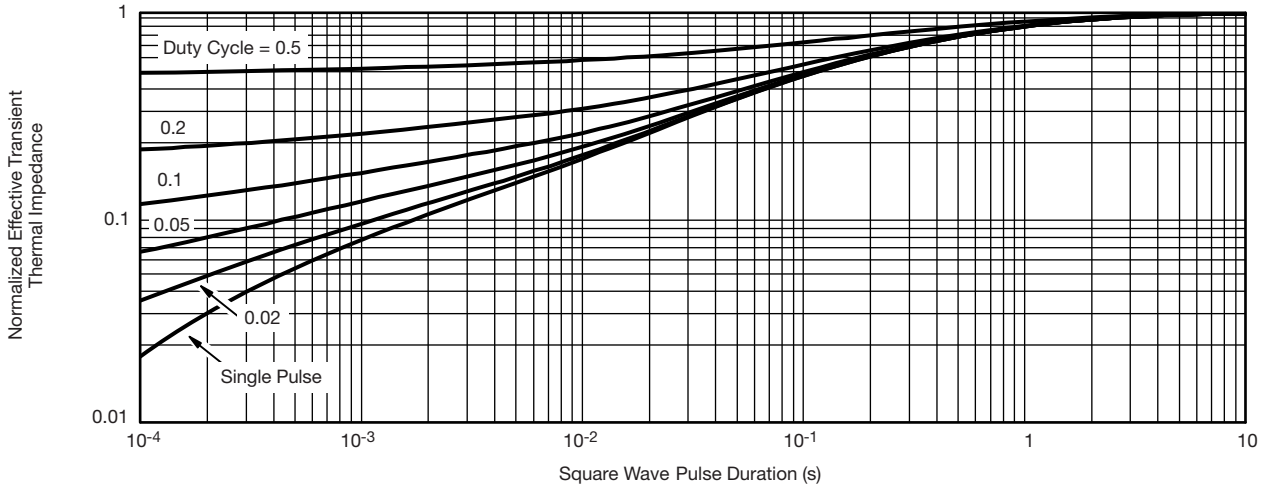
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



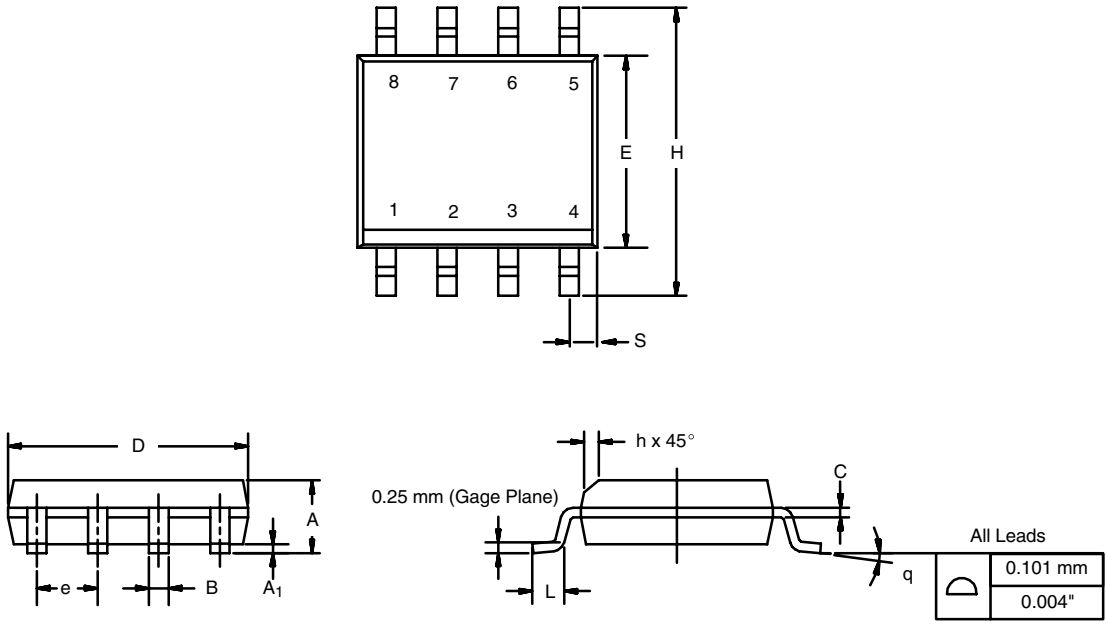
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

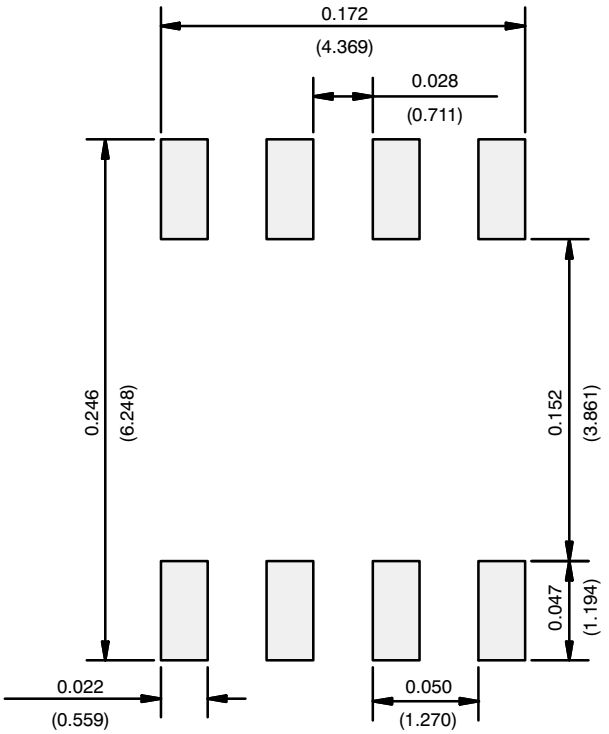
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations.

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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