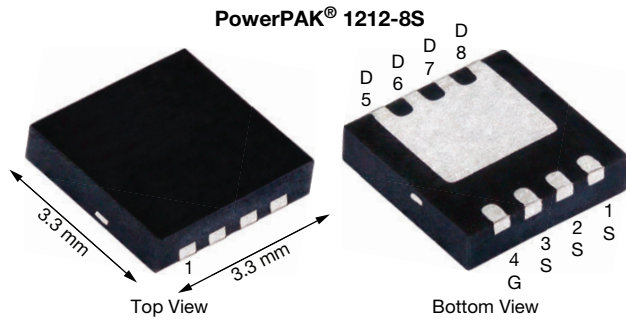


## N-Channel 20 V (D-S) MOSFET



PRODUCT SUMMARY	
$V_{DS}$ (V)	20
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0039
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 3.7$ V	0.0042
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5$ V	0.0058
$Q_g$ typ. (nC)	22.5
$I_D$ (A)	50 f, g
Configuration	Single

### FEATURES

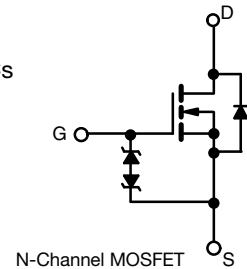
- TrenchFET® power MOSFET
- 100 %  $R_g$  and UIS tested
- Low thermal resistance PowerPAK package with small size and 0.75 mm profile
- Typical ESD performance 3400 V
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Battery switch / load switch
- Power management for tablet PCs and mobile computing



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiS612EDNT-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	20	V
Gate-source voltage	$V_{GS}$	$\pm 12$	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	50 <sup>g</sup>
		$T_C = 70$ °C	50 <sup>g</sup>
		$T_A = 25$ °C	24.6 <sup>a, b</sup>
		$T_A = 70$ °C	19.7 <sup>a, b</sup>
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	200	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	3.1 <sup>a, b</sup>
Single pulse avalanche current	$I_{AS}$	20	mJ
Single pulse avalanche energy	$E_{AS}$	20	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	52
		$T_C = 70$ °C	33
		$T_A = 25$ °C	3.7 <sup>a, b</sup>
		$T_A = 70$ °C	2.4 <sup>a, b</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c, d</sup>		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>a, e</sup>	$t \leq 10$ s	$R_{thJA}$	24	33	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	1.9	2.4	

### Notes

- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 81 °C/W
- Based on  $T_C = 25$  °C
- Package limited



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	18	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>		-	-3.5	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1 mA	0.5	-	1.2	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V	-	-	± 10	μA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 4.5 V	-	-	± 1	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	-	-	1	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	20	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 14 A	-	0.0032	0.0039	Ω
		V <sub>GS</sub> = 3.7 V, I <sub>D</sub> = 14 A	-	0.0035	0.0042	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 13 A	-	0.0041	0.0058	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 14 A	-	50	-	S
<b>Dynamic<sup>b</sup></b>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	2060	-	pF
Output capacitance	C <sub>oss</sub>		-	558	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	365	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	46	70	nC
		V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	-	22.5	34	
Gate-source charge	Q <sub>gs</sub>		-	4.1	-	
Gate-drain charge	Q <sub>gd</sub>		-	5.3	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.2	1	2	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	16	24	ns
Rise time	t <sub>r</sub>		-	65	98	
Turn-off delay time	t <sub>d(off)</sub>		-	40	60	
Fall time	t <sub>f</sub>		-	12	20	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	9	18	
Rise time	t <sub>r</sub>		-	5	10	
Turn-off delay time	t <sub>d(off)</sub>		-	34	51	
Fall time	t <sub>f</sub>		-	4	8	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	50	A
Pulse diode forward current (t = 100 μs)	I <sub>SM</sub>		-	-	200	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.75	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	22	44	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	10	20	nC
Reverse recovery fall time	t <sub>a</sub>		-	11	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	11	-	

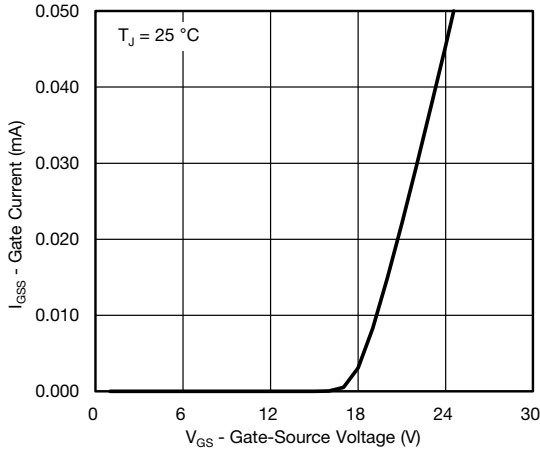
**Notes**

- a. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2 %  
b. Guaranteed by design, not subject to production testing

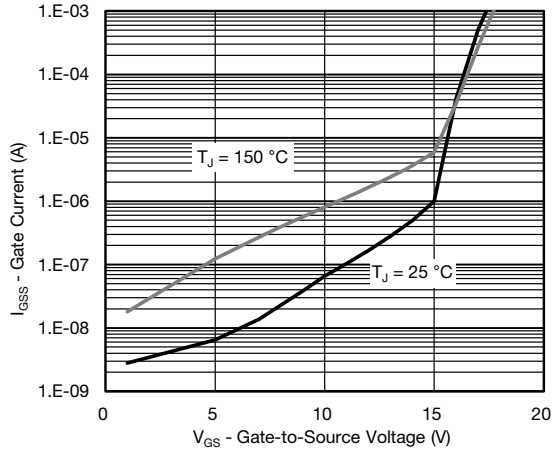
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



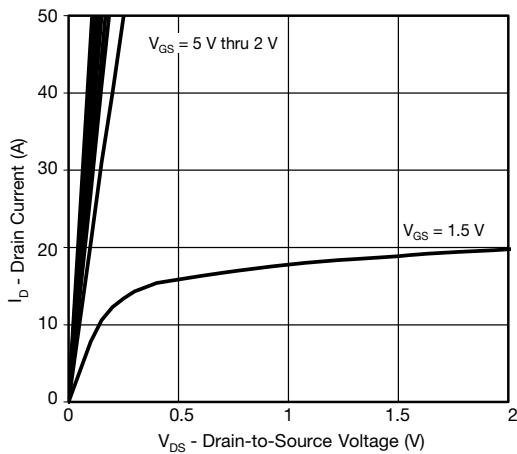
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



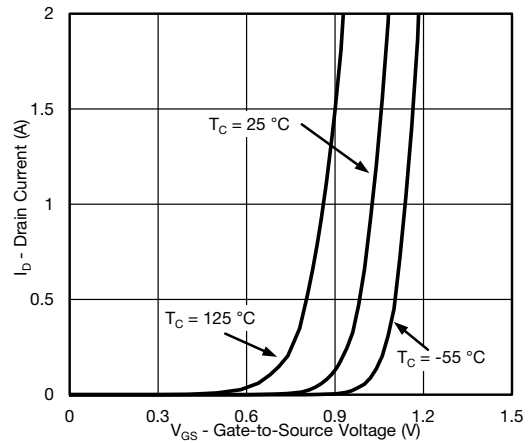
Gate Current vs. Gate-to-Source Voltage



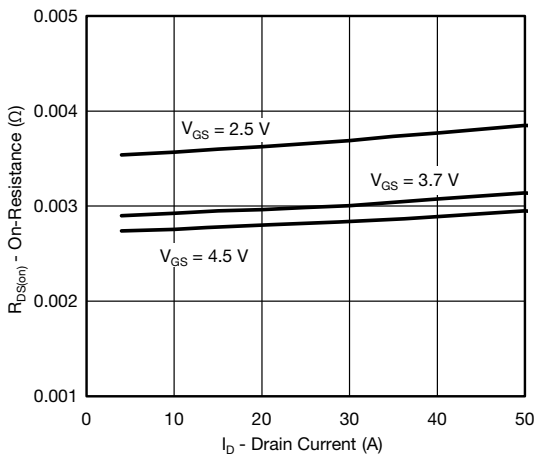
Gate Current vs. Gate-to-Source Voltage



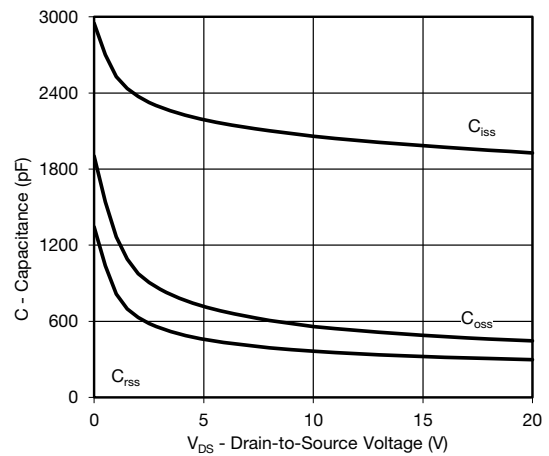
Output Characteristics



Transfer Characteristics



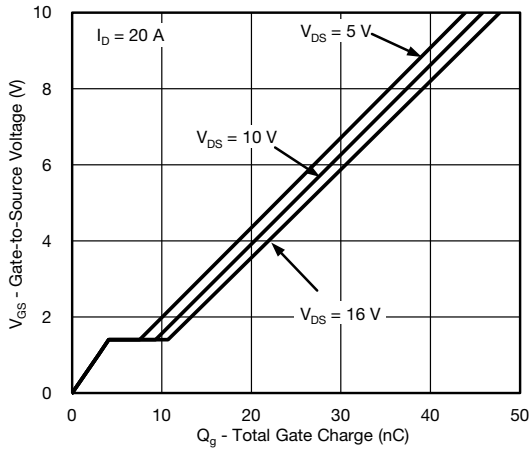
On-Resistance vs. Drain Current and Gate Voltage



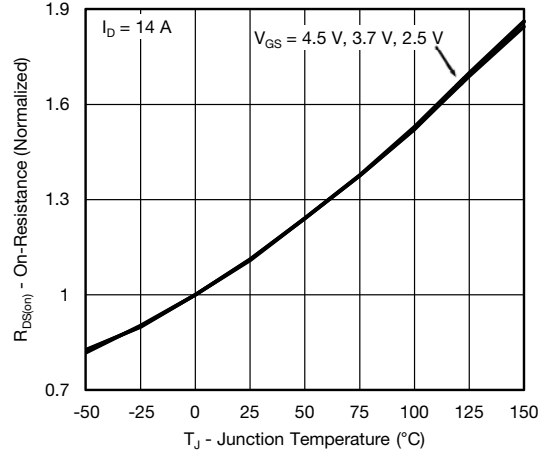
Capacitance



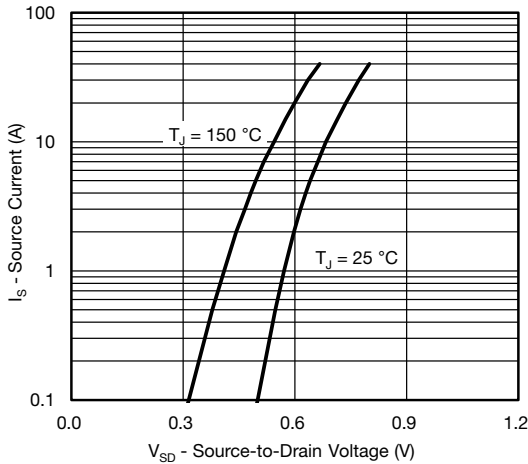
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



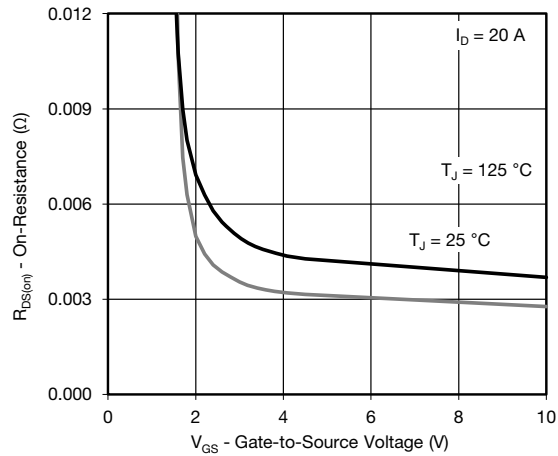
Gate Charge



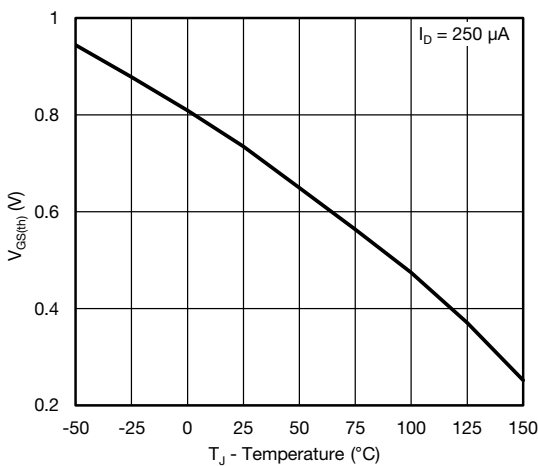
On-Resistance vs. Junction Temperature



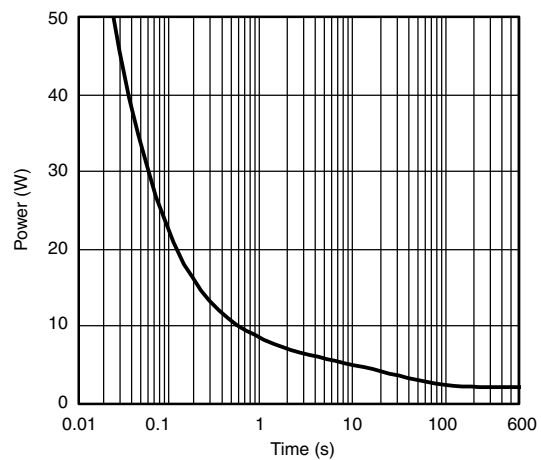
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



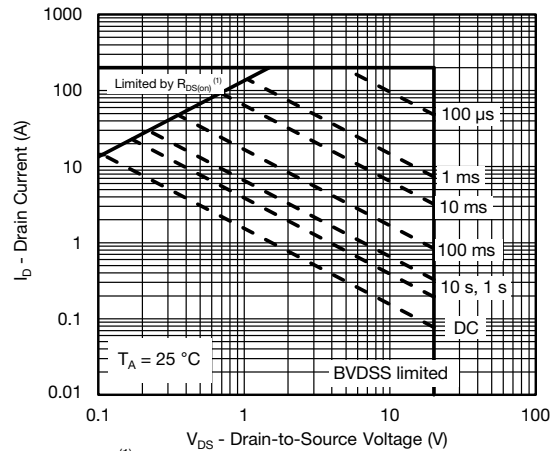
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

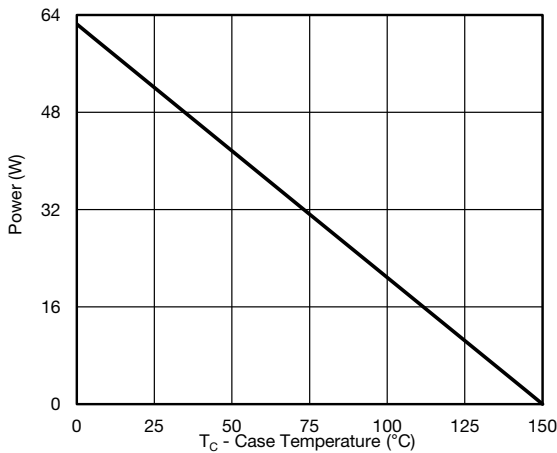


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

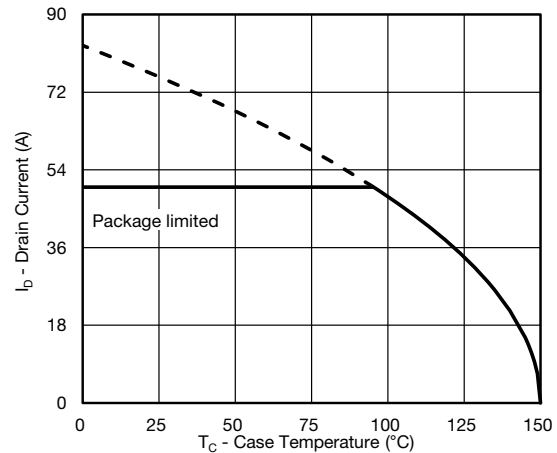


(1)  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area



Power, Junction-to-Case



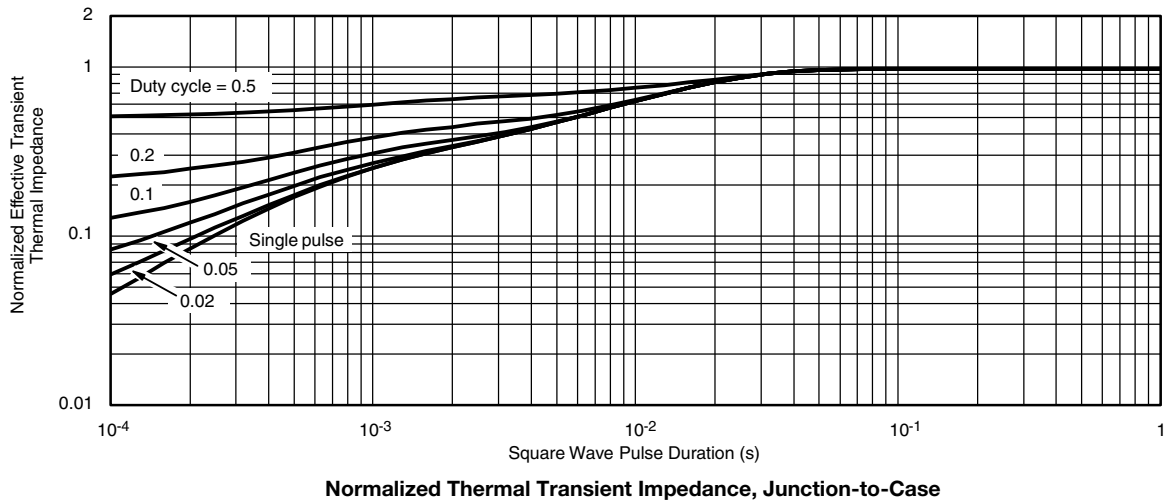
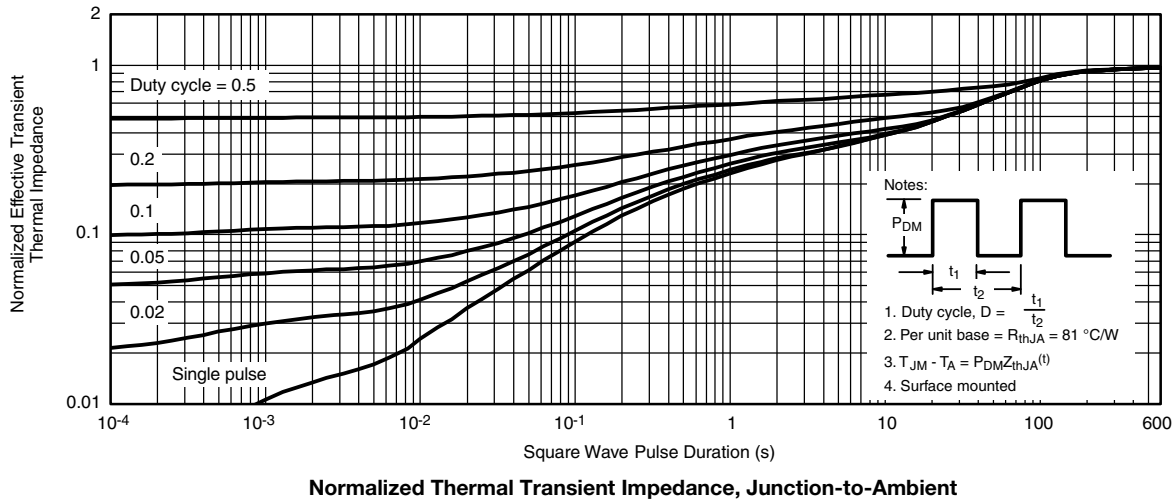
Current Derating <sup>a</sup>

Note

- a. The power dissipation  $P_D$  is based on  $T_J \text{ max.} = 150 \text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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