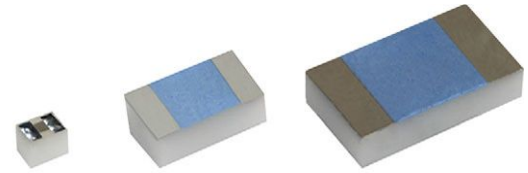
AEC-Q200 Qualified
High Frequency 70 GHz Thin Film Chip Resistor



CH02016 (flip chip) CH0402 (flip chip) CH0603 (flip chip)

LINKS TO ADDITIONAL RESOURCES

3D Models | S-Parameters | Simulation Tools | Application Notes | Capabilities and Custom Options | Did You Know? | Infographics | Why It Matters

Those miniaturized components are designed in such a way that their internal reactance is very small. When correctly mounted and utilized, they function as almost pure resistors on a very large range of frequency, up to 50 GHz, and 70 GHz for CH02016 from 50 Ω to 100 Ω.

FEATURES

- Operating frequency 70 GHz
- AEC-Q200 qualified (CH02016 flip chip only)
- Thin film microwave resistors
- Flip chip, wraparound or one face termination
- Small size, down to 20 mils by 16 mils
- Edged trimmed block resistors
- Pure alumina substrate (99.5 %)
- Ohmic range: 10R to 500R
- Design kits available
- Modelithics® library available
- Small internal reactance (LC down to 1 x 10^{-24})
- Tolerance 1 %, 2 %, 5 %
- TCR: 100 ppm/°C in (-55 °C, +155 °C) temperature range
- TCR: 50 ppm/°C available upon request for 10 Ω to150 Ω ohmic range
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

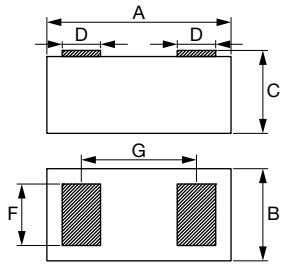
Pb-free RoHS COMPLIANT HALOGEN FREE GREEN (5-2008)

STANDARD ELECTRICAL SPECIFICATIONS

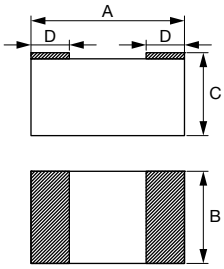
MODEL	SIZE	RESISTANCE RANGE Ω	RATED POWER Pn W	LIMITING ELEMENT VOLTAGE V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
CH02016	02016	10 to 500	0.030	30	1, 2, 5	100 (50 upon request)
CH0402	0402	10 to 500	0.050	37	1, 2, 5	100 (50 upon request)
CH0603	0603	10 to 500	0.125	50	1, 2, 5	100 (50 upon request)

DIMENSIONS in millimeters (inches)

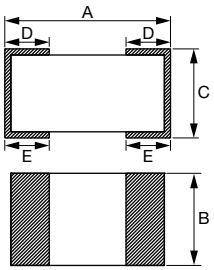
CH02016 F / CH02016 P / CH0402 P / CH0603 P



CH0402 F / CH0603 F



CH0402 N / CH0402 G /CH0603 N / CH0603 G



CASE SIZE / MODEL / TERMINATION	DIMENSIONS A ± 0.10 (± 0.004)	B ± 0.10 (± 0.004)	C ± 0.127 (± 0.005)	D E when applicable MIN.	D E when applicable MAX.	F ± 0.050 (± 0.002)	G ± 0.050 (± 0.002)
CH02016 F CH02016 P	0.480 (0.020)	0.390 (0.016)	0.420 (0.016) (1)	0.110 (0.004)	0.150 (0.006)	0.260 (0.010)	0.300 (0.012)
CH0402 F CH0402 N CH0402 G	1.000 (0.040)	0.600 (0.023)	0.500 (0.020)	0.150 (0.006)	0.350 (0.014)	n/a	n/a
CH0402 P	1.200 (0.047)	0.600 (0.023)	0.500 (0.020)	0.110 (0.004)	0.150 (0.006)	0.320 (0.013)	0.880 (0.035)
CH0603 F CH0603 N CH0603 G	1.520 (0.060)	0.750 (0.030)	0.500 (0.020)	0.250 (0.010)	0.510 (0.020)	n/a	n/a
CH0603 P	1.720 (0.068)	0.750 (0.030)	0.500 (0.020)	0.235 (0.009)	0.275 (0.011)	0.660 (0.026)	1.355 (0.053)

Note

(1) ± 0.070 (± 0.003)

TOLERANCE VS. OHMIC VALUES		
Ohmic range	10 Ω ≤ *R* < 50 Ω	50 Ω ≤ *R* ≤ 500 Ω
Tolerance CH02016	5 %	1 % for 50 Ω and 100 Ω, 2 %, 5 %
Tolerance CH0402 and CH0603	2 %, 5 %	1 %, 2 %, 5 %

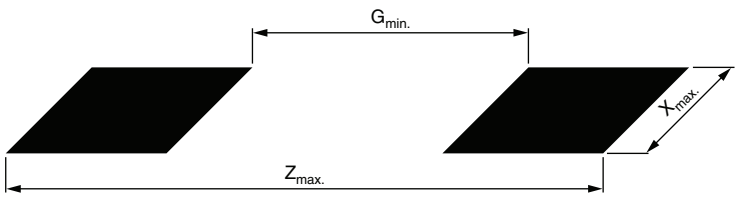
LAND PATTERN FOR F "FLIP CHIP" TERMINATIONS in millimeters (inches)

CHIP SIZE	$Z_{max.}$	$X_{max.}$	$G_{min.}$
02016	0.53 (0.021)	0.44 (0.017)	0.15 (0.006)
0402	1.40 (0.055)	0.65 (0.026)	0.40 (0.016)
0603	1.71 (0.067)	0.90 (0.035)	0.76 (0.030)

Note

- Suggested land pattern: according to IPC-7351

LAND PATTERN FOR N AND G WRAPAROUND TERMINATIONS in millimeters (inches)



CHIP SIZE	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0402	1.55 (0.061)	0.15 (0.006)	0.73 (0.029)
0603	2.37 (0.093)	0.35 (0.014)	0.98 (0.039)

Dimension and tolerance of land pattern shall be defined by PCB designer; PCB can be designed according to IPC-7351A "Generic Requirements for Surface Mount Design and Land Pattern Standard"

PERFORMANCE (CH02016 F TERMINATION)

TEST PROCEDURES AND REQUIREMENTS				
AEC-Q200 CLAUSE	TEST	PROCEDURE	GLOBAL PERFORMANCES	TYPICAL PERFORMANCES (25 Ω TO 250 Ω)
3	High temperature exposure	MIL-STD-202 method 108 1000 h at T = 125 °C, unpowered	± 2 % ± 0.05 Ω	± 0.2 % ± 0.05 Ω
4	Temperature cycling	JESD22 method JA-104 1000 cycles (-55 °C to +155 °C)	± 5 % ± 0.05 Ω	± 1 % ± 0.05 Ω
7	Biased humidity	MIL-STD-202 method 103 1000 h 85 °C / 85 % RH 10 % of operating power	± 2 % ± 0.05 Ω	± 0.75 % ± 0.05 Ω

TEST PROCEDURES AND REQUIREMENTS				
AEC-Q200 CLAUSE	**TEST**	**PROCEDURE**	**GLOBAL PERFORMANCES**	**TYPICAL PERFORMANCES (25 Ω TO 250 Ω)**
8	Operational life	MIL-STD-202 method 108 Condition D steady state T = 125 °C at rated power 90' on / 30' off / 1000 h	± 2.5 % ± 0.05 Ω	± 1 % ± 0.05 Ω
13	Mechanical shock	MIL-STD-202 method 213 condition C 100 *g*/6 ms 3.75 m/s 3 shock/direction, 2 directions along 3 axes (18 shocks)	± 0.05 % ± 0.05 Ω	± 0.015 % ± 0.05 Ω
14	Vibration	MIL-STD-202 method 204 5 g for 20 min, 12 cycles each of 3 orientations Test from 10 Hz to 2000 Hz	± 0.1 % ± 0.05 Ω	± 0.05 % ± 0.05 Ω
15	Resistance to soldering heat	MIL-STD-202 method 210 condition D Flux used: alpha 611 Solder temp.: 260 °C ± 5 °C Total immersion during 10 s	± 2.5 % ± 0.05 Ω	± 0.5 % ± 0.05 Ω
17	ESD	AEC-Q200-002	Classification 1C 1000 V_{DC} to 2000 V_{DC}	
18	Solderability	J-STD-002 - Preconditioning 4 h dry heat aging and 235 °C SnPb 5 s - 215 °C SnPb 5 s - 260 °C SnAgCu 10 s	Good tinning (≥ 95 % covered) No visible damage	
20	Flammability	UL 94	Class V-0 No burning	
21	Board flex	AEC-Q200-005	± 0.1 % ± 0.05 Ω	± 0.05 % ± 0.05 Ω
24	Flame retardance	AEC-Q200-001	No flame, no explosion, no temperature higher than 350 °C	

PREFERRED MODELS AND VALUES

Vishay Sfernice highly recommend to use the smallest sizes and flip chip version to get the best performances.

Recommended Values:

10R/18R/25R/50R/75R/100R/150R/180R/200R/250R/330R /500R

Those values are available with a **MOQ of 100 pieces.**

Other values can be ordered upon request, but higher MOQ will apply: 1000 pieces for CH02016, 500 pieces for CH0402, 250 pieces for CH0603.

Recommended termination:

F

Recommended tolerance:

2 %

DESIGN KITS

Design kits are available Ex Stock in CH02016 and CH0402 sizes. There are 20 pieces per recommended value. F termination. 5 % tolerance.

Those kits are packaged in pieces of tape and delivered in ESD bags.

PACKAGING

Standard packaging is plastic tape and reel for all sizes.
Paper tape and reel is available for sizes 0402 and 0603.
Waffle pack is available for all sizes.

Depending on the type of terminations, parts will be packed differently:

One face:

- Gold terminations: (P termination option): active face up
- Tin / silver terminations: (F termination option): active face down in tape and reel
  active face up in waffle pack

Note

- Please refer to Vishay Sfernice Application Note “Guidelines for Vishay Sfernice Resistive and Inductive Products” for soldering recommendation (document number 52029, 3. Guidelines for Surface Mounting Components (SMD), profile number 3 applies

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
		WAFFLE PACK 2" x 2"	TAPE AND REEL		
			MIN.	MAX.	
02016	See MOQ mentioned on preferred models and values	484	100	5000	8 mm
0402		100			
0603		100			

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover. To get “not stacked up” waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code.

Tape and Reel

See Part Numbering information to get the quantity desired by tape.

In regard to the CH02016 size only, up to 5 empty cavities can be found every 1000 parts in the reel. Nevertheless, the number of requested parts will be respected.

GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: CH0402-50RJF (preferred part number format)

C	H	0	4	0	2	-	5	0	R	J	F	T		9	9	9

GLOBAL MODEL	SIZE	OHMIC VALUE	TOLERANCE	TERMINATION	PACKAGING	OPTION
CH	**02016** **0402** **0603**	**10R to 500R**	**F** = 1 % **G** = 2 % **J** = 5 %	**F** (flip chip): SnAg over nickel barrier **N** (W/A): SnAg over nickel barrier (except 02016) **P** (one face): (1) gold bonding pads **G** (W/A): gold over nickel barrier (except 02016)	For more information see Codification of Packaging table	From 1 to 3 digits. Leave blank if no option.

Historical Part Number example: **CH02016-100RGFPT1K (tapes of 1K pieces)**
CH0402-50RJF (waffle pack)

CHKIT Part Numbers (2): **CHKIT-02016**
CHKIT-0402

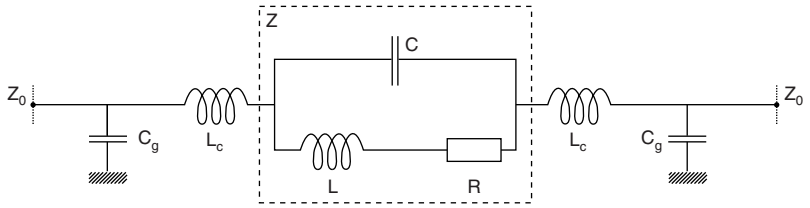
Notes

- Historical part numbers are not recommended but can still be used for ordering

(1) Gold termination for application in hermetic package. Can also be mounted on PCB with SnAg solder paste
(2) CHKIT for 0603 size is not available

CODIFICATION OF PACKAGING	
WAFFLE PACK (available for all sizes)	
W	100 min., 1 mult.
PLASTIC TAPE (standard packaging for all sizes)	
T	100 min., 1 mult.
TA	100 min., 100 mult.
TB	250 min., 250 mult.
TC	500 min., 500 mult.
TD	1000 min., 1000 mult.
TE	2500 min., 2500 mult.
TF	Full tape (quantity depending on size of chips)
PAPER TAPE (available for 0402 and 0603)	
PT	100 min., 1 mult.
PA	100 min., 100 mult.
PB	250 min., 250 mult.
PC	500 min., 500 mult.
PD (not available for size 0402)	1000 min., 1000 mult.
PE (not available for size 0402)	2500 min., 2500 mult.
PF (not available for size 0402)	Full tape (quantity depending on size of chips)

TYPICAL HIGH FREQUENCY PERFORMANCE ELECTRICAL MODEL



C	Internal shunt capacitance
L	Internal inductance
R	Resistance
Z	Internal impedance (R, L, C)
L_c	External connection inductance
C_g	External capacitance to ground

The complex impedance of the chip resistor is given by the following equations:

$$Z = \frac{R + j\omega(L - R^2C - L^2C\omega^2)}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]}$$

$$\frac{[Z]}{R} = \frac{1}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]} \times \sqrt{1 + \left[\frac{\omega(L - R^2C - L^2C\omega^2)}{R}\right]^2}$$

$$\theta = \tan^{-1}\frac{\omega(L - R^2C - L^2C\omega^2)}{R}$$

Notes

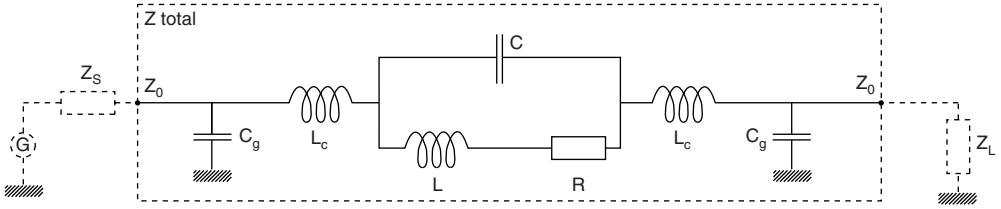
- $\omega = 2 \times \pi \times f$
- f: frequency

R, L and C are relevant to the chip resistor itself.
L_c and C_g also depend on the way the chip resistor is mounted.
It is important to notice that after assembly the external reactance of L_c and C_g will be combined to internal reactance of L and C. This combination can upgrade or downgrade the HF behavior of the component.
This is why we are displaying three sets of data:

- $\frac{[Z]}{R}$ versus frequency curves which aim to show at a glance the intrinsic HF performance of a given chip resistor
- $\frac{[Z_{total}]}{R}$ versus frequency curves which aim to show the behavior of the chip resistor when mounted

These lines are terminated with adapted source and load impedance respectively Z_s and Z_l with $Z_0 = Z_L = Z_s$ (for others configurations please consult us).

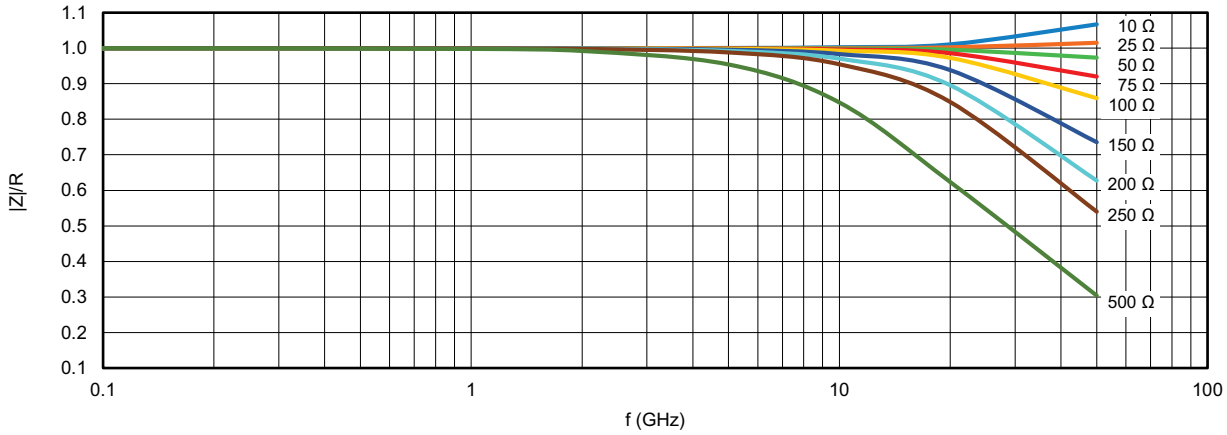
Equivalent circuit for S-parameters:



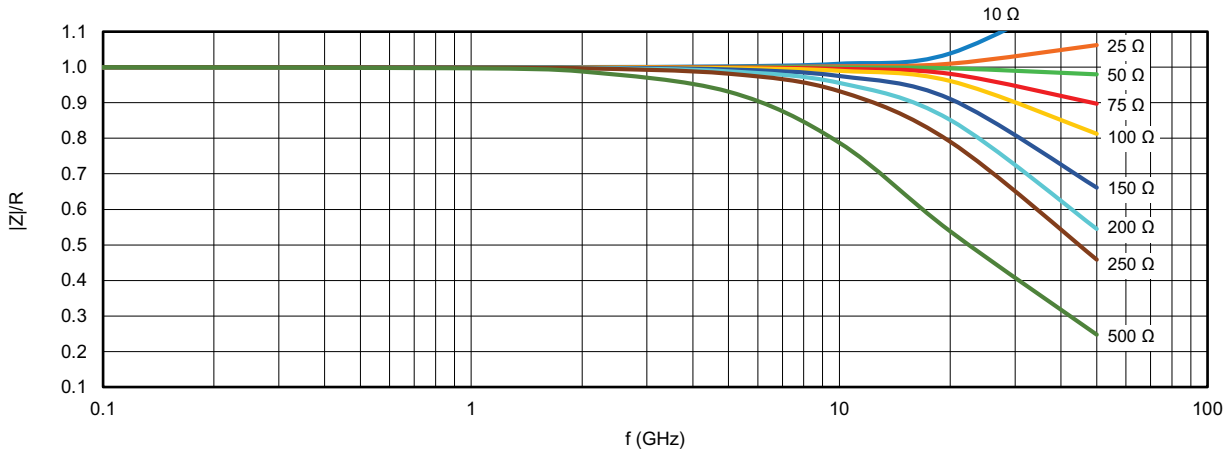
S-parameters are computed taking into account all the resistive, inductive and capacitive elements (Z total) and $Z_0 = Z_L = Z_s = R$.

For simulation purposes, those S-parameter data are available for download here: www.vishay.com/doc?53061

INTERNAL IMPEDANCE CURVES

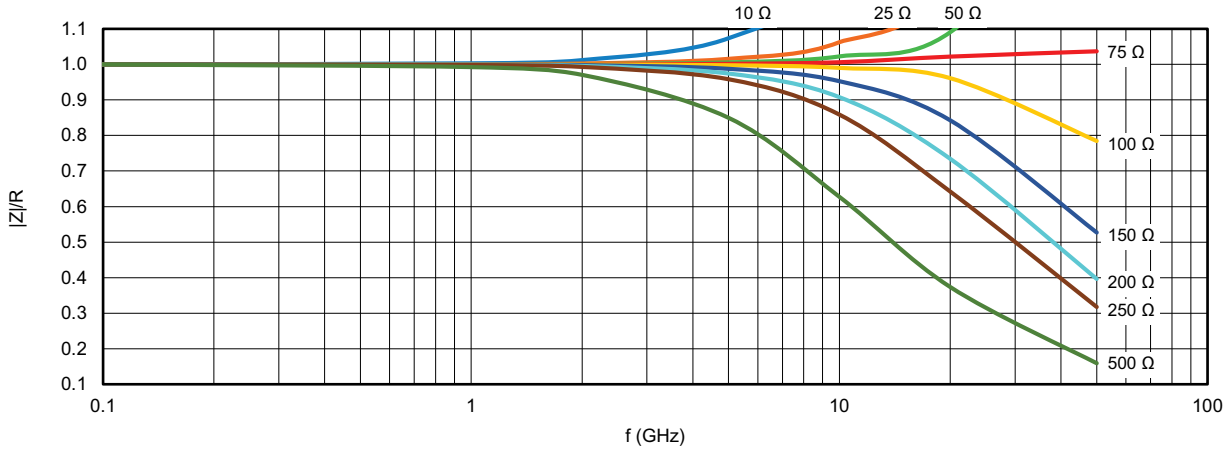


Internal impedance curve for 02016 size (F and P terminations)

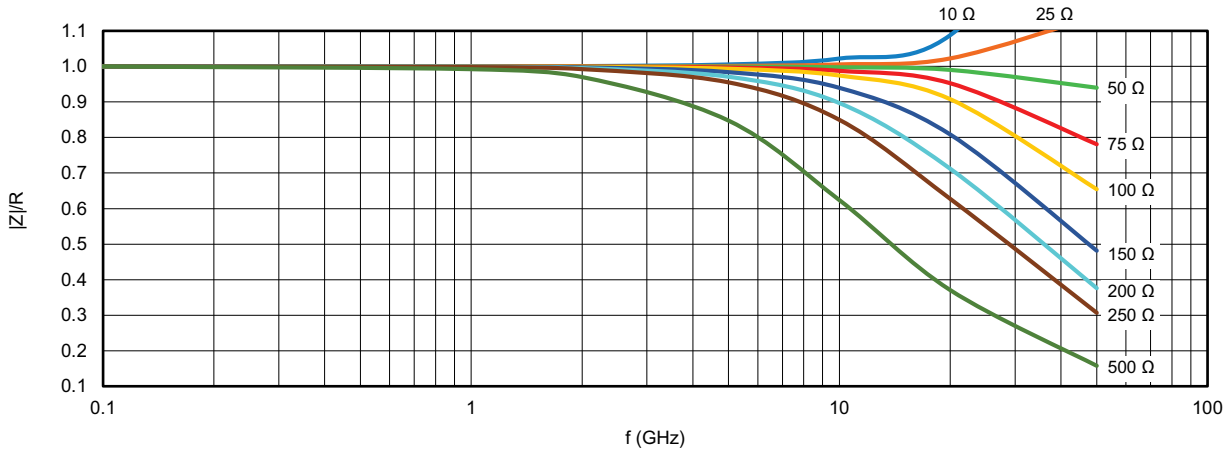


Internal impedance curve for 0402 size (F and P terminations)

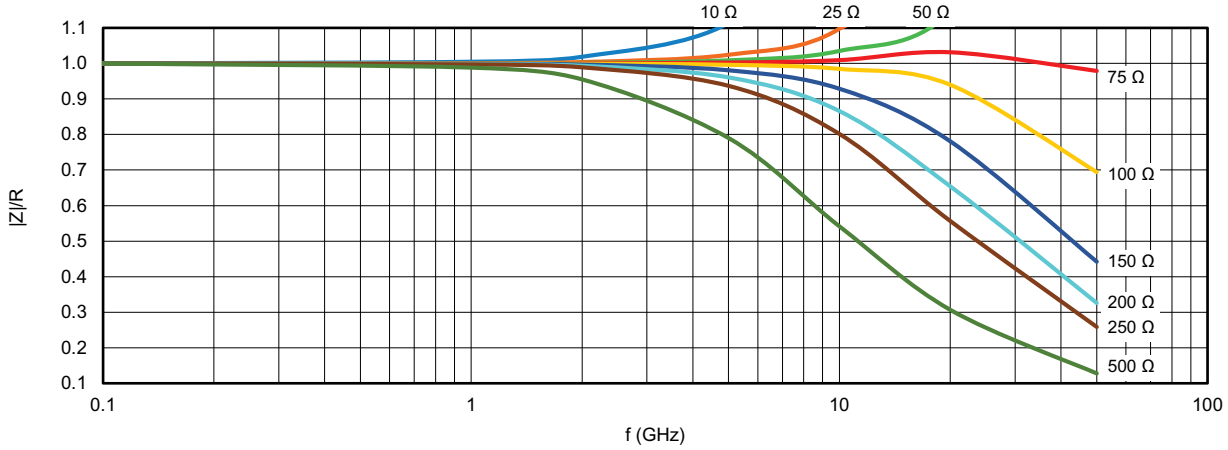
INTERNAL IMPEDANCE CURVES



Internal impedance curve for 0402 size (N and G terminations)

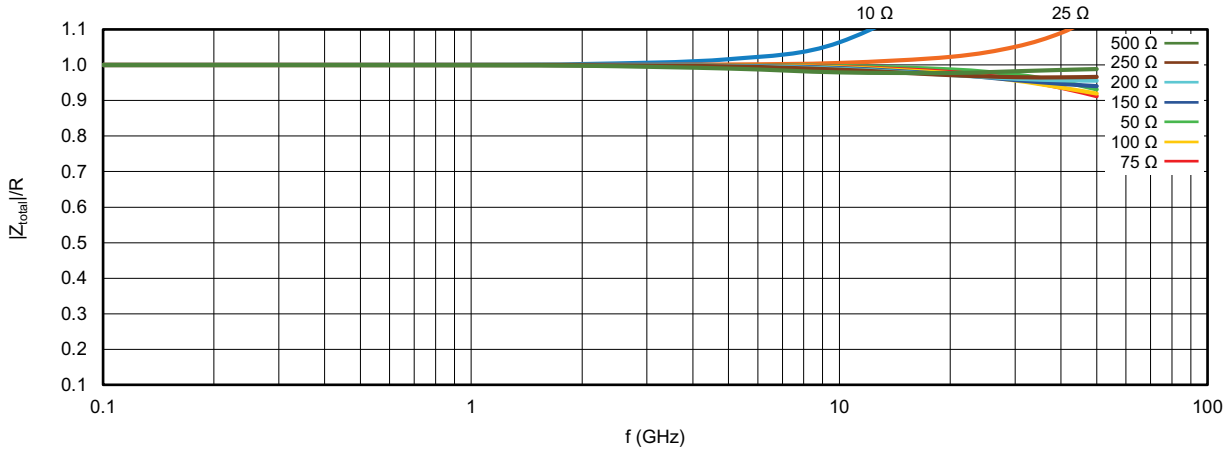


Internal impedance curve for 0603 size (F and P terminations)

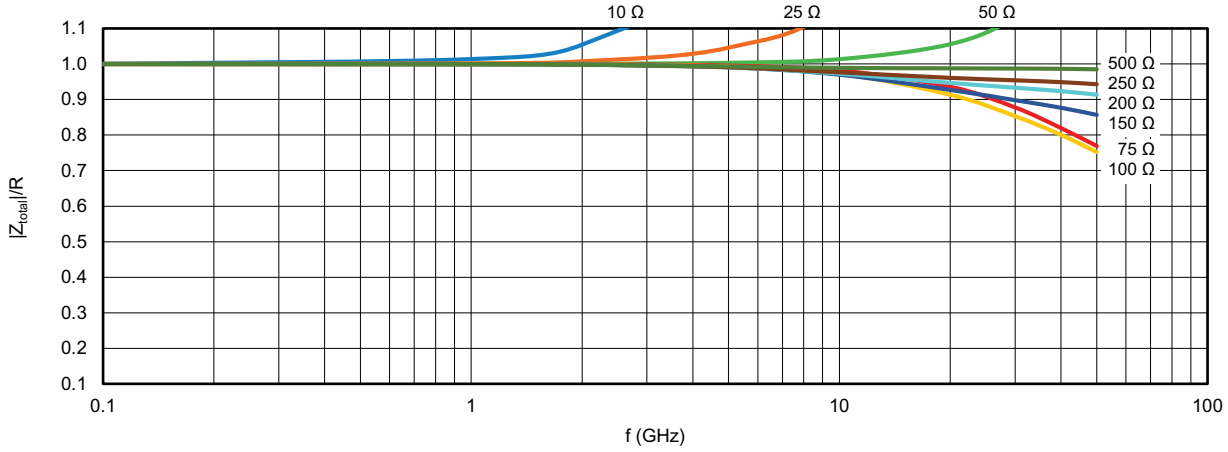


Internal impedance curve for 0603 size (N and G terminations)

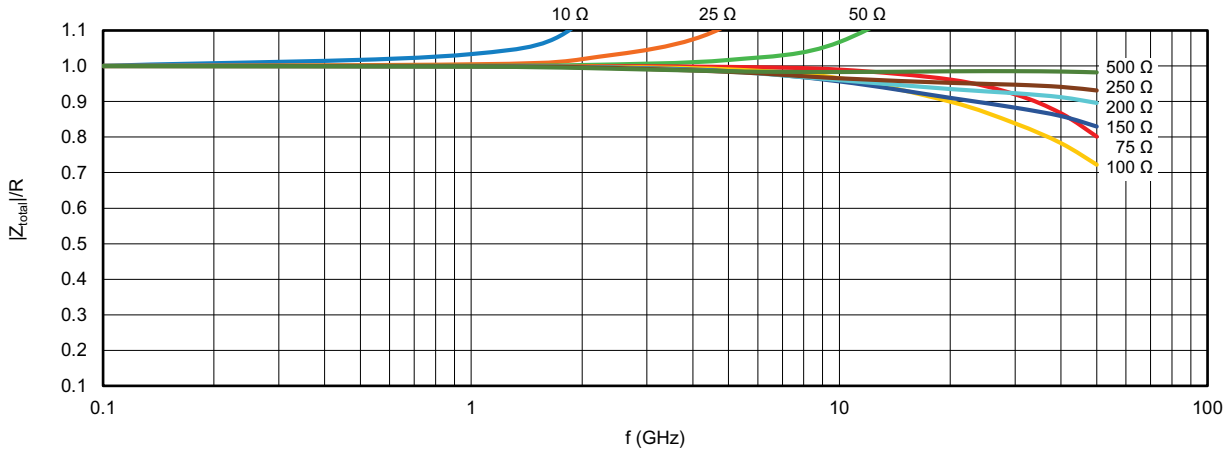
INTERNAL IMPEDANCE CURVES ($|Z_{TOTAL}|$ / R)



Internal impedance curve for 02016 size (F and P terminations)

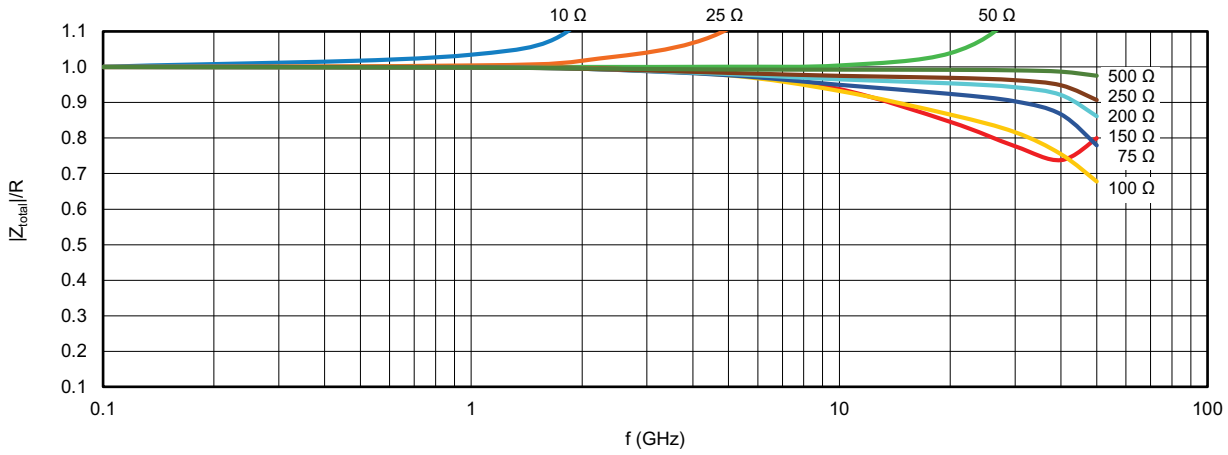


Internal impedance curve for 0402 size (F and P terminations)

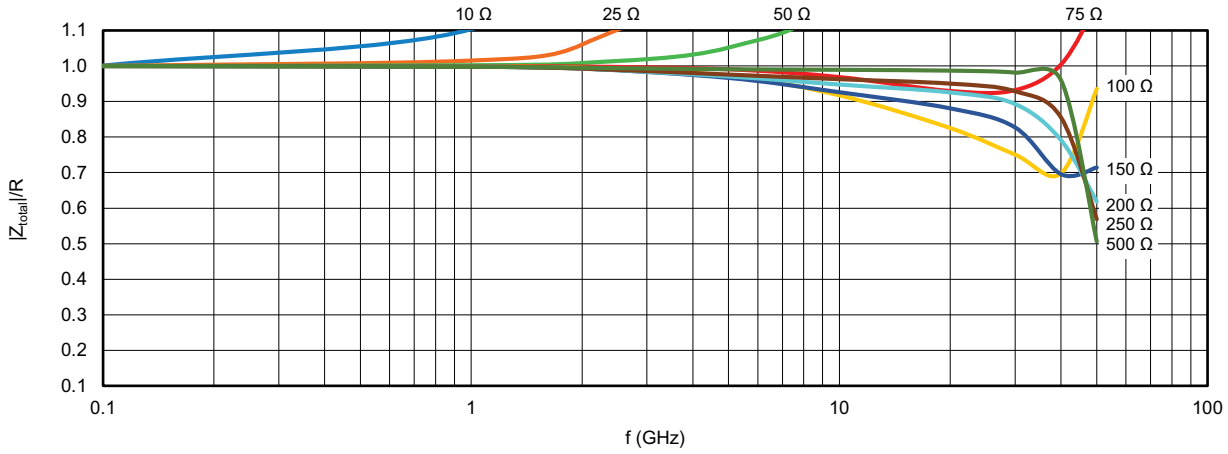


Internal impedance curve for 0402 size (N and G terminations)

INTERNAL IMPEDANCE CURVES ($|Z_{TOTAL}|$ / R)



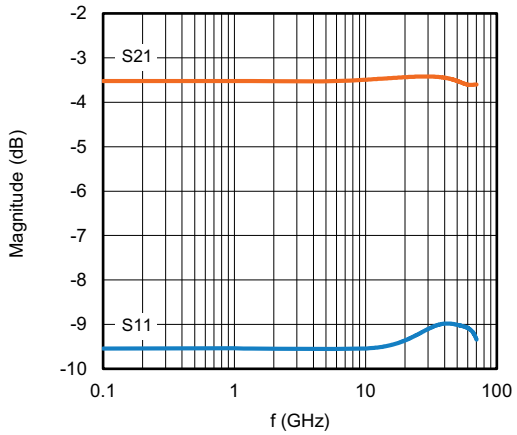
Internal impedance curve for 0603 size (F and P terminations)



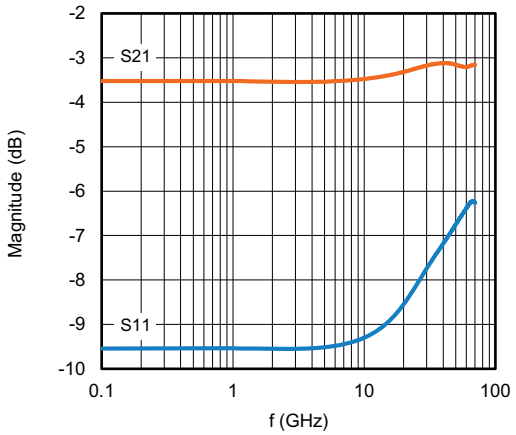
Internal impedance curve for 0603 size (N and G terminations)

S-PARAMETER

CH02016 (F and P Terminations)



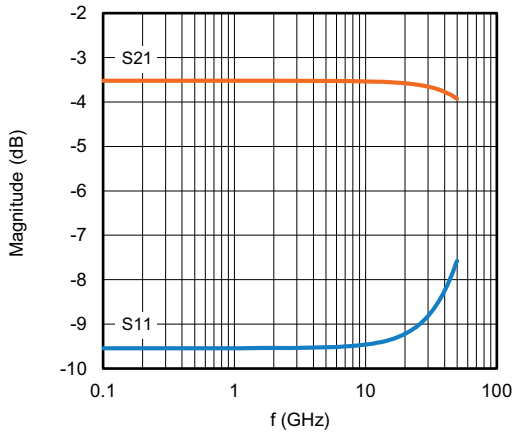
CH02016 flip chip ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)



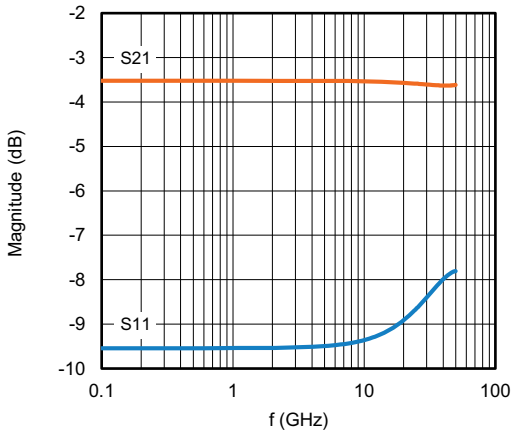
CH02016 flip chip ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

S-PARAMETER

CH0402 (F and P Terminations)

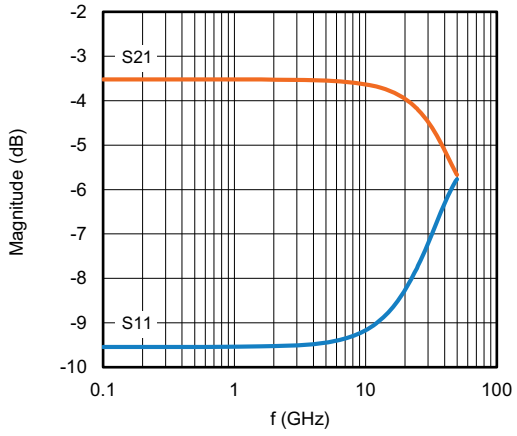


CH0402 flip chip ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)

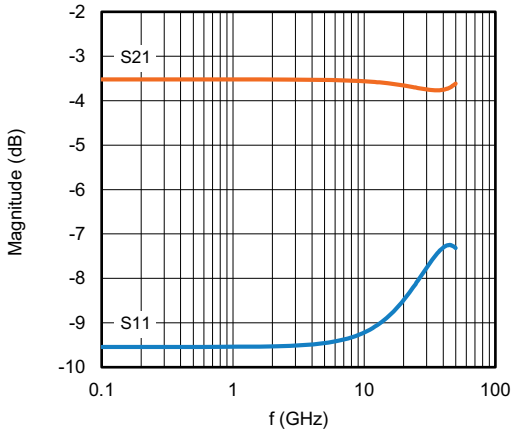


CH0402 flip chip ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

CH0402 (N and G Terminations)

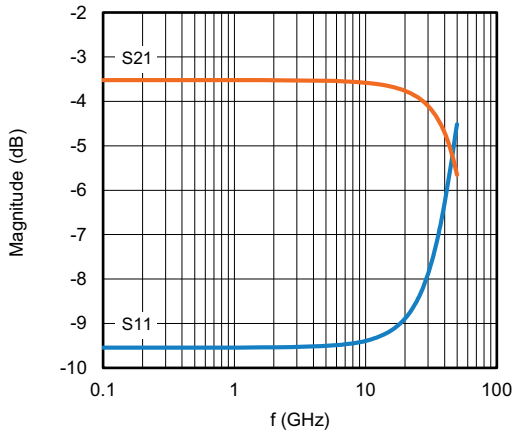


CH0402 wraparound ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)

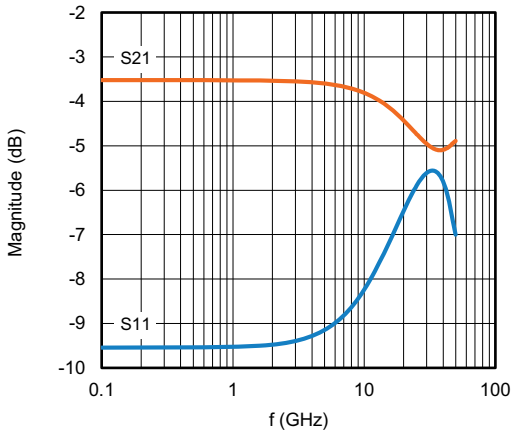


CH0402 wraparound ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

CH0603 (F and P Terminations)



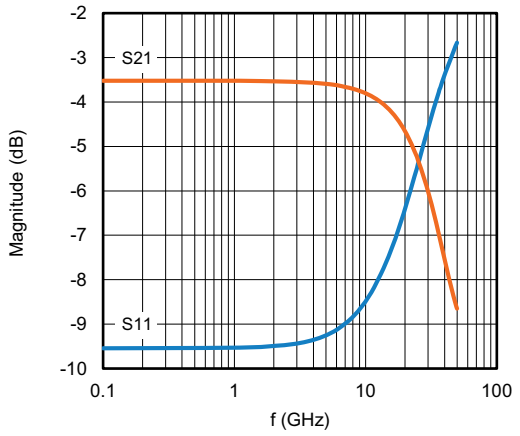
CH0603 flip chip ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)



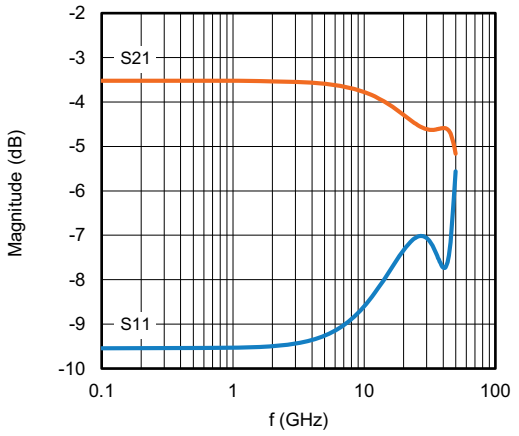
CH0603 flip chip ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

S-PARAMETER

CH0603 (N and G Terminations)



CH0603 wraparound ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)



CH0603 wraparound ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

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