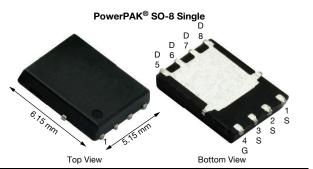
# SiRA14BDP

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**Vishay Siliconix** 



PRODUCT SUMMARY						
V <sub>DS</sub> (V)	30					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_GS$ = 10 V	0.00538					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_GS$ = 4.5 V	0.00702					
Q <sub>g</sub> typ. (nC)	6.6					
I <sub>D</sub> (A) <sup>a</sup>	64					
Configuration	Single					

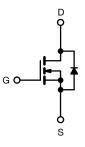
#### **FEATURES**

N-Channel 30 V (D-S) MOSFET

- TrenchFET<sup>®</sup> Gen IV power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

#### **APPLICATIONS**

- High power density DC/DC
- Synchronous rectification
- VRMs and embedded DC/DC



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiRA14BDP-T1-GE3

<b>ABSOLUTE MAXIMUM RATINGS</b> (T	<sub>A</sub> = 25 °C, unless	s otherwise no	ted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	30	v	
Gate-source voltage		V <sub>GS</sub>	+20, -16	v	
	T <sub>C</sub> = 25 °C		64		
Continuous drain current ( $T_{1}$ = 150 °C)	T <sub>C</sub> = 70 °C		52		
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	21 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		16 <sup>b, c</sup>	•	
Pulsed drain current (t = 100 µs)		I <sub>DM</sub>	130	A	
Ocationa como ducio dicale coment	T <sub>C</sub> = 25 °C		33		
Continuous source-drain diode current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	3.3 <sup>b, c</sup>		
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	15		
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	11.3	mJ	
	T <sub>C</sub> = 25 °C		36		
Maximum power dissipation	T <sub>C</sub> = 70 °C		23	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.7 <sup>b, c</sup>	vv	
	T <sub>A</sub> = 70 °C	-	2.4 <sup>b, c</sup>	]	
Operating junction and storage temperature range	e	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature)	d, e		260	C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SMYBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	28	34	°C/W
Maximum junction-to-case (drain)	Steady state	R <sub>thJC</sub>	2.7	3.5	0/11

Notes a. Based on  $T_C$  = 25  $^\circ C$ 

b. Surface mounted on 1" x 1" FR4 board

t = 10 s c.

See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection d.

Rework conditions: manual soldering with a soldering iron is not recommended for leadless components Maximum under steady state conditions is 72 °C/W e.

f.

S18-0993-Rev. A, 01-Oct-2018

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SiRA14BDP

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**Vishay Siliconix** 

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	1 1						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30	-	-		
Drain-source breakdown voltage <sup>(c)</sup> (transient)	V <sub>DSt</sub>	$\label{eq:VGS} \begin{array}{l} V_{GS} = 0 \ V, \ I_{D(aval)} = 40 \ A, \\ t_{transcient} \leq 50 \ ns \end{array}$	36	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	15.2	-	m)//%	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-4.7	-	mv/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	1.1	-	2.2	V	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20, -16 V	-	-	± 100	nA	
	l . I	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1		
Zero gate voltage drain current	IDSS	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	μA	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	30	-	-	А	
	_	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	0.00370	0.00538	-	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 8 \text{ A}$	-	0.00540	0.00702	Ω	
Forward transconductance <sup>a</sup>	<b>g</b> <sub>fs</sub>	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	-	65	-	S	
Dynamic <sup>b</sup>	010		<u> </u>	<u> </u>			
Input capacitance	C <sub>iss</sub>		-	917	-		
Output capacitance	C <sub>oss</sub>		-	389	-	V mV/°C V nA μA A	nF
Reverse transfer capacitance	C <sub>rss</sub>	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz$	-	37	-		
C <sub>rss</sub> /C <sub>iss</sub> ratio	- 135		-	0.04	0.08		
		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	14	22		
Total gate charge	Qg		-	6.6	10	1	
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$	-	2.93	-	nC	
Gate-drain charge	Q <sub>gd</sub>		-	1.61	-		
Output charge	Q <sub>oss</sub>	$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	11	-		
Gate resistance	Rg	f = 1 MHz	0.6	2.8	5.6	Ω	
Turn-on delay time	t <sub>d(on)</sub>		_	10	20		
Rise time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, \text{ R}_{\text{L}} = 1.5 \Omega$	_	5	10		
Turn-off delay time	t <sub>d(off)</sub>	$V_{DD} = 15 V$ , $R_L = 1.5 \Omega$ $I_D \cong 10 A$ , $V_{GEN} = 10 V$ , $R_g = 1 \Omega$	-	16	30		
Fall time	t <sub>f</sub>		-	5	10	ns	
Turn-on delay time	t <sub>d(on)</sub>		-	15	30		
Rise time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, \text{ R}_{\text{L}} = 1.5 \Omega$	-	30	60		
Turn-off delay time	t <sub>d(off)</sub>	$V_{DD} = 15 \text{ V}, \text{ R}_{L} = 1.5 \Omega$ $I_{D} \cong 10 \text{ A}, \text{ V}_{\text{GEN}} = 4.5 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$	-	17	35	-	
Fall time	t <sub>f</sub>		-	10	20		
Drain-Source Body Diode Characteristic	1		I		20		
Continuous source-drain diode current	Is I	T <sub>C</sub> = 25 °C	[ -	I -	33		
Pulse diode forward current <sup>a</sup>	I <sub>SM</sub>	10-20 0	-	-	130	Α	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A	-	0.77	1.1	V	
Body diode reverse recovery time		15 - 10 A	-	20	40		
,	t <sub>rr</sub>		-	20	40 20		
Body diode reverse recovery charge	Q <sub>rr</sub>	l <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C			20	no	
Reverse recovery fall time Reverse recovery rise time	t <sub>a</sub> t <sub>b</sub>	13-20 0	-	10 10	-	ns	

#### Notes

a. Pulse test: pulse width  $\leq 300~\mu\text{s},\,duty~cycle \leq 2~\%$ 

b. Guaranteed by design, not subject to production testing

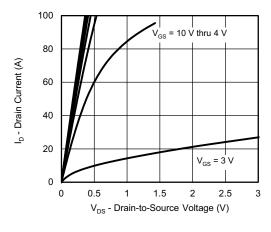
c. Based on characterization, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

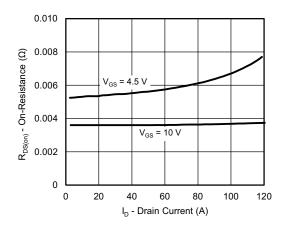
2



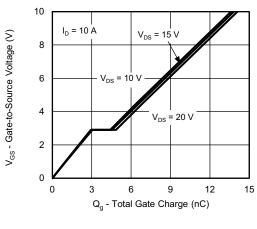
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



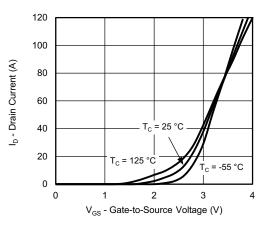
**Output Characteristics** 



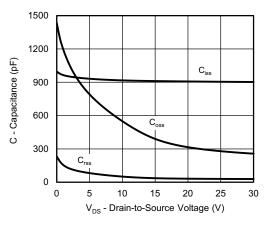
**On-Resistance vs. Drain Current** 



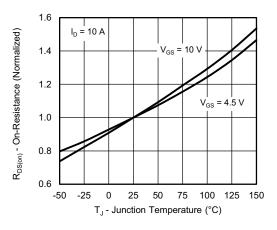
Gate Charge



**Transfer Characteristics** 



Capacitance



**On-Resistance vs. Junction Temperature** 

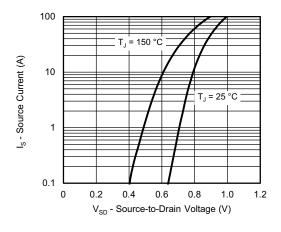
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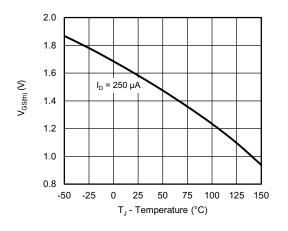
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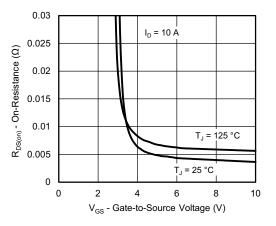
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



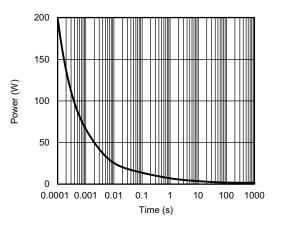
Source-Drain Diode Forward Voltage



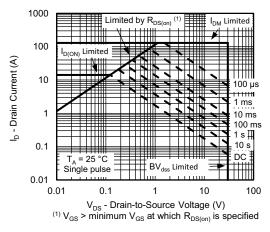
**Threshold Voltage** 



**On-Resistance vs. Gate-to-Source Voltage** 



Single Pulse Power, Junction-to-Ambient

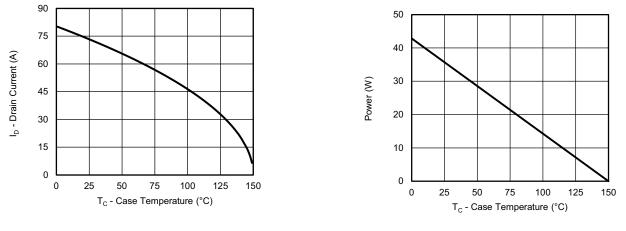


Safe Operating Area

4



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



#### Current Derating <sup>a</sup>

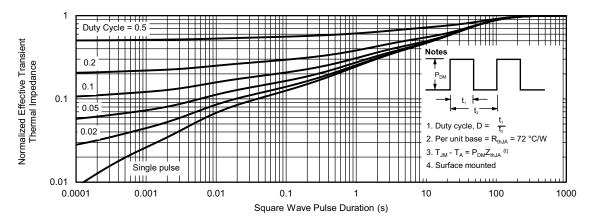
Power, Junction-to-Case

#### Note

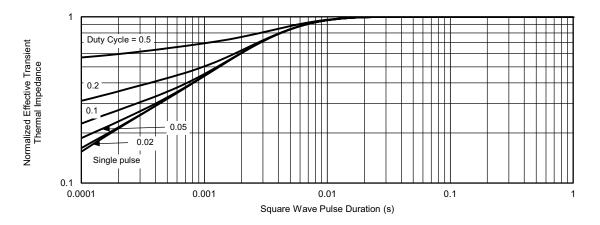
a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?76789">www.vishay.com/ppg?76789</a>.

D2

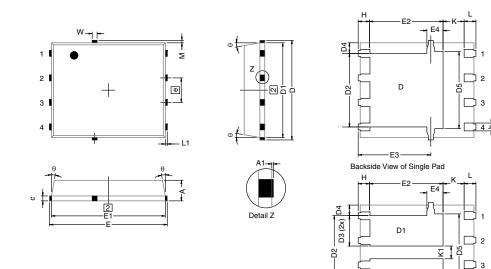
E3

Backside View of Dual Pad



**Vishay Siliconix** 

# PowerPAK<sup>®</sup> SO-8, (Single/Dual)



#### Notes

1. Inch will govern.

2 Dimensions exclusive of mold gate burrs.

3. Dimensions exclusive of mold flash and cutting burrs.

		MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX		
А	0.97	1.04	1.12	0.038	0.041	0.044		
A1		-	0.05	0	-	0.002		
b	0.33	0.41	0.51	0.013	0.016	0.020		
С	0.23	0.28	0.33	0.009	0.011	0.013		
D	5.05	5.15	5.26	0.199	0.203	0.207		
D1	4.80	4.90	5.00	0.189	0.193	0.19		
D2	3.56	3.76	3.91	0.140	0.148	0.154		
D3	1.32	1.50	1.68	0.052	0.059	0.066		
D4		0.57 typ. 0.0225 typ.						
D5		3.98 typ.		0.157 typ.				
E	6.05	6.15	6.25	0.238	0.242	0.246		
E1	5.79	5.89	5.99	0.228	0.232	0.236		
E2	3.48	3.66	3.84	0.137	0.144	0.15		
E3	3.68	3.78	3.91	0.145	0.149	0.154		
E4		0.75 typ.			0.030 typ.			
е		1.27 BSC		0.050 BSC				
К		1.27 typ.		0.050 typ.				
K1	0.56	-	-	0.022	-	-		
Н	0.51	0.61	0.71	0.020	0.024	0.028		
L	0.51	0.61	0.71	0.020	0.024	0.028		
L1	0.06	0.13	0.20	0.002	0.005	0.008		
θ	0°	-	12°	0°	-	12°		
W	0.15	0.25	0.36	0.006	0.010	0.014		
М		0.125 typ.			0.005 typ.			

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# Application Note 826

Vishay Siliconix

# RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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