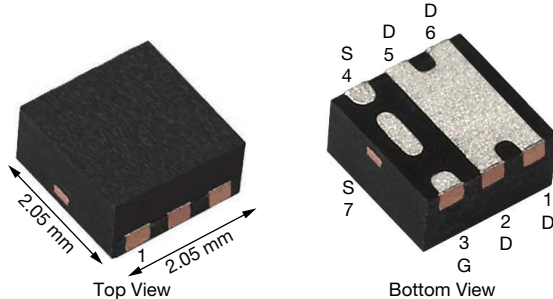


## Automotive P-Channel 30 V (D-S) 175 °C MOSFET

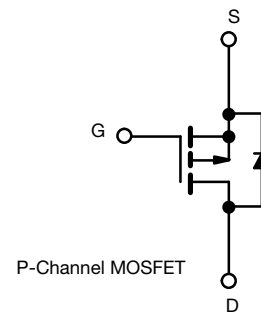
**PowerPAK® SC-70-6L Single**

**Marking Code:** QFXXXX

PRODUCT SUMMARY	
$V_{DS}$ (V)	-30
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -10$ V	0.020
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.033
$I_D$ (A)	-10
Configuration	Single
Package	PowerPAK SC-70

**FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified <sup>d</sup>
- 100 %  $R_g$  and UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

 AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	-30	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current	$I_D$	$T_C = 25$ °C	-10	
		$T_C = 125$ °C	-10	
Continuous source current (diode conduction) <sup>a</sup>	$I_S$	10	A	
Pulsed drain current <sup>b</sup>	$I_{DM}$	-40		
Single pulse avalanche current	$I_{AS}$	15		
Single pulse avalanche energy	$E_{AS}$	L = 0.1 mH	11.25	mJ
Maximum power dissipation <sup>b</sup>			$P_D$	
Operating junction and storage temperature range	$T_J, T_{stg}$	$T_C = 25$ °C	4.5	W
		$T_C = 125$ °C	4.5	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	90	°C/W
Junction-to-case (drain)			

**Notes**

- Package limited
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)
- Parametric verification ongoing



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = -250 μA	-30	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.5	-2	-2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -30 V	-	-	-1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -30 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -30 V, T <sub>J</sub> = 175 °C	-	-	-150	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V, V <sub>DS</sub> ≥ 5 V	-8	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A	-	0.016	0.020	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A, T <sub>J</sub> = 125 °C	-	-	0.029	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A, T <sub>J</sub> = 175 °C	-	-	0.035	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4 A	-	0.026	0.033	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -7 A	-	17	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>iSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -10 V, f = 1 MHz	-	1505	1880	pF
Output capacitance	C <sub>oSS</sub>		-	205	260	
Reverse transfer capacitance	C <sub>rSS</sub>		-	181	227	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = -10 V, V <sub>DS</sub> = -15 V, I <sub>D</sub> = -8 A	-	26	33	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>		-	4.2	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	4.7	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	4.5	7.6	11.2	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 6 Ω I <sub>D</sub> ≅ -2.5 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	-	20	30	ns
Rise time <sup>c</sup>	t <sub>r</sub>		-	18	27	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>		-	19	28	
Fall time <sup>c</sup>	t <sub>f</sub>		-	8	12	
<b>Source-Drain Diode Ratings and Characteristics</b>						
Pulsed current <sup>a</sup>	I <sub>SM</sub>		-	-	-40	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = -5 A, V <sub>GS</sub> = 0	-	-0.8	-1.2	V

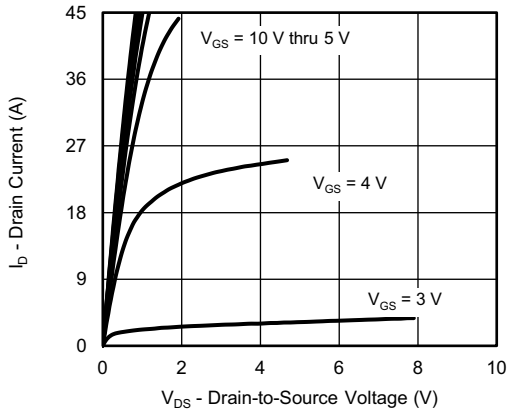
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

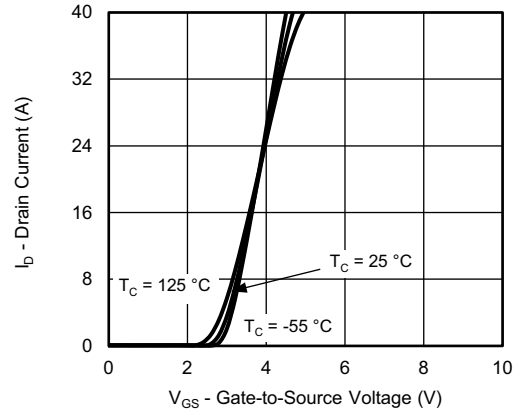
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



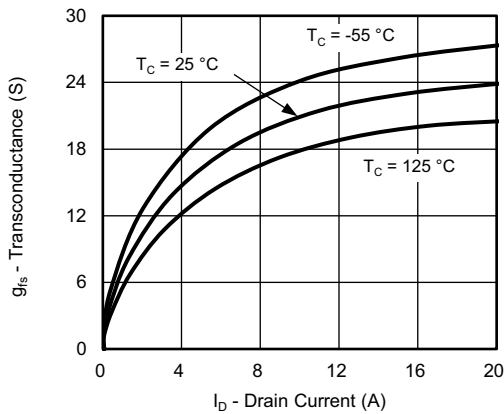
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



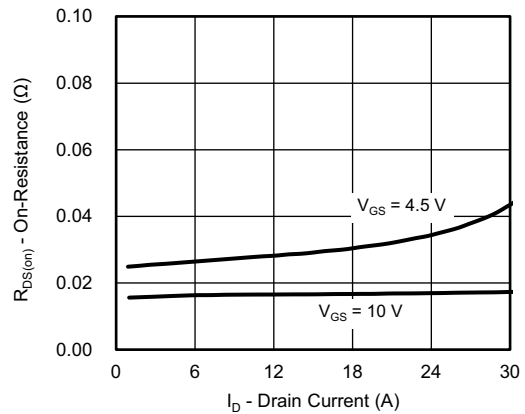
**Output Characteristics**



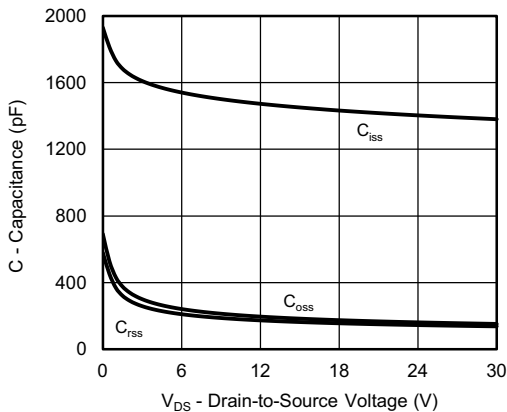
**Transfer Characteristics**



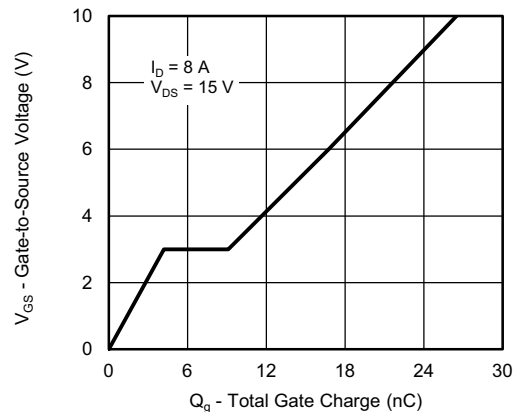
**Transconductance**



**On-Resistance vs. Drain Current**

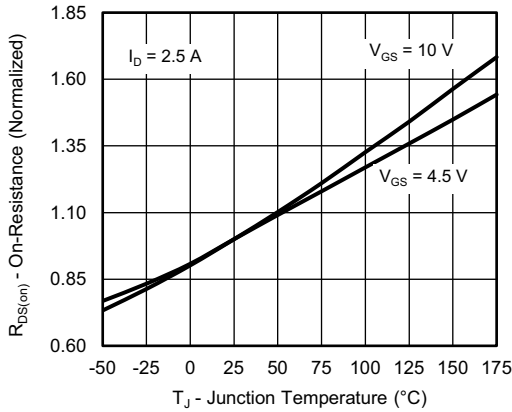


**Capacitance**

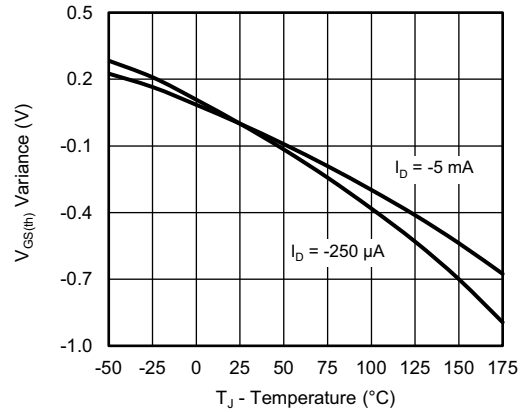


**Gate Charge**

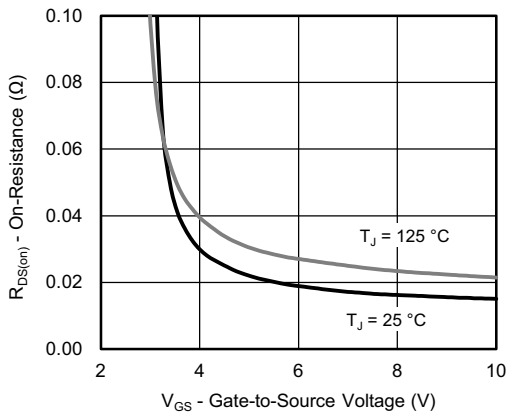
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



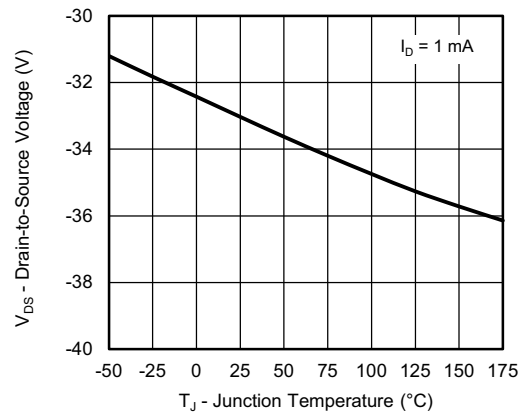
**On-Resistance vs. Junction Temperature**



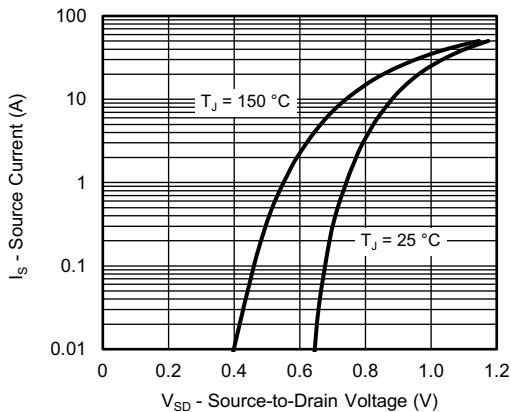
**Threshold Voltage**



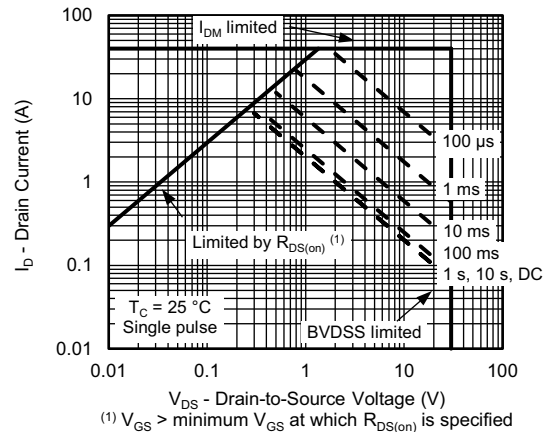
**On-Resistance vs. Gate-to-Source Voltage**



**Drain Source Breakdown vs. Junction Temperature**

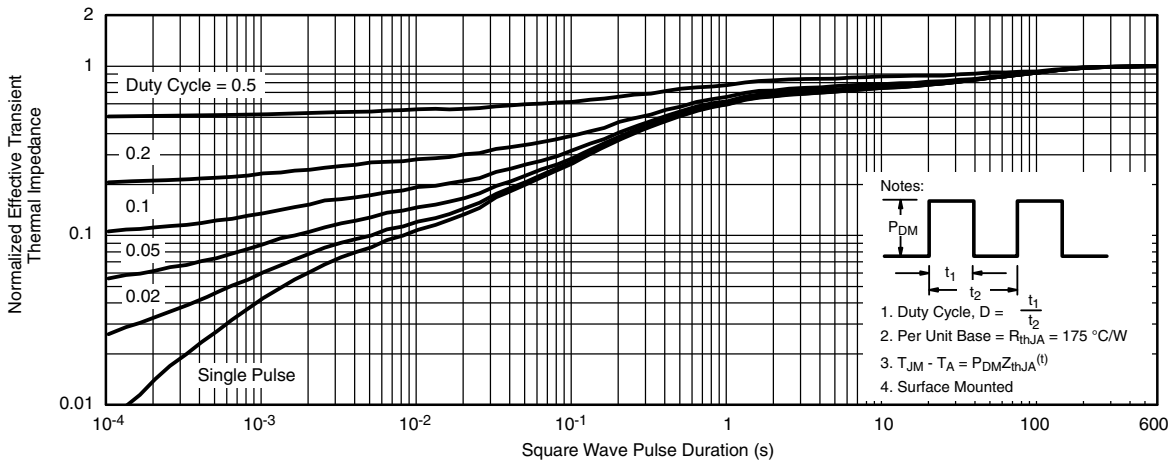


**Source-Drain Diode Forward Voltage**

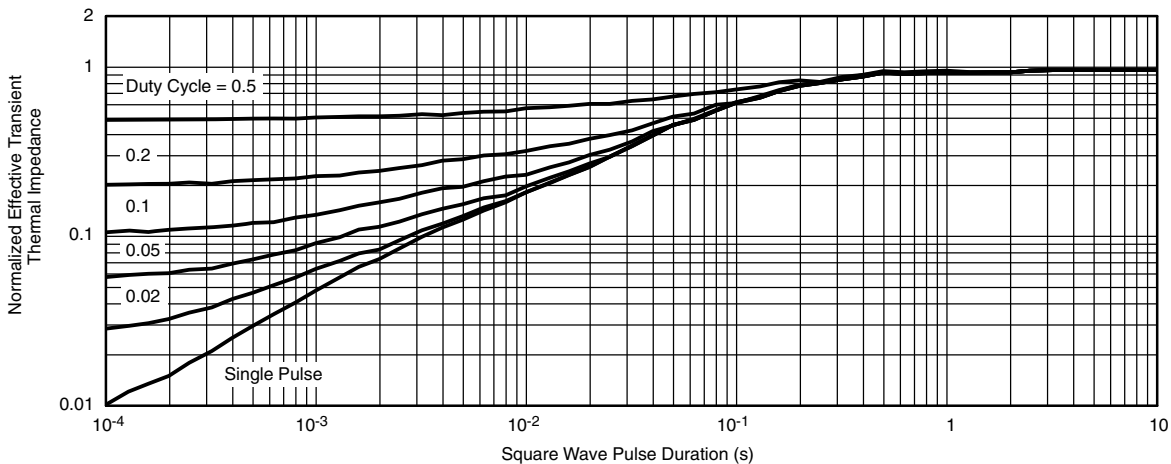


**Safe Operating Area**

**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



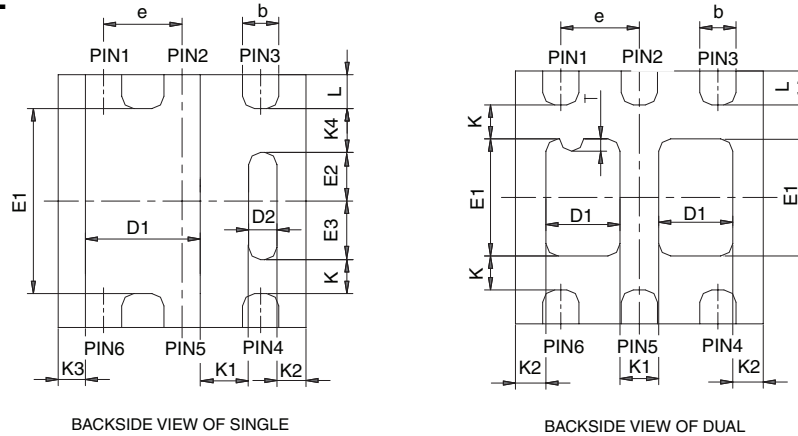
**Normalized Thermal Transient Impedance, Junction-to-Foot**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^\circ\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Foot ( $25\text{ }^\circ\text{C}$ )
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

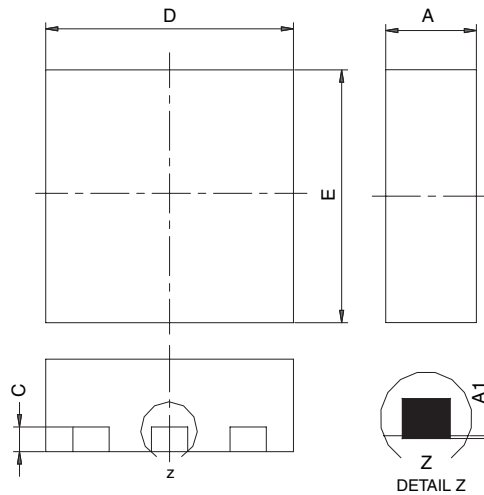
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## PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- Notes:
1. All dimensions are in millimeters
  2. Package outline exclusive of mold flash and metal burr
  3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07  
DWG: 5934

## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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