

Vishay Siliconix

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	V_{DS} (V) $R_{DS(on)}$ (Ω) MAX.		Q _g (TYP.)		
60	0.0024 at V _{GS} = 10 V	120	128 nC		
	0.0027 at V _{GS} = 7.5 V	120			



Ordering Information:

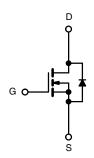
SUP50020E-GE3 (lead (Pb)-free and halogen-free)

FEATURES

- TrenchFET® power MOSFET
- Maximum 175 °C junction temperature
- Q_{gd}/Q_{gs} ratio < 0.25
- Operable with logic-level gate drive
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Power supply
 - Secondary synchronous rectification
- DC/DC converter
- Power tools
- · Motor drive switch
- DC/AC inverter
- · Battery management



COMPLIANT

HALOGEN

FREE

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V _{DS}	60	V		
Gate-Source Voltage	V _{GS}	± 20	V		
Outline - Build Outline - 150 (0)	T _C = 25 °C		120 ^d		
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	- I _D	120 ^d		
Pulsed Drain Current (t = 100 μs)	I _{DM}	300	Α		
Avalanche Current	L = 0.1 mH	I _{AS}	75		
Single Avalanche Energy ^a	L = 0.1 IIII	E _{AS}	281	mJ	
Marina Baras Biorinalia a	T _C = 25 °C	В	375 b	· w	
Maximum Power Dissipation ^a	T _C = 125 °C	P _D	125 ^b		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W	
Junction-to-Case (Drain)	R _{thJC}	0.4	C/VV	

Notes

- a. Duty cycle ≤ 1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR4 material).
- d. Package limited.



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		-	-	V	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2	-	4	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 250	nA	
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μΑ	
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125 °C	-	-	150		
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 175 °C	-	-	5	mA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	120	-	-	Α	
Drain-Source On-State Resistance a	В	V _{GS} = 10 V, I _D = 30 A	-	0.0020	0.0024	Ω	
Drain-Source On-State Resistance 4	R _{DS(on)}	V _{GS} = 7.5 V, I _D = 20 A	-	0.0022	0.0027		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A	-	145	-	S	
Dynamic ^b			•	•			
Input Capacitance	C _{iss}		-	11 150	-	pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 30 \text{ V}, f = 1 \text{ MHz}$	-	4255	-		
Reverse Transfer Capacitance	C _{rss}		-	420	-		
Total Gate Charge ^c	Q_g		-	128	-	nC	
Gate-Source Charge ^c	Q_{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	44	-		
Gate-Drain Charge ^c	Q_{gd}		-	9	-		
Gate Resistance	R_g	f = 1 MHz	0.32	1.6	3.2	Ω	
Turn-On Delay Time ^c	t _{d(on)}		-	18	36		
Rise Time ^c	t _r	$V_{DD} = 30 \text{ V}, R_L = 5 \Omega$	-	20	40		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D\cong 10~A,~V_{GEN}=10~V,~R_g=1~\Omega$	-	55	100	ns	
Fall Time ^c	t _f		-	23	35		
Drain-Source Body Diode Ratings at	nd Characteris	stics ^b (T _C = 25 °C)		•			
Pulsed Current (t = 100 μs)	I _{SM}		-	-	300	Α	
Forward Voltage ^a	V_{SD}	$I_F = 10 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.8	1.5	V	
Reverse Recovery Time	t _{rr}		-	120	180	ns	
Peak Reverse Recovery Charge	I _{RM(REC)}	$I_F = 39 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	5.5	11	Α	
Reverse Recovery Charge	Q _{rr}		-	0.320	0.480	μC	

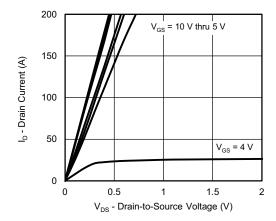
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

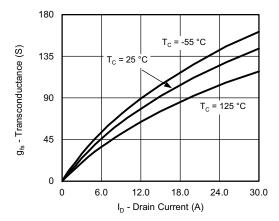
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



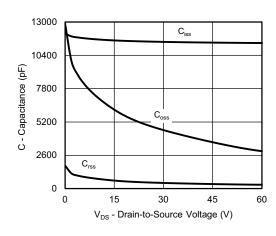
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Output Characteristics

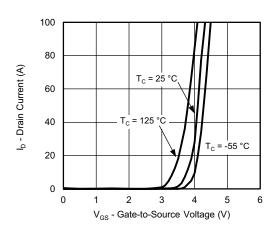


Transconductance

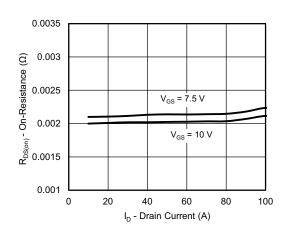


Capacitance

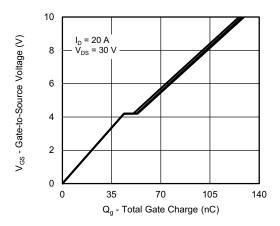
S16-2567-Rev. A, 19-Dec-16



Transfer Characteristics



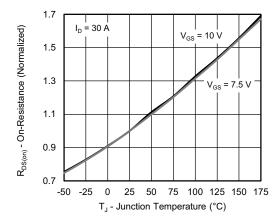
On-Resistance vs. Drain Current



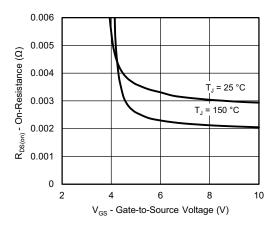
Gate Charge



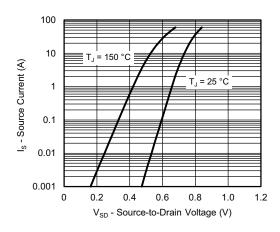
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



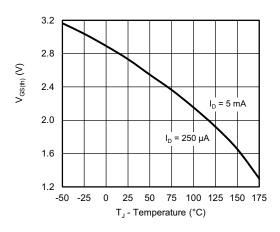
On-Resistance vs. Junction Temperature



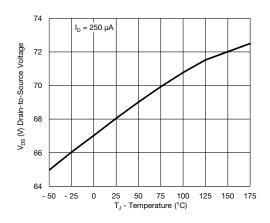
On-Resistance vs. Gate-to-Source Voltage



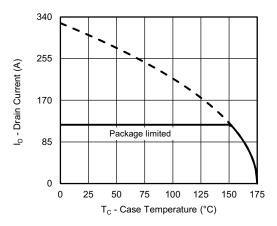
Source Drain Diode Forward Voltage



Threshold Voltage



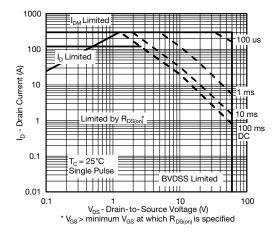
Drain Source Breakdown vs. Junction Temperature

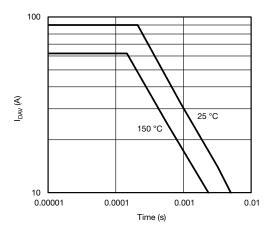


Current De-rating



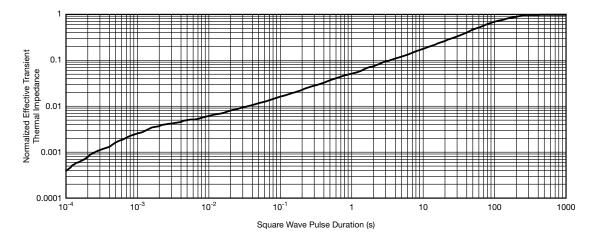
THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)





Safe Operating Area

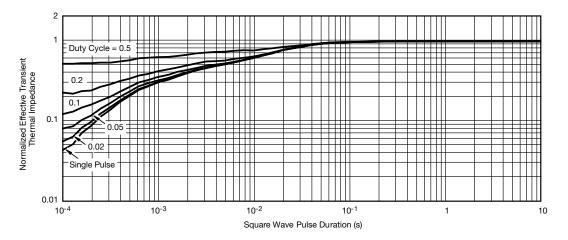
Single Pulse Avalanche Current Capability vs. Time



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient (25 °C)

can widely vary depending on actual application parameters and operating conditions.

- Normalized Transient Thermal Impedance Junction to Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities

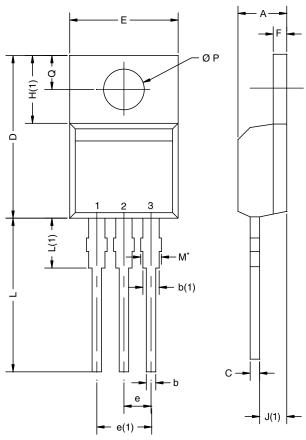
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74901.

S16-2567-Rev. A, 19-Dec-16 6 Document Number: 74901





TO-220AB



- 6	e(1) -	
		D2

	MILLIM	IETERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
D2	12.19	12.70	0.480	0.500	
E	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØΡ	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: T14-0413-Rev. P, 16-Jun-14 DWG: 5471					

Note

 $^{^{\}star}$ M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



Vishay

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