APPROVAL SHEET

RF Switch Series – RoSH Compliance

SP12T MIPI Switch

Halogens Free Product

Any 2G/3G/4G Band for TRx system

P/N: RMASMF496ATF03

*Contents in this sheet are subject to change without prior notice.

FEATURES

- Low Insertion Loss and Low Distortion
- Broadband frequency range：0.4 to 2.7 GHz
- High Isolation and linearity
- Integrated MIPI RFFE Slave Controller
- High ESD tolerance of 2kV HBM at all pins
- Small LGA(20-pin, 2.5 x 2.5 x 0.78 mm^3) package
- **M**oisture **S**ensitive **L**evel 3 (MSL3)

Description

- The RMASMF496ATF03 is a Single Pole, Twelve Throw (SP12T) antenna switch with an integrated Mobile Industry Processor Interface (MIPI) controller. Using an advanced switching technology, the RMASMF496ATF03 maintains low insertion and high isolation, which makes it an ideal choice for UMTS, CDMA2000, EDGE, GSM, and LTE applications.
- The design integrated two GSM transmit ports and ten low loss TRX ports. The switch also has an excellent $2^{nd}/3^{rd}$ Order Intermodulation Distortion (IMD2/IMD3) performance.
- Switching is controlled by the MIPI decoder and High ESD tolerance of 2kV HBM at all pins.
- No blocking capacitor requirements on the RF paths as long as no DC voltage are applied. The RMASMF496ATF03 is manufactured in a compact, 2.5 x 2.5 x 0.78 mm^3 package.
- The functional block diagram is shown in Figure 1. The pin assignment and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Application

- 2G/3G/4G multimode cellular handsets (LTE, UMTS, CDMA2000, EDGE, GSM, TDD-LTE, TD-SCDMA)

Block Diagram and Pin Out (Top View)

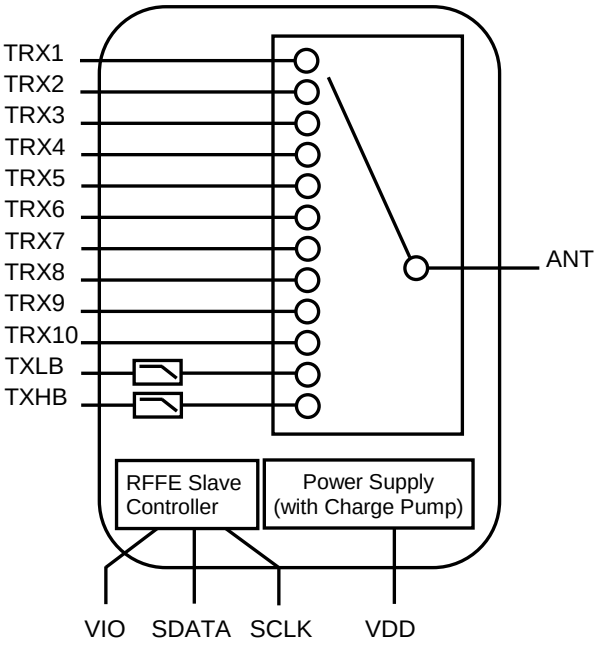


Figure 1. RMASMF496ATF03 Block Diagram

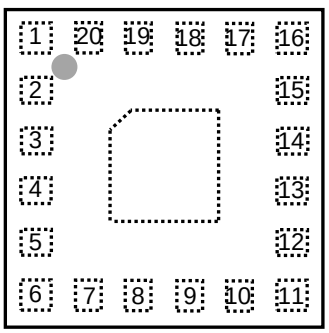


Figure 2. RMASMF496ATF03 Pin assignment

Table 1. RMASMF496ATF03 Pin Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	ANT	Antenna port	11	TRX3	RF path 3
2	TRX7	RF path 7	12	TRX2	RF path 2
3	TRX6	RF path 6	13	TRX1	RF path 1
4	TRX5	RF path 5	14	TRX10	RF path 10
5	TRX4	RF path 4	15	TRX9	RF path 9
6	GND	Ground	16	TRX8	RF path 8
7	VDD	DC power supply	17	GND	Ground
8	VIO	RFFE Interface Power Supply	18	TXHB	GSM transmit high band
9	SDATA	RFFE Data input/output	19	TXLB	GSM transmit low band
10	SCLK	RFFE Clock Input	20	GND	Ground

Note 1：Bottom ground paddles must be connected to ground.

Application Circuit

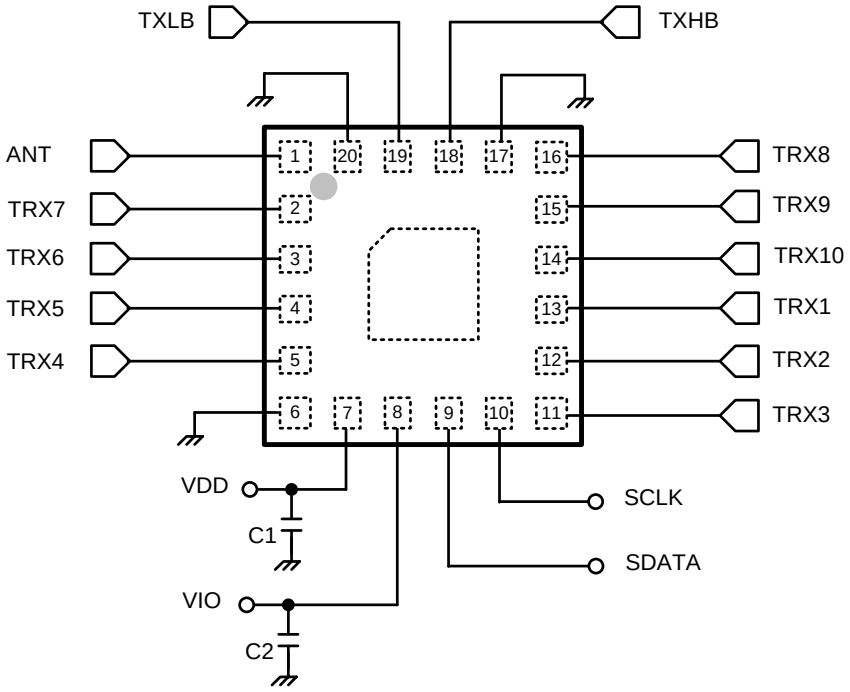


Figure 3. RMASMF496ATF03 Application Circuit

Note: No DC Blocking capacitors are required for all RF ports unless DC is biased externally.

Parts List

Parts No.	Value
C1-C2	0.1 μF

Table 2. RMASMF496ATF03 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	VDD	-0.3	5.5	V
Interface Supply Voltage	VIO	-0.3	2.0	V
Control Input/ Output Voltage Range (SDATA, SCLK)	V_{IN_OUT}	-0.3	2.0	V
Maximum Control Output Current (SDATA)	I_{OUT}	-5	+5	mA
TXLB Input Power (f = 824 ~ 915 MHz, 50Ω, Duty = 50%)	PIN		+38	dBm
TXHB Input Power (f = 1710 ~ 1910 MHz, 50Ω, Duty = 50%)			+36	dBm
TRXx Input Power (f = 698 ~ 2690 MHz, 50Ω, CW)			+30	dBm
Storage temperature	T_{STG}	-55	+125	°C
Operating temperature	T_{OP}	-30	+90	°C
HBM ESD Voltage, All Pins	V_{ESD}[1]		2000	V
MM ESD Voltage, All Pins	V_{ESD}[2]		190	V

Note 1 : Human Body Model ESD Voltage (HBM, MIL_STD 883 Method 3015.7)
Note 2 : Machine Model ESD Voltage (MM, JEITA EIAJ ED-4701)

Exceeding absolute maximum ratings may cause permanent damage. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrical and Mechanical Specifications

- The absolute maximum ratings of the RMASMF496ATF03 are provided in Table 2. Electrical specifications are provided in Tables 3 and 5. The Table 8 and 9 are provides the measurement result.
- Figure 4, 5 and Table4 describes the RMASMF496ATF03 has four operating states.
- IMD2 and IMD3 test conditions for various frequencies are listed in Tables 6 and 7, respectively.
- Figure 6, 7, 8, 9 and Table10 show the important parameters for SCLK and SDATA required for proper operations of the Toshiba MIPI RFFE slave interface.
- Table 11 describes the MIPI transaction details and programming read/write sequences. Refer to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.
- Table 12 register mapping shows the list of the registers inside the RMASMF496ATF03.
- Table 13 provides the switch control register.
- Table 14, 15 and 16 describes the detail information of RFFE status, power mode and trigger states, respectively.
- Figure 10 and Table 17 describes the solder land pad and dimensions.

Table 3. RMASMF496ATF03 DC Electrical Specifications (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	2.3	2.8	4.8	V
Supply current, active mode (VDD=4.8V)	IDD		110	200	μA
Supply current, low power mode (VDD=4.8V)	IDD		20	35	μA
Interface supply voltage	VIO	1.65	1.80	1.95	V
Interface signal: High Low	SDATA	 0.8 × VIO 0		 VIO 0.2 × VIO	 V V
Control current: High Low		 -3 -3	 1 1	 10 3	 μA μA

Note 1 : Performance is guaranteed only under the conditions listed in this Table.

Operating States

The RMASMF496ATF03 has four operating states, which are ACTIVE, SHUTDOWN, STATUP and LOW POWER. The transitions between these four states are set writing the PWR_MODE register or VIO as shown in Figure 4. The internal circuit operations in each operating state are shown in Table 4.

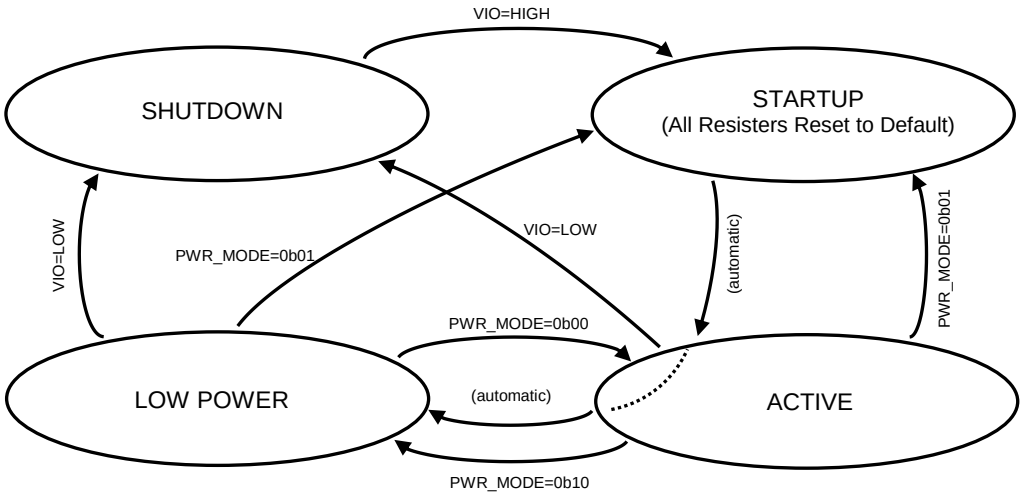


Figure 4. Slave State Diagram

Table 4. RMASMF496ATF03 Internal Operations (Note 1)

Operating State	RFFE Slave Controller	RF Switch Core	Charge Pump
SHUTSOWN	Inactive	Undetermined (Note1)	Off
STARTUP	All registers are set to Default value	Undetermined (Note1)	Off
ACTIVE	Active	Controllable by mipi-command	On
LOW POWER	Active	Undetermined (Note1)	Off

Note 1 : All switch are insufficiently On or Off as the Charge pump is not powered up.

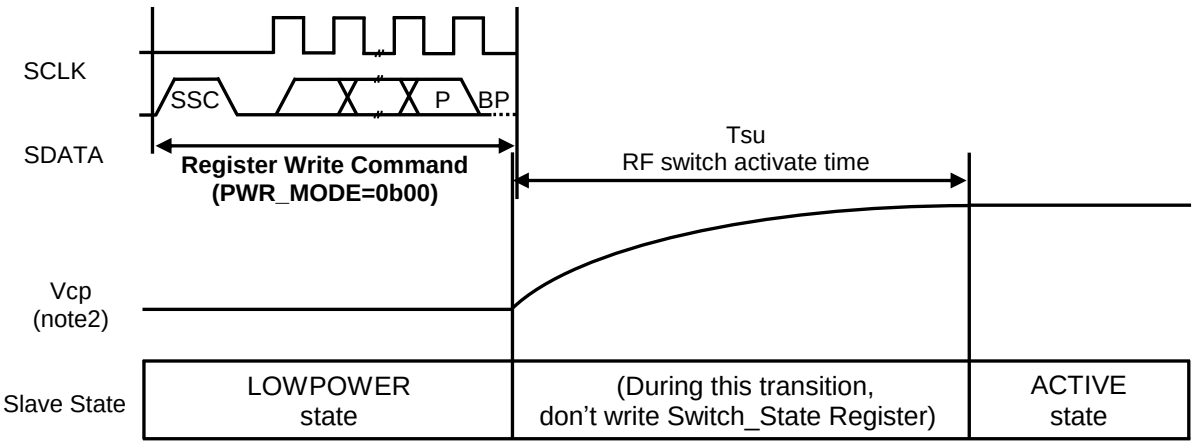


Figure 5. LOW POWER to AVTIVE Process

Note 2 : Vcp is the output voltage of internal charge-pump circuit. The Vcp traces in above figure are only image for illustrative purpose.

Table 5. RMASMF496ATF03 RF Electrical Specifications (Note 1)

(T_{op}= 25°C, VDD = 2.8 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
Operating frequency	f		0.4		2.7	GHz
Insertion loss	IL	TXLB, 824 to 915 MHz TXHB, 1710 to 1910 MHz TRXx ports: 824 to 915 MHz 1710 to 2170 MHz 1880 to 2690 MHz		1.25 1.25 0.60 0.80 0.85	1.45 1.45 0.70 0.90 1.00	dB dB dB dB dB
GSM Attenuation	2fo, 3fo	TXLB: 1648 to 1930 MHz 2472 to 2745 MHz TXHB: 3420 to 3820 MHz 5130 to 5730 MHz	 25 25 25 25	 30 30 30 30		 dB dB dB dB
Isolation (TRXx to any off TRXx port [non-adjacent ports])	Iso	Up to 1.0 GHz Up to 2.0 GHz Up to 2.7 GHz	30 25 23			dB dB dB
Isolation (TRXx to any off TRXx port [adjacent ports])	Iso	Up to 1.0 GHz Up to 2.0 GHz Up to 2.7 GHz	26 23 20			dB dB dB
On state match	VSWR	Up to 2.7 GHz		1.43	2.0	-
GSM harmonics: High band Low band	2fo, 3fo	 PIN = +33 dBm, 50 Ω, CW PIN = +33 dBm, 50 Ω, CW		 -100 -100	 -90 -90	 dBc dBc
TRXx harmonics	2fo, 3fo	PIN = +27 dBm, CW f = 824 to 2700 MHz		-97	-90	dBc
2nd Order Intermodulation Distortion	IMD2	See test conditions in Table 6		-104	-100	dBm
3rd Order Intermodulation Distortion	IMD3	See test conditions in Table 7		-118	-112	dBm
Turn-on time	t_{ON}	From application of VDD and VIO			20	μs
Switching speed	t_S	Port to port			5	μs

Note 1 : Performance is guaranteed only under the conditions listed in this Table.

Table 6. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	–15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 7. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Table 8. Isolation Matrix : ANT to Off Path (1 of 2)

(T_{op}= 25°C, VDD = 2.8 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

On Path	Freq (GHz)	Isolation (dB)											
		TXLB	TXHB	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
TXLB	1.0		-37.6	-45.0	-45.6	-42.2	-40.2	-41.3	-33.1	-26.0	-38.6	-40.7	-42.2
	2.0		-38.5	-38.9	-41.0	-37.2	-38.7	-34.2	-28.1	-23.0	-32.0	-33.8	-35.5
	2.7		-46.7	-39.8	-42.5	-38.7	-41.1	-37.5	-29.4	-27.9	-32.1	-34.3	-36.5
TXHB	1.0	-47.0		-52.8	-43.1	-41.0	-42.8	-39.8	-35.6	-30.1	-39.4	-42.3	-46.3
	2.0	-35.5		-53.0	-39.3	-35.9	-36.4	-33.8	-30.1	-23.7	-30.8	-33.8	-41.4
	2.7	-35.3		-29.0	-39.6	-34.6	-30.1	-29.2	-27.1	-23.3	-30.8	-29.9	-29.4
TRX1	1.0	-43.0	-41.1		-32.2	-37.0	-44.7	-41.5	-36.7	-31.3	-44.9	-39.7	-33.4
	2.0	-45.4	-32.8		-27.0	-31.2	-36.6	-34.8	-31.0	-26.3	-34.9	-32.4	-27.5
	2.7	-40.5	-38.4		-25.6	-30.4	-33.4	-32.2	-29.0	-25.0	-31.4	-29.5	-25.4
TRX2	1.0	-43.2	-40.4	-32.2		-31.1	-45.0	-41.8	-36.8	-31.3	-43.7	-44.4	-39.5
	2.0	-45.3	-41.0	-26.8		-25.5	-36.7	-34.9	-31.1	-26.2	-34.8	-34.6	-32.7
	2.7	-40.0	-46.9	-25.5		-24.9	-33.0	-32.0	-28.8	-25.1	-31.6	-31.3	-30.6
TRX3	1.0	-43.3	-39.1	-37.3	-31.2		-46.3	-42.4	-37.1	-31.5	-43.0	-45.9	-43.6
	2.0	-45.5	-56.7	-30.9	-25.4		-36.8	-35.0	-31.0	-26.1	-34.7	-35.2	-34.5
	2.7	-39.6	-42.6	-29.3	-24.2		-32.0	-31.3	-28.6	-24.9	-31.5	-31.5	-31.3

Table 8. Isolation Matrix : ANT to Off Path (2 of 2)

(T_{op}= 25°C, VDD = 2.8 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

On Path	Freq (GHz)	Isolation (dB)											
		TXLB	TXHB	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
TRX4	1.0	-39.0	-40.7	-49.6	-54.3	-52.3		-33.9	-41.1	-32.4	-41.7	-44.4	-46.0
	2.0	-45.7	-48.7	-41.3	-43.3	-41.8		-27.2	-31.0	-26.1	-35.2	-36.9	-38.5
	2.7	-41.7	-41.6	-37.8	-40.1	-37.8		-24.7	-27.7	-24.4	-32.4	-33.6	-35.1
TRX5	1.0	-36.8	-39.8	-49.5	-51.8	-52.2	-33.1		-36.9	-33.0	-41.7	-44.0	-45.1
	2.0	-46.7	-52.8	-40.6	-43.0	-41.6	-27.2		-28.0	-25.8	-34.9	-36.5	-38.3
	2.7	-42.1	-40.7	-37.4	-39.5	-37.7	-24.6		-24.5	-23.9	-32.2	-33.5	-34.9
TRX6	1.0	-36.9	-41.1	-47.9	-50.7	-50.3	-42.0	-35.4		-33.7	-41.7	-43.6	-45.0
	2.0	-40.1	-49.8	-40.0	-42.1	-41.0	-33.3	-27.9		-24.0	-34.7	-36.1	-37.5
	2.7	-43.4	-41.4	-36.6	-39.0	-37.5	-29.7	-25.2		-21.3	-31.5	-32.9	-34.5
TRX7	1.0	-32.6	-34.1	-48.4	-49.7	-49.7	-45.7	-42.9	-36.0		-42.0	-44.4	-46.0
	2.0	-27.9	-35.1	-39.8	-42.0	-41.0	-35.3	-32.6	-26.7		-34.6	-36.3	-37.9
	2.7	-32.1	-28.0	-37.2	-39.2	-37.9	-31.1	-28.9	-23.4		-31.1	-32.8	-34.7
TRX8	1.0	-43.9	-43.0	-49.0	-52.4	-52.5	-43.6	-41.0	-36.5	-31.1		-39.3	-44.2
	2.0	-49.4	-51.9	-39.2	-42.0	-41.6	-36.9	-35.0	-30.9	-25.9		-31.2	-35.2
	2.7	-41.1	-38.3	-35.6	-38.7	-38.6	-33.3	-32.0	-28.5	-24.4		-27.9	-31.9
TRX9	1.0	-43.6	-41.0	-38.6	-43.3	-46.5	-44.0	-41.1	-36.7	-31.4	-39.8		-31.6
	2.0	-47.5	-40.4	-32.8	-37.1	-38.8	-36.7	-34.9	-30.9	-26.1	-31.1		-26.0
	2.7	-40.8	-42.4	-31.1	-35.4	-37.0	-33.7	-32.3	-28.8	-24.7	-27.8		-24.2
TRX10	1.0	-43.6	-40.6	-33.0	-38.7	-42.3	-44.4	-41.9	-36.8	-31.5	-43.8	-32.0	
	2.0	-46.1	-34.6	-27.4	-33.3	-35.8	-36.9	-34.8	-31.0	-26.2	-34.0	-26.2	
	2.7	-40.7	-43.1	-25.7	-31.9	-34.7	-33.5	-32.3	-29.0	-24.8	-30.4	-24.0	

Table 9. Insertion Loss and Return Loss Matrix

(T_{op}= 25°C, VDD = 2.8 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

On_Path	Freq (MHz)	IL (dB)	RL_Pole (dB)	RL_Throw (dB)
TXLB	915	-0.92	-26.36	-42.06
	1910	-30.95	-2.01	-1.22
	2690	-36.85	-1.84	-1.28
TXHB	915	-0.60	-27.16	-23.33
	1910	-1.00	-18.40	-17.59
	2690	-5.31	-7.00	-6.03
TRX1	915	-0.37	-29.18	-30.98
	1910	-0.48	-22.09	-20.16
	2690	-0.66	-14.86	-16.72
TRX2	915	-0.36	-30.01	-31.07
	1910	-0.45	-23.40	-21.64
	2690	-0.66	-14.25	-15.79
TRX3	915	-0.37	-28.77	-32.30
	1910	-0.46	-23.95	-21.76
	2690	-0.68	-14.68	-16.38
TRX4	915	-0.35	-30.29	-29.81
	1910	-0.41	-23.78	-22.42
	2690	-0.62	-14.32	-15.90
TRX5	915	-0.35	-27.13	-29.00
	1910	-0.46	-21.10	-20.31
	2690	-0.73	-13.41	-15.23
TRX6	915	-0.39	-29.44	-27.75
	1910	-0.48	-24.46	-24.59
	2690	-0.78	-13.47	-15.89
TRX7	915	-0.36	-29.06	-27.64
	1910	-0.45	-23.53	-24.03
	2690	-0.86	-12.07	-13.03
TRX8	915	-0.35	-28.94	-28.06
	1910	-0.42	-23.15	-22.28
	2690	-0.68	-13.53	-14.97
TRX9	915	-0.34	-29.09	-28.50
	1910	-0.44	-21.70	-20.72
	2690	-0.67	-13.68	-15.06
TRX10	915	-0.33	-30.19	-31.16
	1910	-0.41	-22.73	-21.08
	2690	-0.59	-15.11	-16.85

Table 10. Digital Interface Timing Specifications

(T_{op}= 25°C, VDD = 2.8 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Condition	Min.	Max.	Unit
Data Setup Time (Note 1)	T_S	See the Figure 6, input Tr/Tf = 3.5 to 6.5ns	1	-	ns
Data Hold Time (Note 1)	T_H	See the Figure 6, input Tr/Tf = 3.5 to 6.5ns	5	-	ns
Time for Data Output Valid from SCLK rising edge (Note 2)	T_D	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	0	22	ns
SDATA Output Transition (Rise/Fall) Time	$T_{SDATAOTR}$	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	2.1	10	ns
Data Drive Release Time	T_{SDATAZ}	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	-	18	ns
Vio Supply Rise Time	T_{VIO-R}	See the Figure 8	-	400	µs
RFFE I/O Voltage Reset Timing	$T_{VIO-RST}$	See the Figure 8	10	-	µs
Signal Reset Delay Time	T_{SIGOL}	See the Figure 8	120	-	µs
RF Switching Time	T_{SW}	See the Figure 9	-	5	µs
Switching Interval (Note 3)	T_{int}	See the Figure 9	20	-	µs
Startup Time (Note 4)	T_{SU}	See the Figure 4	-	20	µs

Note 1 : Input SDATA is sampled at the falling edge of the SCLK.
Note 2 : Output SDATA changes at the rising edge of the SCLK.
Note 3 : The time between the consecutive Register Write Command Sequences for the Switch State register.
Note 4 : The time for the switch to reach Active State.

Note : The table of input SCLK signal conditions as below.

Parameter	Symbol	Ratings		Unit
SCLK Frequency	F_{SCLK}	Full Speed	0.032 to 26	MHz
		Half Speed	0.032 to 13	
SCLK Period	T_{SCLK}	Full Speed	0.038 to 32	µs
		Half Speed	0.077 to 32	
SCLK Rise/Fall Time	$T_{SCLKITR}$	Full/Half Speed	3.5 to 6.5	ns
SCLK Input Duty Cycle, High/Low Time	$T_{SCLKDCH}$ $T_{SCLKDCL}$	50		%

AC Waveforms

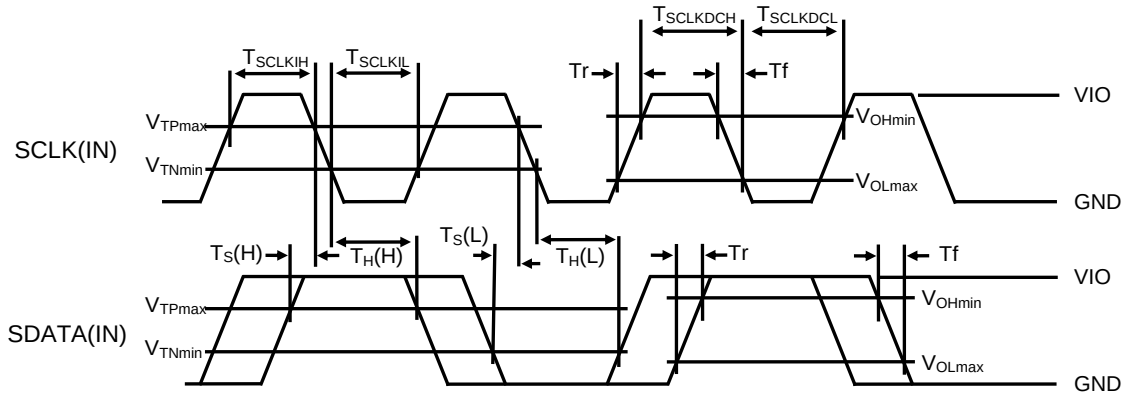


Figure 6. T_{SCLKDH}, $T_{SCLKDCL}$, T_{SCLKIH}, T_{SCLKIL}, T_S, T_H

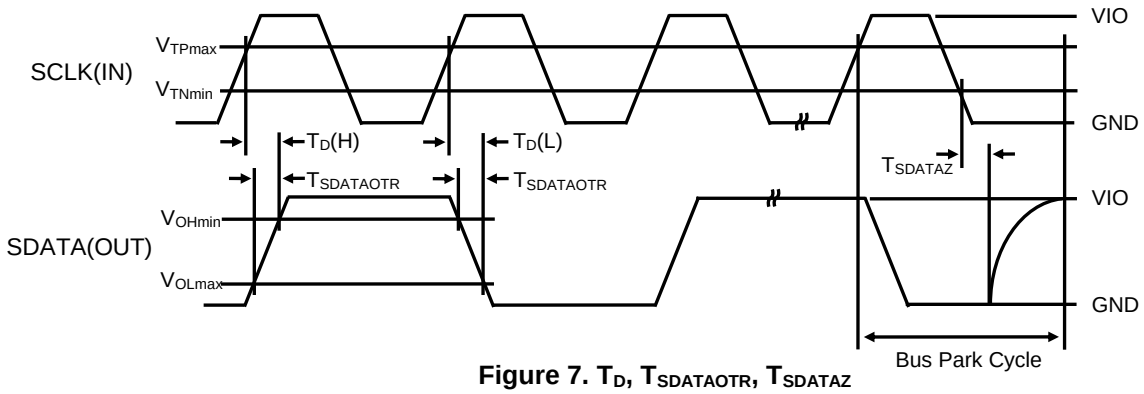


Figure 7. T_D, $T_{SDATAOTR}$, T_{SDATAZ}

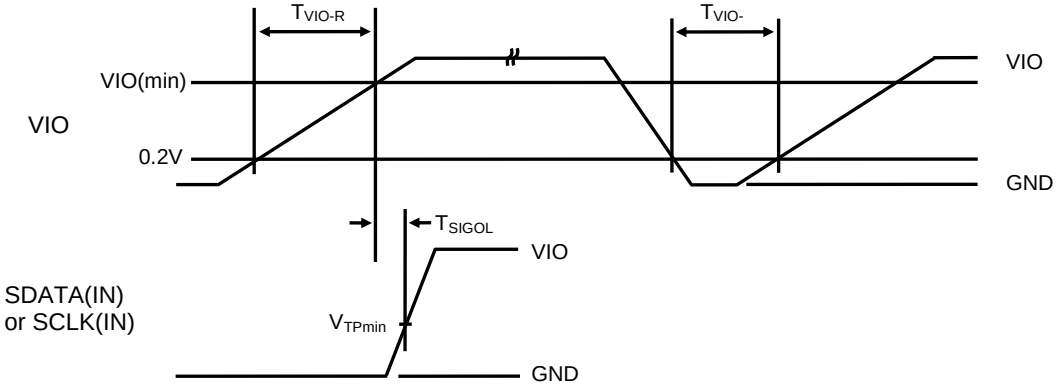


Figure 8. T_{VIO-R}, $T_{VIO-RST}$, T_{SIGOL}

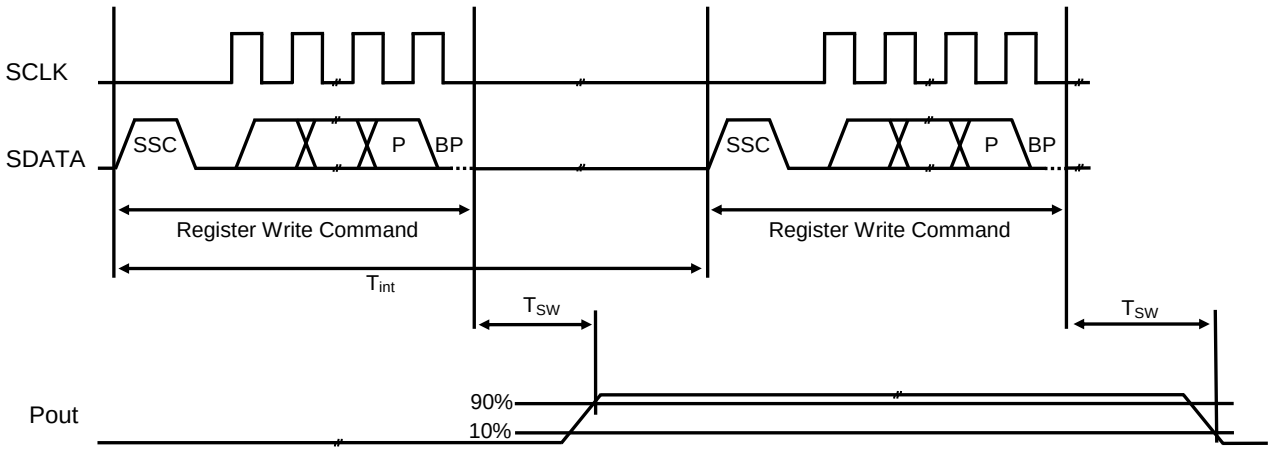


Figure 9. RF Switch Timing

Table 11. MIPI Transaction Details

Write

	State	SSC	USID				Command			Address					Parity	Data								Parity	Bus
			SA3	SA2	SA1	SA0	C7	C6	C5	C4	C3	C2	C1	C0	(P)	D7	D6	D5	D4	D3	D2	D1	D0	(P)	Park
SCLK																									
SDATA	TXLB - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0
	TXHB - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
	TRX1 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
	TRX2 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0
	TRX3 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0
	TRX4 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0
	TRX5 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0
	TRX6 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0
	TRX7 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0
	TRX8 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
	TRX9 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0
	TRX10 - ANT		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0
	Sleep		1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0
	All-Isolated		1	0	1	1	0	1	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	0	0

Read

	State	SSC	USID				Command			Address					Parity	Bus	Data								Parity	Bus
			SA3	SA2	SA1	SA0	C7	C6	C5	C4	C3	C2	C1	C0	(P)	Park	D7	D6	D5	D4	D3	D2	D1	D0	(P)	Park
SCLK																										
SDATA	Read MFR_ID (7:0)		1	0	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0	1	1	0	0	0
	Read MFR_ID (9:8) + USID		1	0	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	1	1	1	0
	Read PROD_ID		1	0	1	1	0	1	1	1	1	1	0	1	0	0	0	0	1	0	1	0	1	0	0	0
	Read FEM State Register		1	0	1	1	0	1	1	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	0

Table 12. Register Mapping

Table 12. shows the list of the registers inside the RMASMF496ATF03.

Register Address		Bits	Read/Write	Description	Default Value (binary)
Hex	Binary				
0x00	00000	[7:0]	R/W	Switch Control Register	See Table 13
0x1A	11010	[7:0]	R/W	RFFE Status (see Table 14)	0000 0000
0x1B	11011	[3:0]	R/W	GSID	0000 0000
0x1C	11100	[7:6] [5:0]	R/W	Power Mode (see Table 15) Triggers (see Table 16)	10 000000
0x1D	11101	[7:0]	R	Product ID	0010 1010
0x1E	11110	[7:0]	R	Manufacturer ID [7:0]	0010 0110
0x1F	11111	[7:6] [5:4] [3:0]	R	SPARE	00
				Manufacturer ID [9:8]	01
				USID	1011

Note : The RMASMF496ATF03 start-up procedure as below description.
The RMASMF496ATF03 requires to be disabled the triggers before programming the switch control registers when RMASMF496ATF03 operating in the active mode. The table of register address setup as below.

Register Address		Bits	Read/Write	Value (binary)
Hex	Binary			
0x1C	11100	[7:6] [5:0]	R/W	00 111000

Table 13. Switch Control Register

Antenna Path	Register_0 Bits							
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
2G transmit low band	0	0	0	0	1	0	1	0
2G transmit high band	0	0	0	0	1	0	0	0
TRX1	0	0	0	0	0	1	0	0
TRX2	0	0	0	0	0	1	0	1
TRX3	0	0	0	0	0	1	1	0
TRX4	0	0	0	0	0	1	1	1
TRX5	0	0	0	0	1	0	0	1
TRX6	0	0	0	0	1	0	1	1
TRX7	0	0	0	0	1	1	0	0
TRX8	0	0	0	0	0	0	0	1
TRX9	0	0	0	0	0	0	1	0
TRX10	0	0	0	0	0	0	1	1
Sleep mode	0	0	0	0	0	0	0	0
Isolation mode	0	1	1	1	1	1	1	1

Table 14. RFFE Status

D[7:0]	Read/Write	Description
D[7]	R/W	SOFTWARE RESET
D[6]	R	COMMAND_FRAME_ PARITY_ERR
D[5]		COMMAND_LENGTH_ERR
D[4]		ADDRESS_FRAME_PARITY_ERR
D[3]		DATA_FRAME_PARITY_ERR
D[2]		READ_UNUSED_REG
D[1]		WRITE_UNUSED_REG
D[0]		BID_GID_ERR

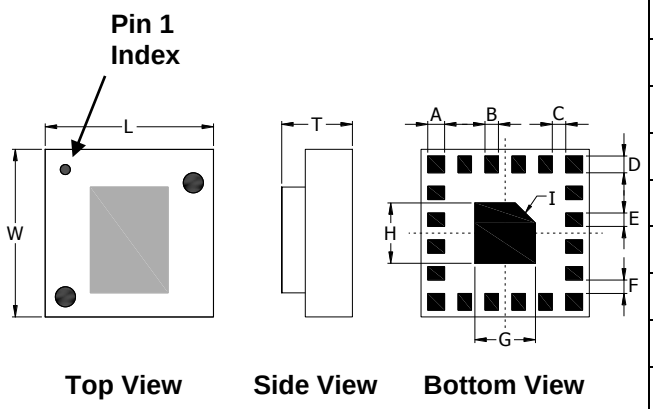
Table 15. Power Mode

D[7:6]	Read/Write	Status
00b	W	Part enters Active mode
	R	Part is in Active mode
01b	W	Part enters Start Up mode - part is reset
	R	Start Up mode will immediately transition to Low Power mode
10b	W	Part enters Low Power mode
	R	Part is in Low Power mode
11b	N/A	Will not occur - The state is discarded
		Will not occur - The state is discarded

Table 16. Trigger States

D[5:0]	Read/Write	Status
D[5]	R/W	1 = Trigger 2 Disabled, 0 = Trigger 2 Enabled
D[4]		1 = Trigger 1 Disabled, 0 = Trigger 1 Enabled
D[3]		1 = Trigger 0 Disabled, 0 = Trigger 0 Enabled
D[2]	W	1 = Load Bits to Trigger 2, Trigger 2 states is Disabled
D[1]		1 = Load Bits to Trigger 1, Trigger 1 states is Disabled
D[0]		1 = Load Bits to Trigger 0, Trigger 0 states is Disabled

Table 17. Dimensions

Figure	Symbol	Dimension
	L	2.50 ± 0.10mm
	W	2.50 ± 0.10mm
	T	0.78 ± 0.10mm
	A	0.25 ± 0.10mm
	B	0.20 ± 0.10mm
	C	0.20 ± 0.10mm
	D	0.25 ± 0.10mm
	E	0.20 ± 0.10mm
	F	0.20 ± 0.10mm
	G	0.90 ± 0.10mm
	H	0.90 ± 0.10mm
	I	0.30 ± 0.05mm x 45°

Solder land pattern for reference only

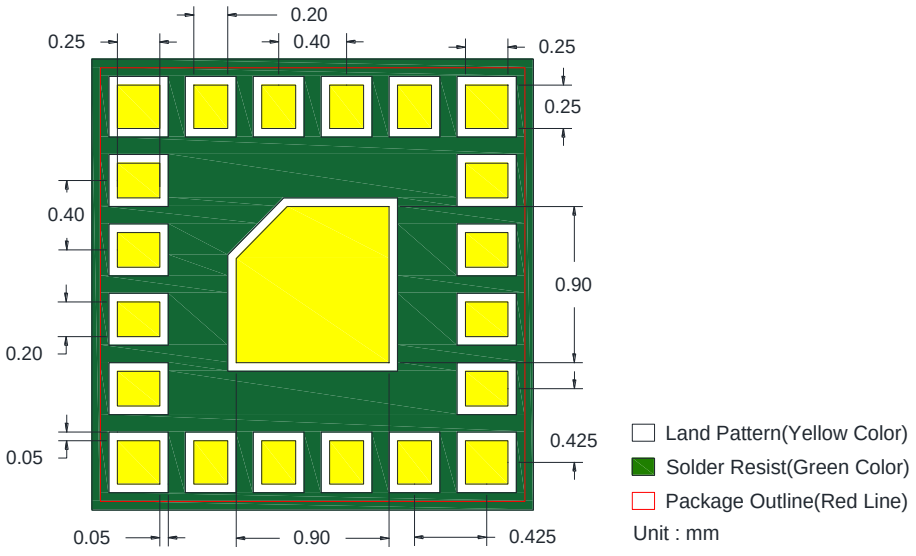


Figure 10. Solder Land Pattern Top View

Reliability test

TEST	PROCEDURE / TEST METHOD	REQUIREMENT
Solderability JIS C 0050-4.6 JESD22-B102D	*Solder bath temperature：255 ± 5°C *Immersion time：5 ± 0.5 sec Solder：Sn3Ag0.5Cu for lead-free	At least 95% of a surface of each terminal electrode must be covered by fresh solder.
High temperature JIS C 0021	*Temperature：90°C±2°C *Test duration：1000+24/-0 hours Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
Low temperature JIS C 0020	*Temperature：-30°C±2°C *Test duration：1000+24/-0 hours Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
Temperature cycle JIS C 0025	1. 30±3 minutes at -30±3°C, 2. 10~15 minutes at room temperature, 3. 30±3 minutes at +90±3°C, 4. 10~15 minutes at room temperature, Total 100 continuous cycles Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
High temperature operation life (HTOL)	*Temperature：90°C *VDD = 4.8V *Time：1000+24/-0 hrs. Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.

Soldering condition

Typical examples of soldering processes that provide reliable joints without any damage are given in Figure 11.

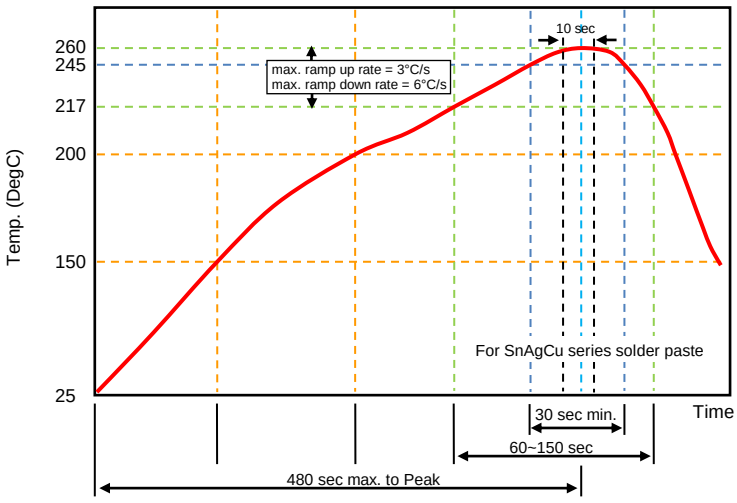


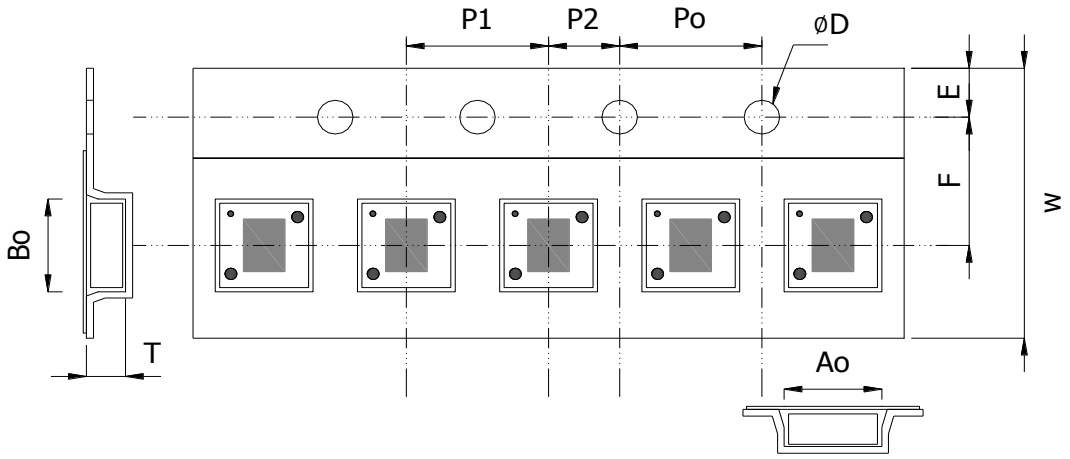
Figure 11. Infrared soldering profile

Ordering code

RM	ASM	F	496A	T
RF module RM: Walsin RF Module Device	**Module type** ASM: Antenna Switch Module	**Application** F: SP12T	**Design Code**	**Packing** T: Taping

Minimum Ordering Quantity: 3000 pcs per reel.

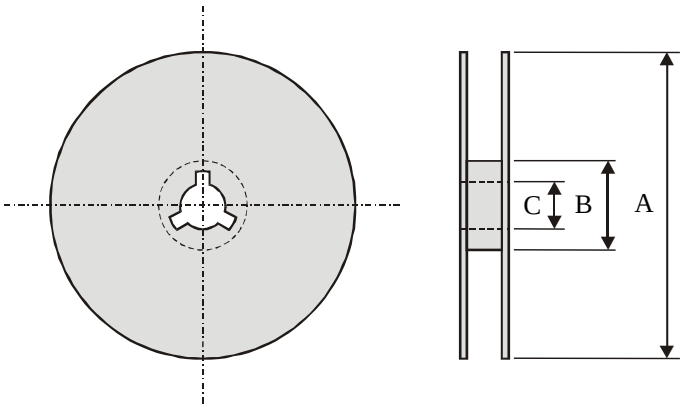
Packaging



Plastic Tape specifications (unit :mm)

Index	Ao	Bo	ΦD	T	W
Dimension (mm)	2.75 ± 0.10	2.75 ± 0.10	1.55 ± 0.05	1.30 ± 0.10	8.0 ± 0.10
Index	E	F	Po	P1	P2
Dimension (mm)	1.75 ± 0.10	3.50 ± 0.05	4.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05

Reel dimensions



Index	A	B	C
Dimension (mm)	Φ178.0	Φ60.0	Φ13.0

Taping Quantity : 3000 pieces per 7” reel

Caution of handling

Limitation of Applications

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects, which might directly cause damage to the third party's life, body or property.

(1) Aircraft equipment
(2) Aerospace equipment
(3) Undersea equipment
(4) Medical equipment
(5) Disaster prevention / crime prevention equipment
(6) Traffic signal equipment
(7) Transportation equipment (vehicles, trains, ships, etc.)
(8) Applications of similar complexity and /or reliability requirements to the applications listed in the above.

Storage condition

(1) Products should be used in 6 months from the day of WALSIN outgoing inspection, which can be confirmed.

(2) Storage environment condition.

- Products should be storage in the warehouse on the following conditions.
- Temperature : -10 to +40°C
- Humidity : 30 to 70% relative humidity
- Don't keep products in corrosive gases such as sulfur. Chlorine gas or acid or it may cause oxidization of electrode, resulting in poor solderability.
- Products should be storage on the palette for the prevention of the influence from humidity, dust and son on.
- Products should be storage in the warehouse without heat shock, vibration, direct sunlight and so on.
- Products should be storage under the airtight packaged condition.