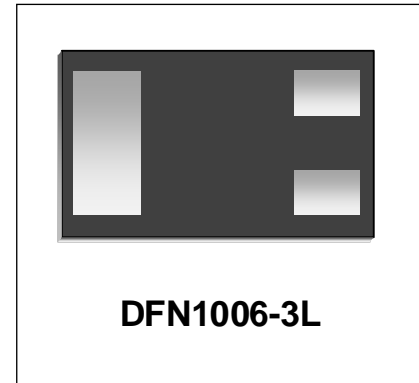


Features

- 36 Watts Peak Power per Line ($t_p = 8/20\mu s$)
- Protects two I/O lines
- Low operating voltage: 5V
- Low capacitance($<0.45pF$)
- Solid-state technology

IEC COMPATIBILITY (EN61000-4)

- IEC 61000-4-2 (ESD) $\pm 12kV$ (air), $\pm 12kV$ (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 3A (8/20 μs)



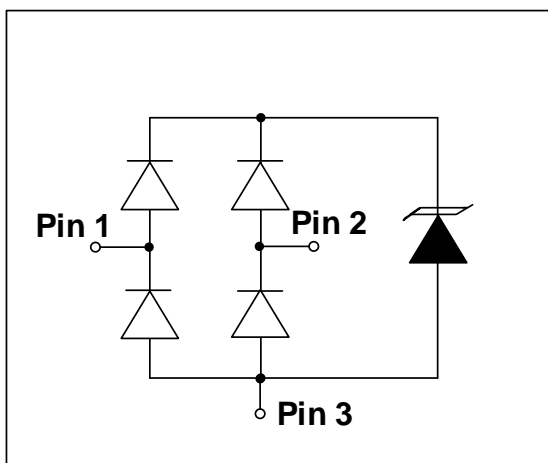
Mechanical Characteristics

- JEDEC DFN1006-3L package
- Marking : Making Code
- Packaging : Tape and Reel per EIA 481
- RoHS Compliant & HF
- Device meets MSL1 requirement

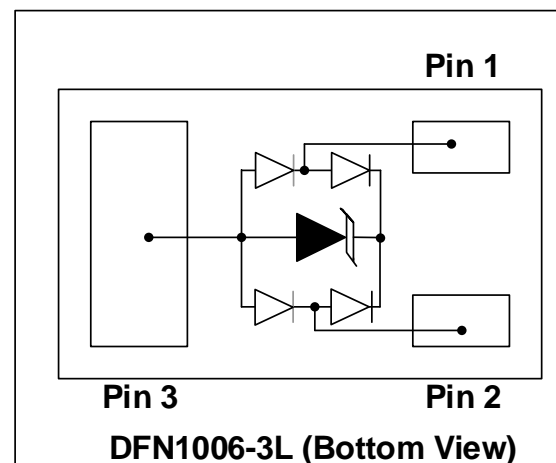
Applications

- FireWire & USB
- Sensitive Analog Inputs
- Portable Electronics
- LAN/WAN equipment
- Video Line Protection
- Microcontroller Input Protection

Circuit Diagram



Schematic & PIN Configuration

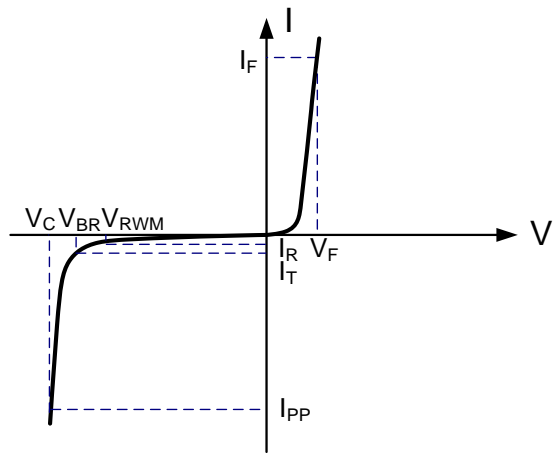


Absolute Maximum Rating

| Rating | Symbol | Value | Units |
|--|-----------|-------------|-------------|
| Peak Pulse Power ($t_p=8/20\mu s$) | P_{PP} | 36 | Watts |
| Peak Pulse Current ($t_p=8/20\mu s$) | I_{PP} | 3 | A |
| Operating Temperature | T_J | -55 to +125 | $^{\circ}C$ |
| Storage Temperature | T_{STG} | -55 to +150 | $^{\circ}C$ |

Electrical Parameters

| Symbol | Parameter |
|-----------|-------------------------------------|
| I_{PP} | Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Reverse Stand-Off Voltage |
| I_R | Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |



Electrical Characteristics (T=25 $^{\circ}C$ unless otherwise noted)

| WE05MGC | | | | | | |
|-----------------------------------|-----------|--|---------|---------|---------|----------|
| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units |
| Reverse Stand-Off Voltage | V_{RWM} | | | | 5.0 | V |
| Breakdown Voltage | V_{BR} | $I_T=1mA$ | 6.0 | | | V |
| Forward Voltage | V_F | $I_F=10mA$ | 0.6 | | 1.2 | V |
| Reverse Leakage Current | I_R | $V_{RWM}=5V$ | | | 200 | nA |
| Clamping Voltage | V_C | $I_{PP}=3A, t_p=8/20\mu s$ | | 10.5 | 12 | V |
| Dynamic Resistance ^{1,2} | R_{DYN} | TLP=0.2/100ns | | 0.5 | | Ω |
| ESD Clamping Voltage ¹ | V_C | $I_{PP} = 4A,$ $t_p = 0.2/100ns$ (TLP) | | 9.8 | | V |
| ESD Clamping Voltage ¹ | V_C | $I_{PP} = 16A,$ $t_p = 0.2/100ns$ (TLP) | | 15.8 | | V |
| Junction Capacitance | C_j | $V_R=0V, f=1MHz$ Between I/O pins and Gnd | | 0.35 | 0.45 | pF |
| | | $V_R=0V, f=1MHz$ Between I/O pins | | 0.20 | 0.30 | pF |

Notes : 1、 TLP Setting : $t_p=100ns, t_r=0.2ns, I_{TLP}$ and V_{TLP} sample window: $t_1=70ns$ to $t_2=90ns$.
 2、 Dynamic resistance calculated from $I_{PP}=4A$ to $I_{PP}=16A$ using "Best Fit".

Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

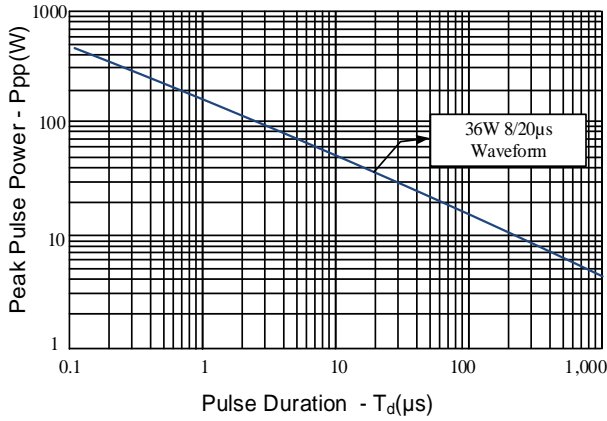


Figure 2: Power Derating Curve

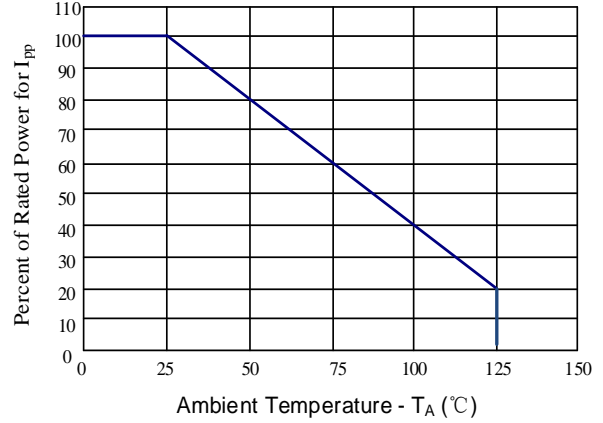


Figure 3: Clamping Voltage vs. Peak Pulse Current

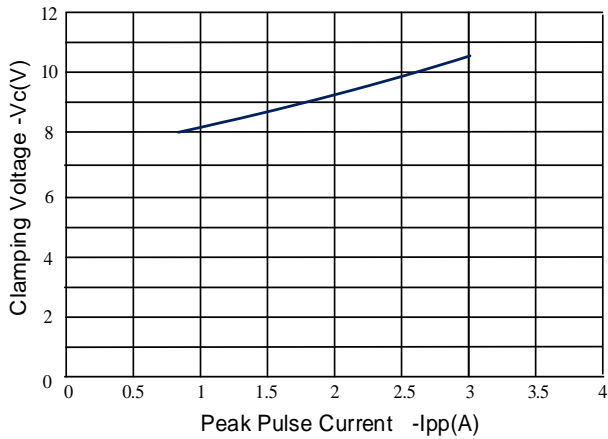


Figure 4: Normalized Junction Capacitance vs. Reverse Voltage

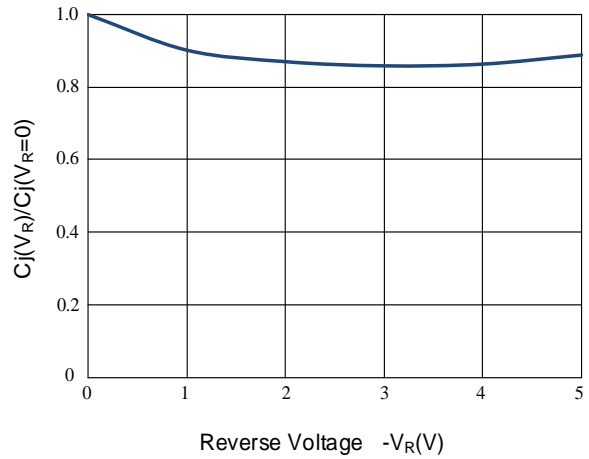


Figure 5: Pulse Waveform

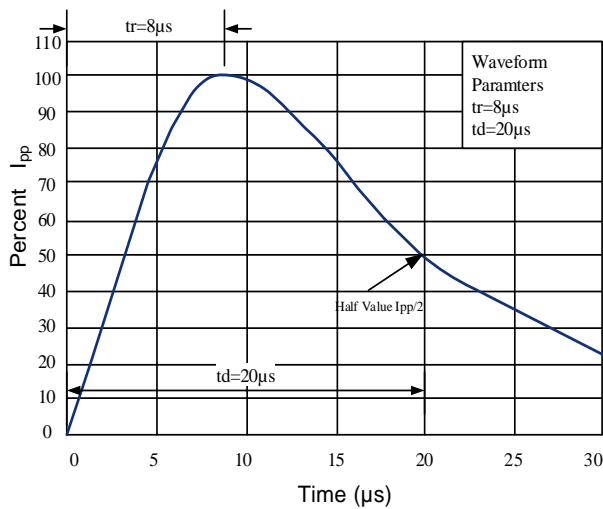
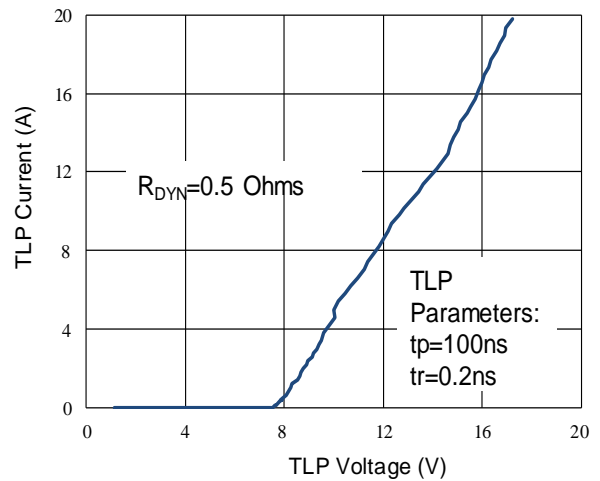
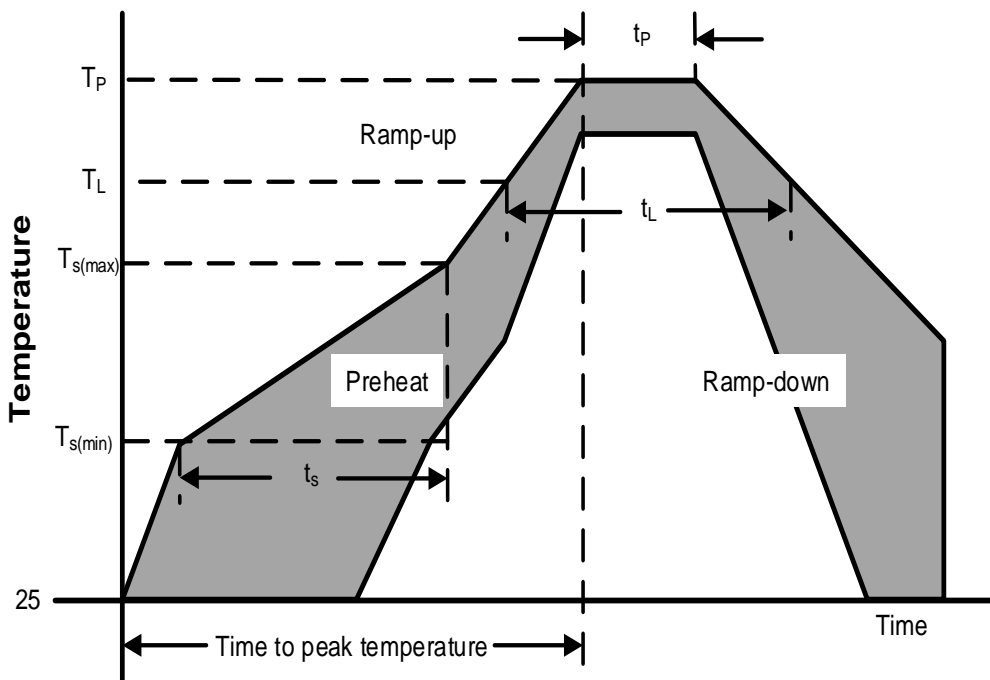


Figure 6: TLP I-V Curve



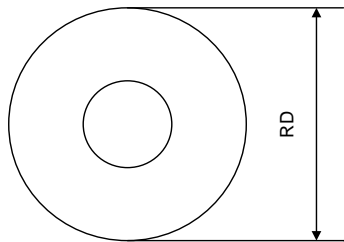
Soldering Parameters

| Reflow Condition | | Pb – Free assembly |
|--|----------------------------------|--------------------|
| Pre Heat | Temperature Min ($T_{s(min)}$) | 150°C |
| | Temperature Max ($T_{s(max)}$) | 200°C |
| | Time (min to max) (t_s) | 60 – 190 secs |
| Average ramp up rate (Liquidus Temp) (T_L) to peak | | 5°C/second max |
| $T_{s(max)}$ to T_L — Ramp-up Rate | | 5°C/second max |
| Reflow | Temperature (T_L) (Liquidus) | 217°C |
| | Temperature (t_L) | 60 – 150 seconds |
| Peak Temperature (T_P) | | 260+0/-5 °C |
| Time within actual peak Temperature (t_p) | | 20 – 40 seconds |
| Ramp-down Rate | | 5°C/second max |
| Time 25°C to peak Temperature (T_P) | | 8 minutes Max. |
| Do not exceed | | 280°C |

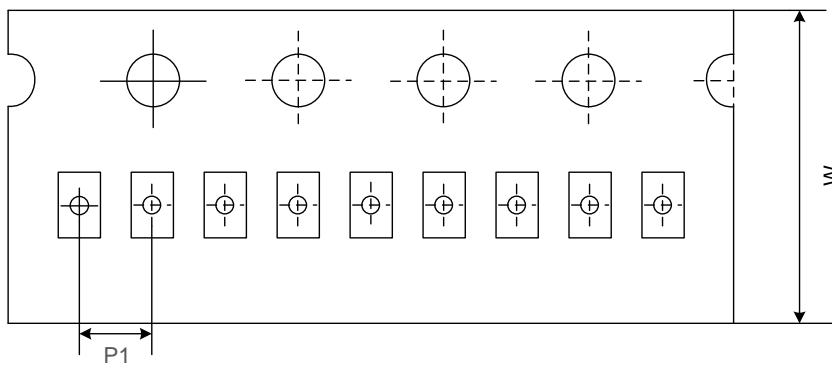


Tape And Reel Information

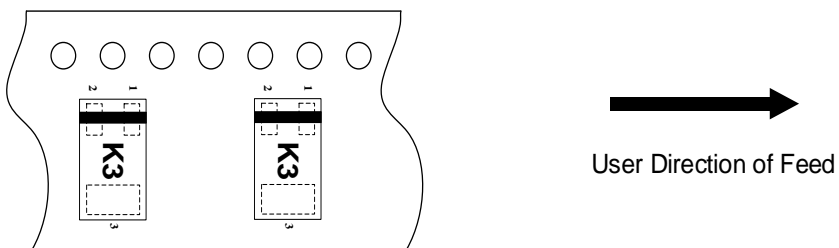
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



| | | |
|----|---|--------|
| RD | Reel Dimensions | 7 inch |
| W | Overall width of the carrier tape | 8 mm |
| P1 | Pitch between successive cavity centers | 2mm |

Outline Drawing – DFN1006-3L

PACKAGE OUTLINE

TOP VIEW

BOTTOM VIEW

DFN1006-3L

| SYMBOL | MILLIMETERS | | |
|--------|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.45 | 0.50 | 0.60 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.45 | 0.50 | 0.55 |
| b1 | 0.10 | 0.15 | 0.20 |
| C | 0.12 | 0.15 | 0.18 |
| D | 0.95 | 1.00 | 1.05 |
| e | 0.65BSC | | |
| E | 0.55 | 0.60 | 0.65 |
| E1 | 0.15 | 0.20 | 0.25 |
| L | 0.20 | 0.25 | 0.30 |
| L1 | 0.05REF | | |

Land Pattern

Marking Codes

| Part Number | Marking Code |
|-------------|--------------|
| WE05MGC | |

Package Information

Qty: 10k/Reel

CONTACT INFORMATION

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WAYON website: <http://www.way-on.com>

For additional information, please contact your local Sales Representative.

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Specifications are subject to change without notice.
The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.
Users should verify actual device performance in their specific applications.

单击下面可查看定价，库存，交付和生命周期等信息

[>>WAY-ON\(维安\)](#)