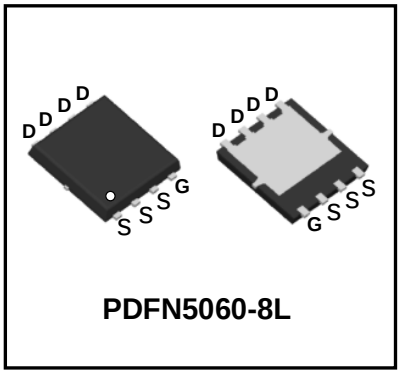
WMB125N12LG2

120V N-Channel Enhancement Mode Power MOSFET

Description

WMB125N12LG2 uses Wayon's 2nd generation POWERTRENCH MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.

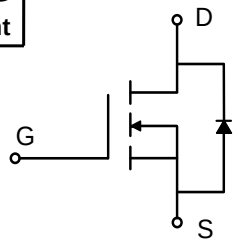


PDFN5060-8L

Features

- V_{DS} = 120V, I_D = 61A(Silicon Limited)
  $R_{DS(on)}$ < 12.5mΩ @ V_{GS} = 10V
  $R_{DS(on)}$ < 17mΩ @ V_{GS} = 4.5V
- Green Device Available
- 100% EAS Guaranteed
- Optimized for High Speed Smooth Switching

RoHS compliant



Applications

- Power Management Switches
- DC/DC Converters
- Synchronous Rectification in SMPS

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source voltage		V_{DS}	120	V
Gate-Source voltage		V_{GS}	±20	V
Continuous Drain Current[1](Silicon Limited)	T_C=25℃	I_D	61	A
	T_C=100℃		38	
Continuous Drain Current[1](Package Limited)	T_C=25℃		60	
Pulsed Drain Current[2]		I_{DM}	250	A
Single Pulse Avalanche Energy[3]		EAS	245	mJ
Avalanche Current		I_{AS}	35	A
Total Power Dissipation[4]	T_C=25℃	P_D	92	W
Operating Junction and Storage Temperature Range		T_J , T_{STG}	-55 to+150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[1]	$R_{\theta JA}$	49.6	°C/W
Thermal Resistance from Junction-to-Case[1]	$R_{\theta JC}$	1.3	°C/W

Electrical Characteristics T_c = 25°C, unless otherwise noted

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	120	-	-	V
Gate-body Leakage Current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25℃	I_{DSS}	V_{DS} = 120V, V_{GS} = 0V	-	-	1	μA
	T_J=100℃			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	2.0	2.5	V
Drain-Source On-Resistance[2]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	9.7	12.5	mΩ
			V_{GS} = 4.5V, I_D = 20A	-	12	17	
Forward Transconductance		g_{fs}	V_{DS} = 5V, I_D = 20A	-	64	-	S
Dynamic Characteristics							
Input Capacitance		C_{iss}	V_{DS} = 60V, V_{GS} =0V, f =1MHz	-	2100	-	pF
Output Capacitance		C_{oss}		-	245	-	
Reverse Transfer Capacitance		C_{rss}		-	10	-	
Switching Characteristics							
Gate Resistance		R_g	V_{DS}=0V, V_{GS} =0V, f =1MHz	-	2.1	-	Ω
Total Gate Charge		Q_g	V_{GS} = 4.5V, V_{DD} = 60V, I_D= 20A	-	14.7	-	nC
Total Gate Charge		Q_g	V_{GS} = 10V, V_{DD} = 60V, I_D= 20A	-	30.5	-	
Gate-Source Charge		Q_{gs}		-	7.9	-	
Gate-Drain Charge		Q_{gd}		-	4.0	-	
Turn-On Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DD} = 60V,R_G = 10Ω, I_D= 20A	-	10.5	-	nS
Rise Time		t_r		-	8.8	-	
Turn-Off Delay Time		$t_{d(off)}$		-	17	-	
Fall Time		t_f		-	9.8	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[2]		V_{SD}	I_S = 1A, V_{GS} = 0V	-	-	1.2	V
Reverse Recovery Time		t_{rr}	V_R =60V, I_F=20A, dI_F/dt=100A/μs	-	49	-	ns
Reverse Recovery Charge		Q_{rr}		-	73	-	nC

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.4mH, I_{AS}=35A

4.The power dissipation is limited by 150℃ junction temperature

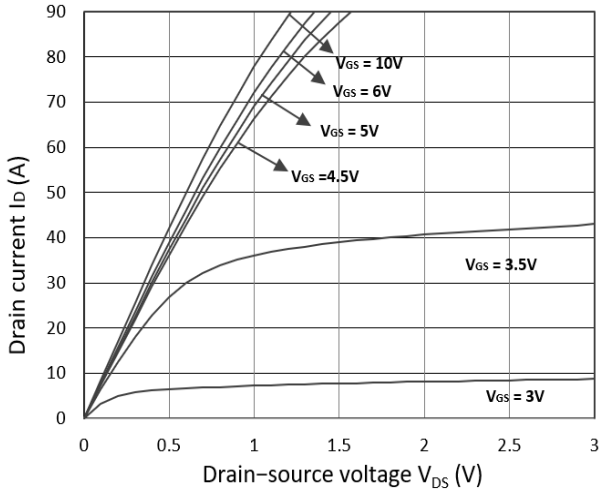


Figure 1. Output Characteristics

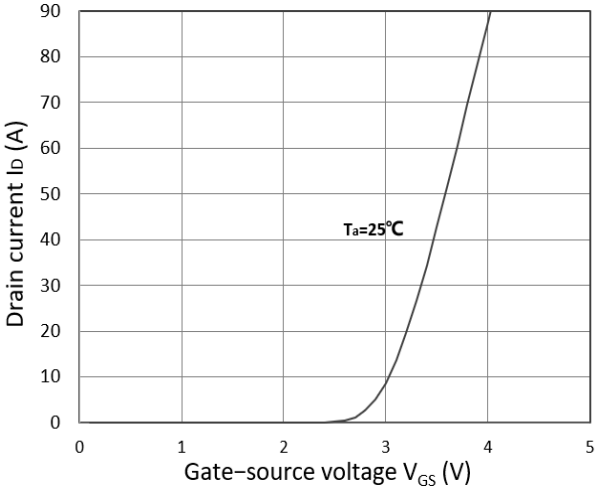


Figure 2. Transfer Characteristics

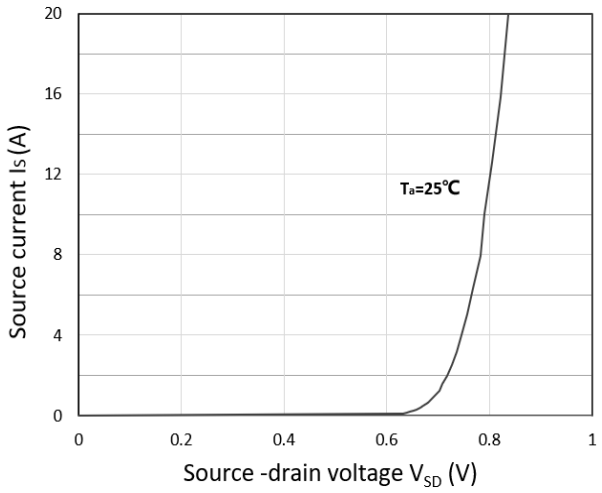


Figure3. Forward Characteristics of Reverse

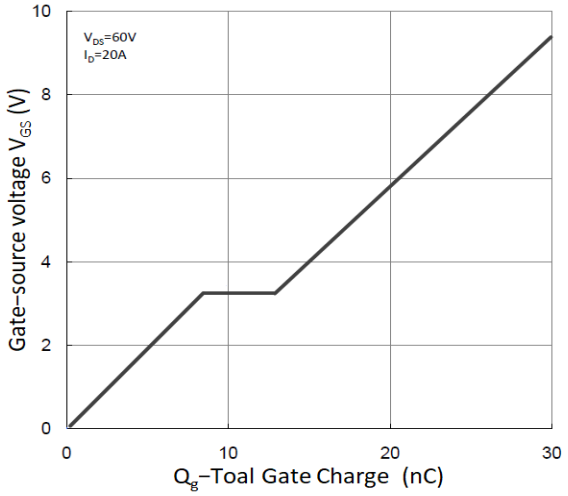


Figure4.Gate Charge Characteristics

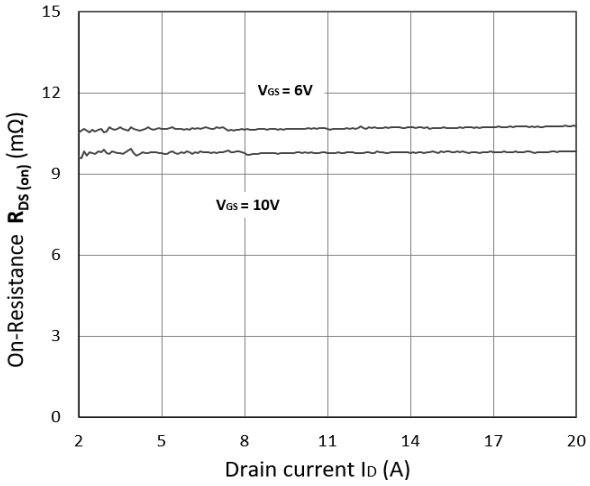


Figure 5. $R_{DS(ON)}$ Vs I_D

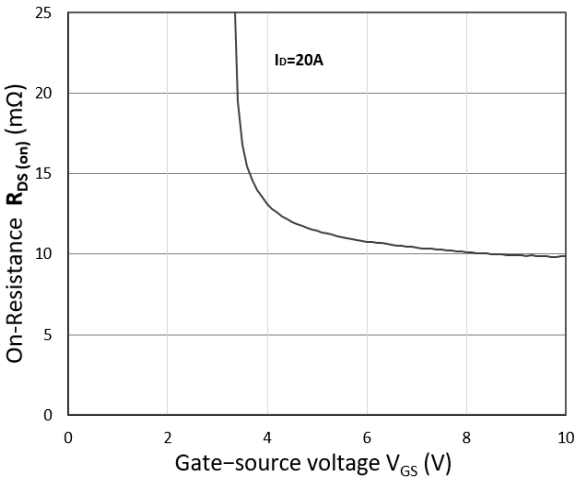


Figure 6. $R_{DS(ON)}$ vs. V_{GS}

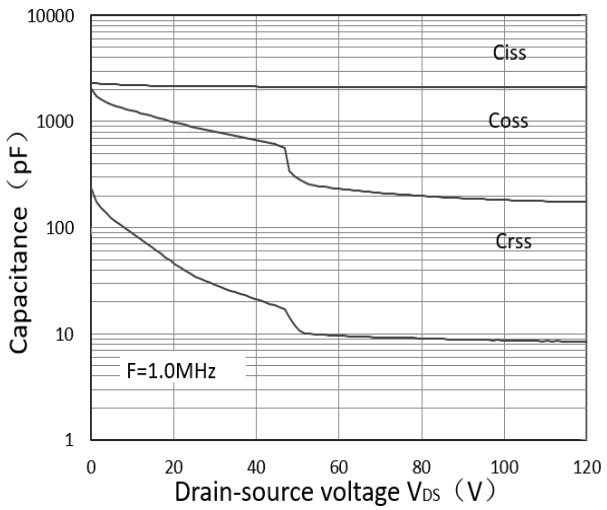


Figure 7. Capacitance Characteristics

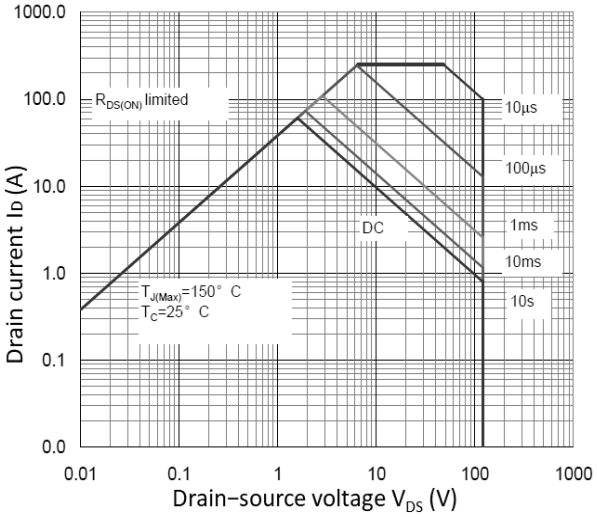


Figure 8. Safe Operating Area

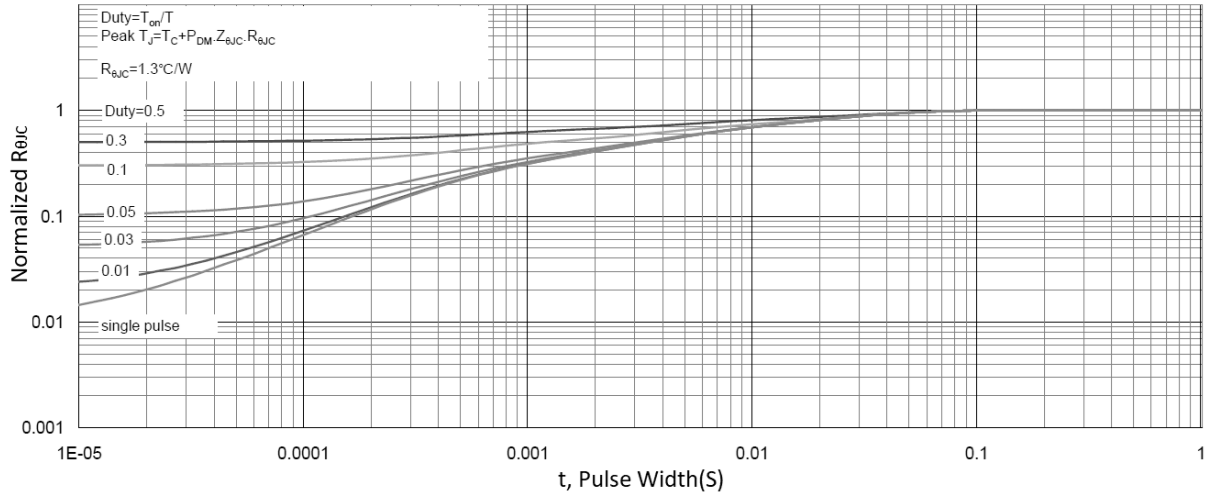


Figure 9. Normalized Maximum Transient Thermal Impedance

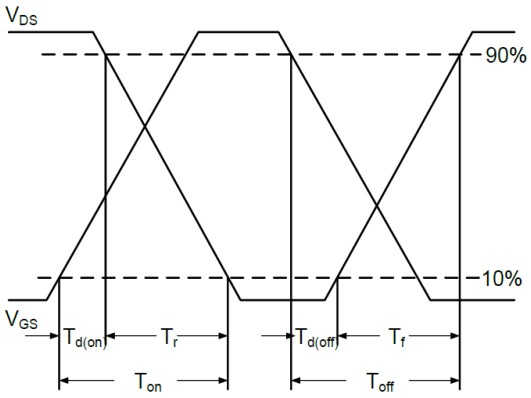


Figure 9.Switching Time Waveform

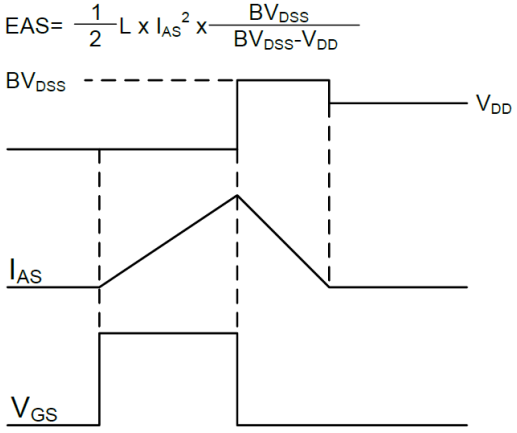
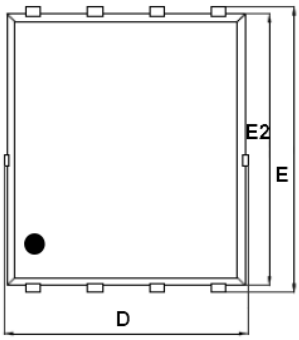
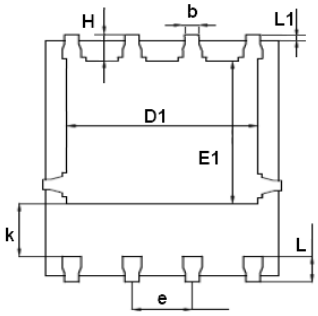


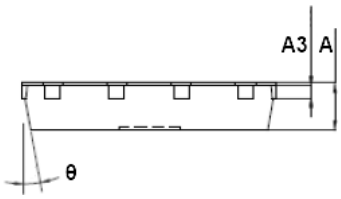
Figure 10.Unclamped Inductive Switching Waveform

Mechanical Dimensions for PDFN5060-8L

COMMON DIMENSIONS





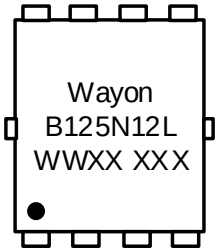


SYMBOL	MM	
	MIN	MAX
A	0.90	1.17
A3	0.20	0.35
D	4.80	5.40
E	5.90	6.15
D1	3.61	4.31
E1	3.30	3.78
E2	5.65	5.85
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.61
θ	0°	12°

Ordering Information

Part	Package	Marking	Packing method
WMB125N12LG2	PDFN5060-8L	B125N12L	Tape and Reel

Marking Information



B125N12L = Device code

WWXX XXX= Date code

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