

USB Connector Over Temperature IC

General Description

WP1682 is a temperature protection IC for USB or Type-C charging connector, with external NTC Thermistor, controlling built-in NMOS switch through inner delay and logic processing circuits to protect charging equipment.

WP1682 is an overheating protection product, using charge pump driver to control the switching state of built-in power NMOS switch on VBUS. When the external NTC resistance sensing temperature is within the normal range, the power NMOS is on. While the NTC sensing temperature is too high and is confirmed to exceed the set value by the internal logic and delay processing, the power NMOS will be shut off to pull down VBUS power supply to protect charging equipment, until the NTC

cools down again, after reset by re-plugging the power supply or equipment, NMOS switch would be turned on to restore VBUS power supply .

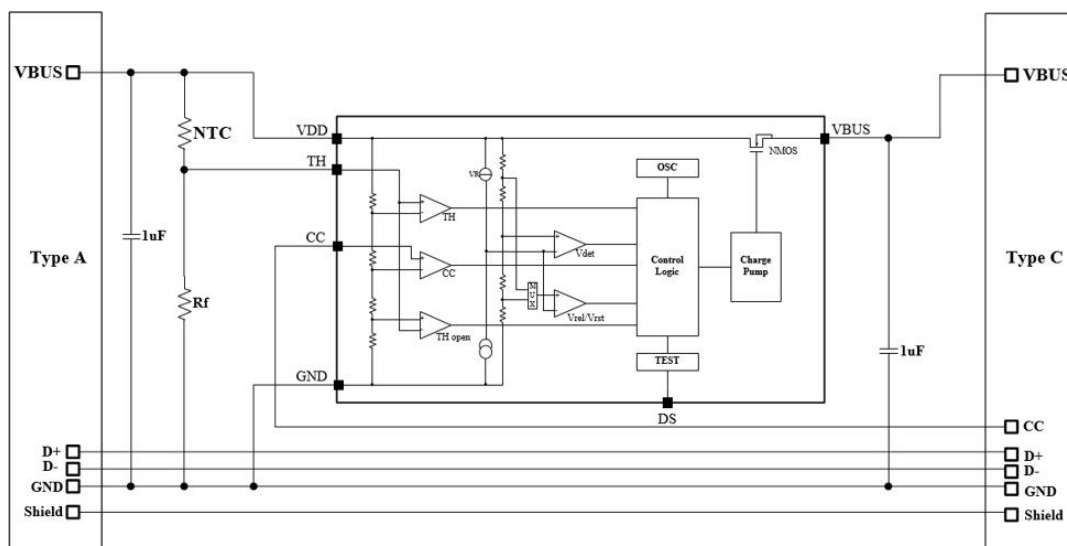
Applications

- USB or Type-C connector for charger

Features

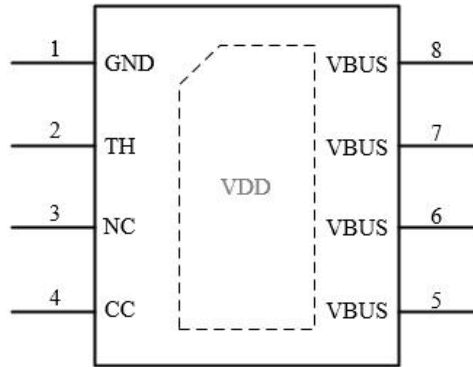
- TH pin detection voltage:
(VDD=5V) 4.165V
($0.833 \times VDD$) $\pm 0.055V$
- TH pin detection dead time: > 20ms
- Low voltage Detect Delay time: > 20ms
- Reset release Delay time: < 200ms
- On-resistance of NMOS switch: $5m\Omega$ (Typ)
- Reset release Voltage: < 4.5V
- Working temperature range: $-40 \sim 85^\circ C$
- Package: DFN-8 (0303*0.75-0.65)

Typical Application



Note: This is a typical application of chip for reference only.

Pin Configuration



(TOP VIEW)

Pin Description

Pin Number	Pin Name	I/O	Function
1	GND	Input	Ground
2	TH	Input	Temperature detection input.
3	NC	/	/
4	CC	Input	Device end plugging detection input, recommended to connect to type-C interface CC pin or to pull up to VDD by Rp. Connect to GND to bypass device end plugging detection.
5,6,7,8	VBUS	Output	Output Voltage. Output of internal NMOS switch and power supply for load.
TAB	VDD	Input	Power supply

Absolute Maximum Ratings

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3~16	V
OUT terminal voltage	VOUT	-0.3~VDD+0.3	V
Storage temperature	Tstg	-55~125	°C
Operating ambient	Topr	-40~85	°C
Operating voltage	Vop	3.3~13.5	V
Power dissipation	Pd	1000	mW

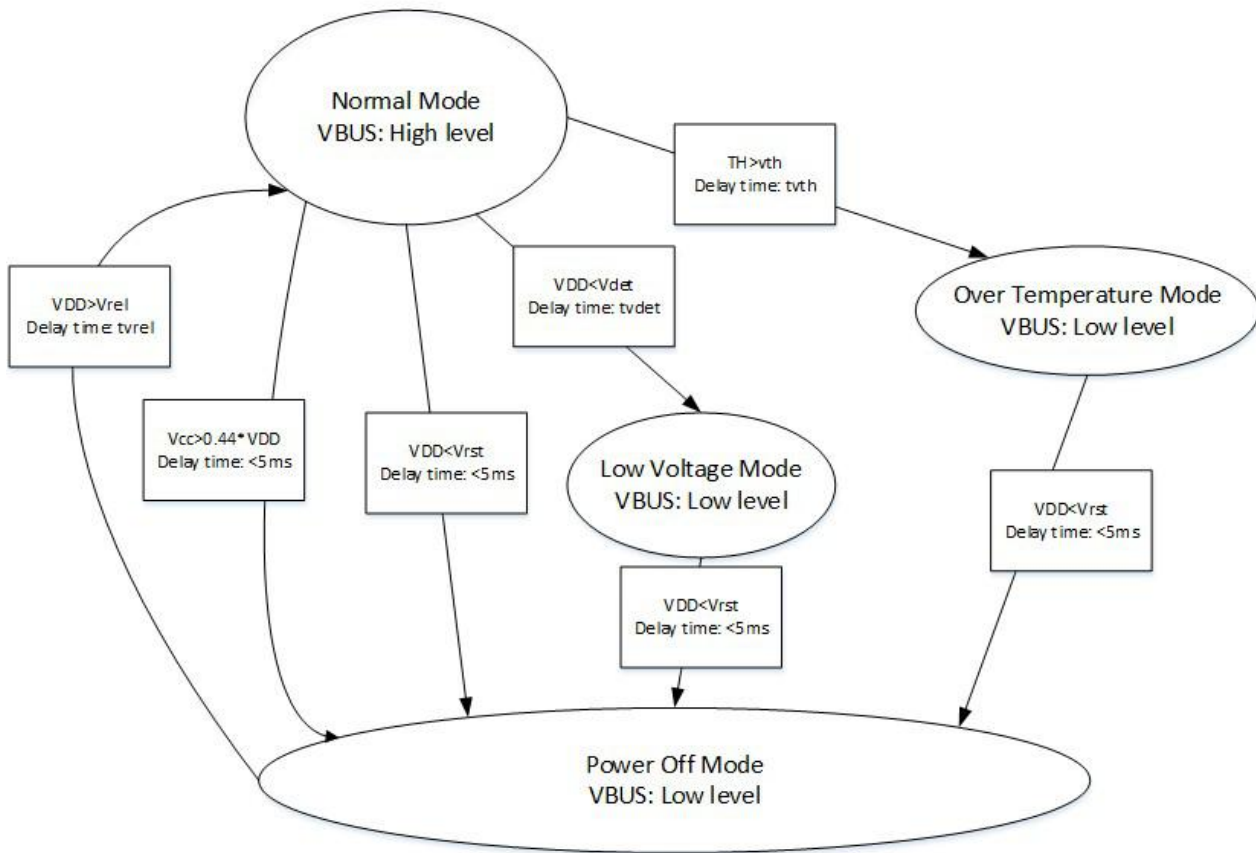
Note: Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Electrical Characteristics

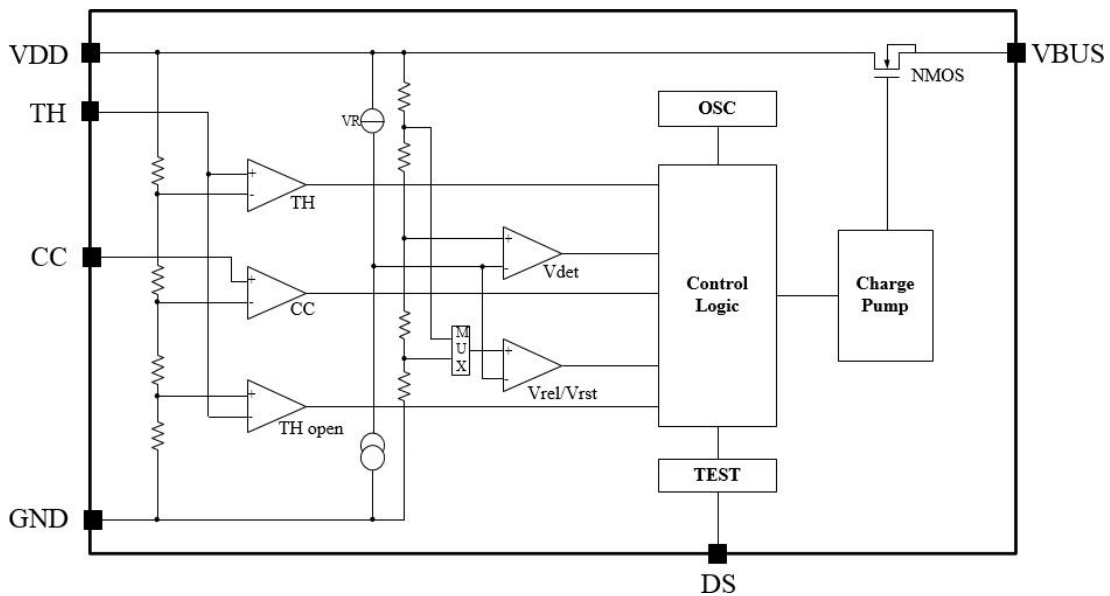
(T_A=25 °C, V_{IN}=5V, unless otherwise noted)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Recommended Operating Voltage	VDD		3.3		13.5	V
Consumption current 1	I _{dd1}	VDD=5V		40		μA
Consumption current 1	I _{dd2}	VDD=12V		80		μA
TH pin detection voltage 1	V _{th1}	VDD=5V TH=2.5V->V _{th1}	4.110	4.165	4.220	V
TH pin detection voltage 2	V _{th2}	VDD=5V,9V,12V TH=0.5×VDD ->V _{th2}	0.822×VDD	0.833×VDD	0.844×VDD	V
TH pin detection dead time	t _{vth}	VDD=5V	20		150	ms
Low voltage Detect	V _{det}	VDD=5V->V _{det} TH=0.5×VDD	V _{rel} -0.4		V _{rel} -0.1	V
Low voltage Detect Delay time	t _{vdet}	VDD=5V->3.5V TH=0.5×VDD	20		150	ms
Reset detection voltage	V _{rst}	VDD=5V->V _{rst} TH=0.5×VDD	V _{det} -0.4		V _{det} -0.1	V
Reset release voltage	V _{rel}	VDD=0V->V _{rel} TH=0.5×VDD	3		4.5	V
Reset release Delay time	t _{vrel}	VDD=V _{rst} ->5V TH=0.5×VDD	30		200	ms
TH pin open detection voltage	V _{th_open}	VDD=5V,9V,12V TH=0.5×VDD ->V _{th_open}	TYP-70mV	0.03×VDD	TYP+70mV	V
Thermistor open detection Delay time	T _{open}	VDD=5V TH=0.5×VDD->0V	20		150	ms
Threshold voltage of CC	V _{cc}	VDD=5V,9V,12V	0.42×VDD	0.44×VDD	0.46×VDD	V
On-resistance of NMOS switch	R _{on}	VDD=5V, I _{load} =1A		5		mΩ

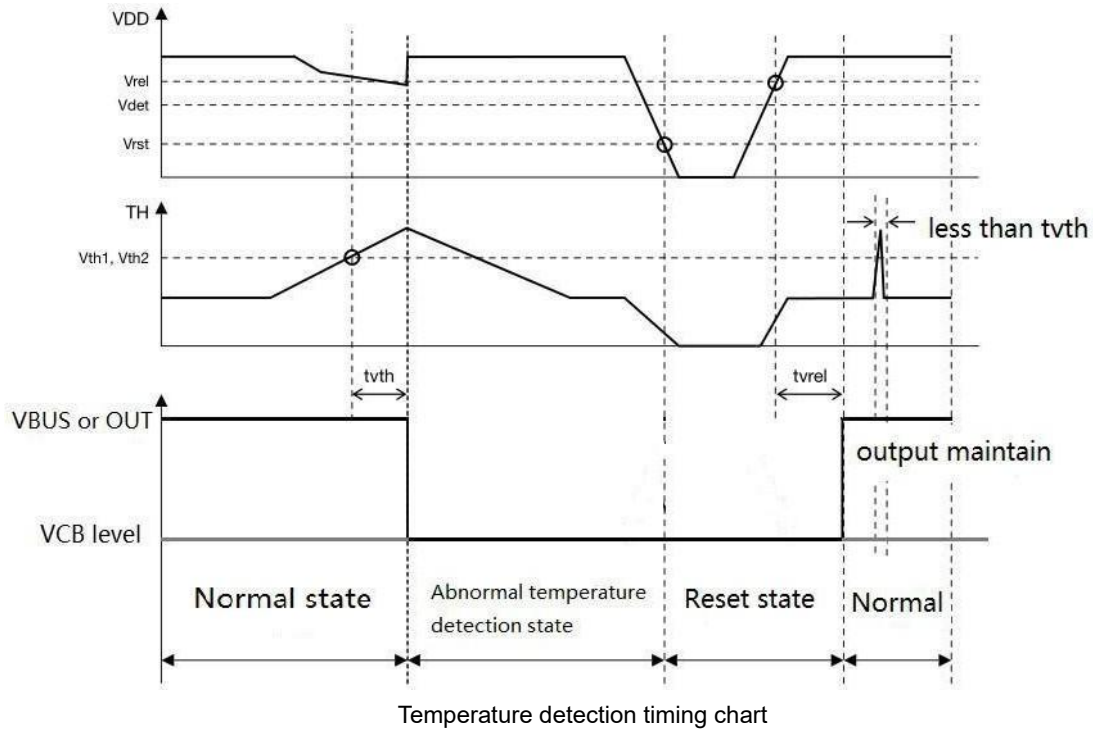
Flow diagram



Block Diagram



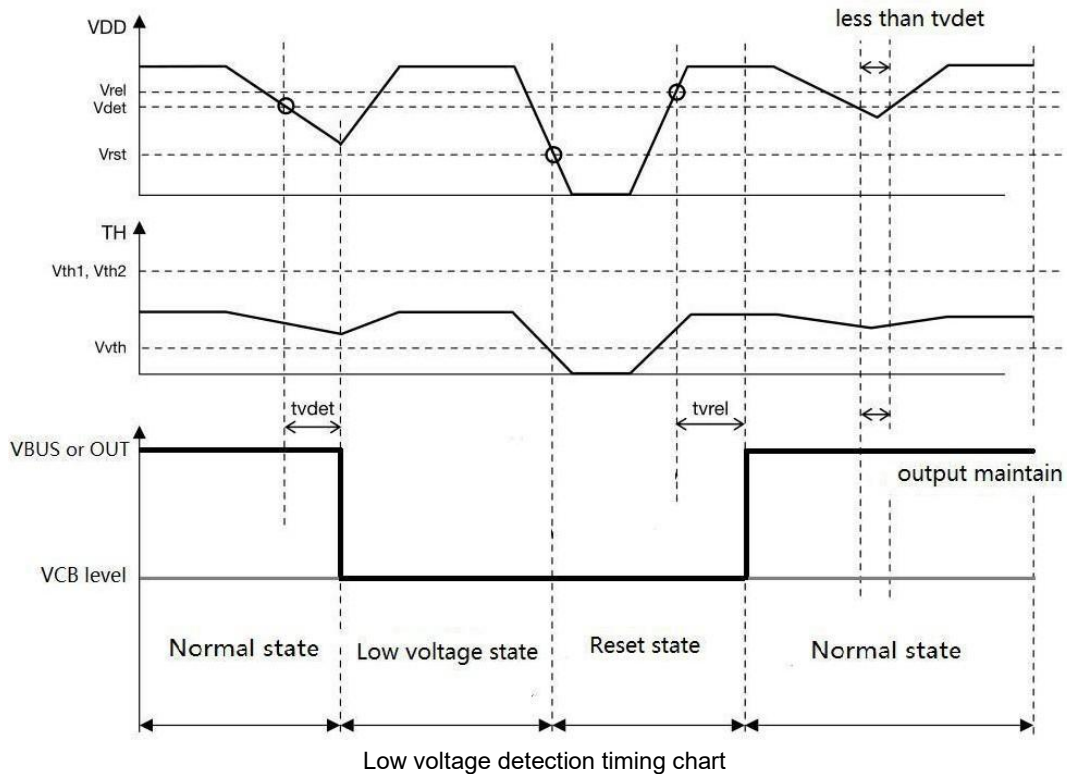
Temperature detection timing chart



< Abnormal temperature detection >

When TH voltage exceeds Vth1 or Vth2 and keeps Tvth, the chip determines that the temperature exceeds the set threshold. The internal NMOS switch would be shut off to pull down VBUS power supply to protect charging equipment. After the over-temperature protection is started, if the temperature drops below the threshold again, that is, when the TH voltage is lower than Vth1 or Vth2, NMOS will not be turned on. After resetting the chip (VDD is lower than Vrst or Vcc>0.44× VDD), the chip can enter normal mode.

TH voltage is greater than the threshold voltage Vth (0.833*VDD) and TH voltage is less than Vth_open, and the chip's response is consistent

Low voltage detection timing chart


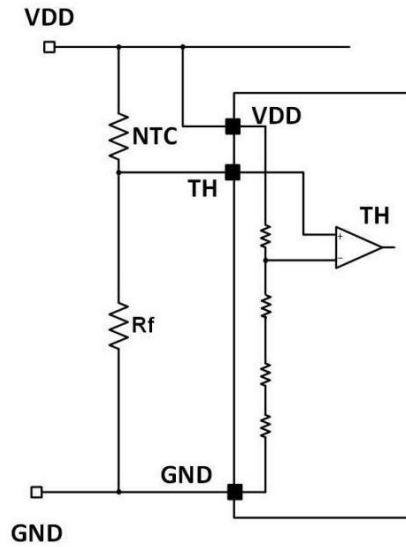
When VDD voltage is lower than Vdet but not lower than Vrst and tvdet is maintained, the chip will determine that the work is low voltage. The internal NMOS switch would be shut off to pull down VBUS power supply to protect charging equipment. After the low voltage protection is started, NMOS will not open if the VDD voltage is higher than Vdet again. After resetting the chip (VDD is lower than Vrst or $V_{cc} > 0.44 \times VDD$), the chip can enter normal mode.

Device end plugging detection identification

When the voltage of CC is higher than $0.44 \times VDD$, the chip immediately enters the reset state. The internal NMOS switch would be shut off to pull down VBUS power supply. Connect CC to GND to bypass device end plugging detection.

When this feature is not used, CC should be connected to GND.

Temperature threshold setting



TH voltage: Typical $0.833 \times VDD$;

Max. $0.844 \times VDD$;

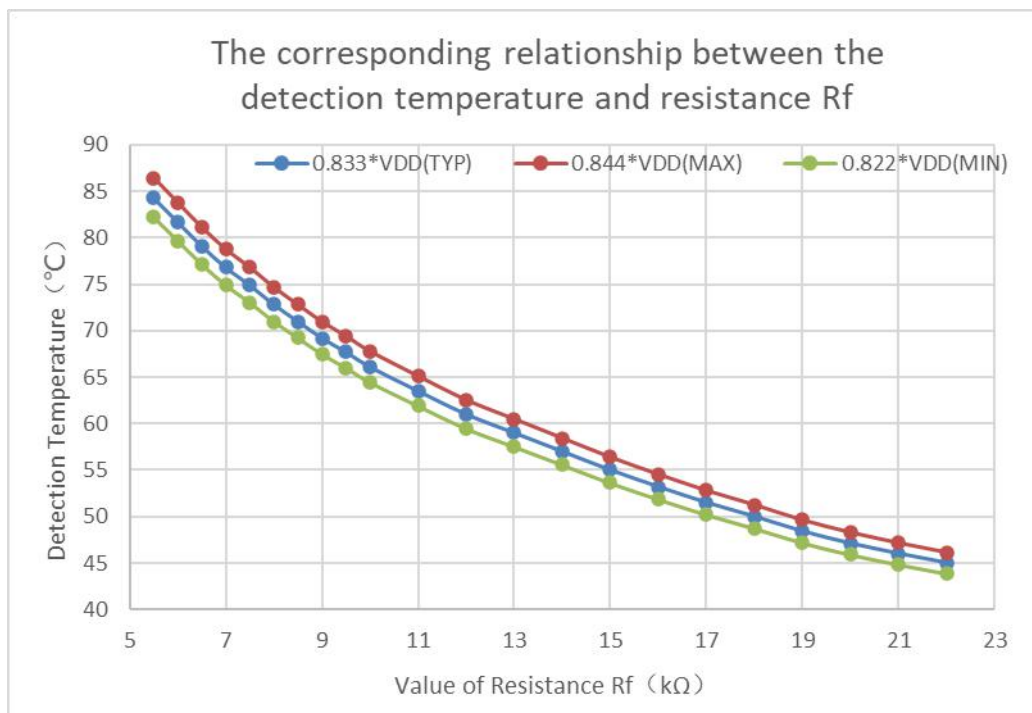
Min. $0.822 \times VDD$;

Reference:

NTC thermistor : NCP21XV103J03RA (Murata Manufacturing Co., Ltd.) $R=10K \pm 1\%$

Reference value: B constant number (25°C-80°C)=3930

t_1 (Detection temperature)=75°C, t_0 (Reference temperature)=25°C



Temperature setting formula

temperature threshold:

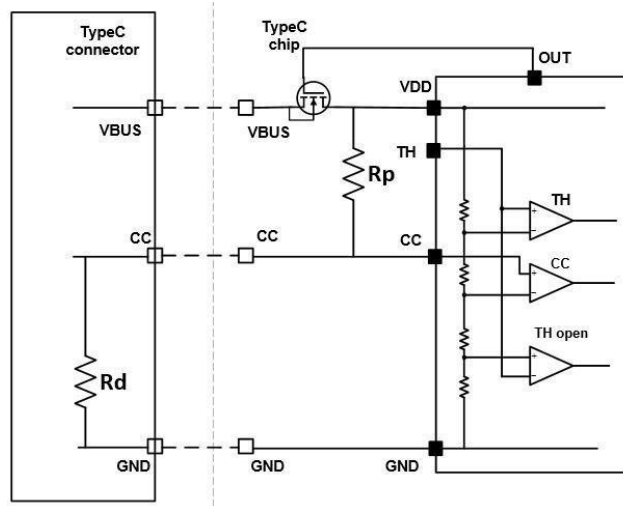
$$= \frac{1}{\frac{\ln(R_f * (1 - 0.833)/(0.833 * R))}{B} + (1/(273.15 + 25))} - 273.15$$

in here:

R_f is the feedback resistance value in series with NTC resistance, R is the resistance value of thermistor at 25 degrees Celsius, and B is a constant of NTC resistance.

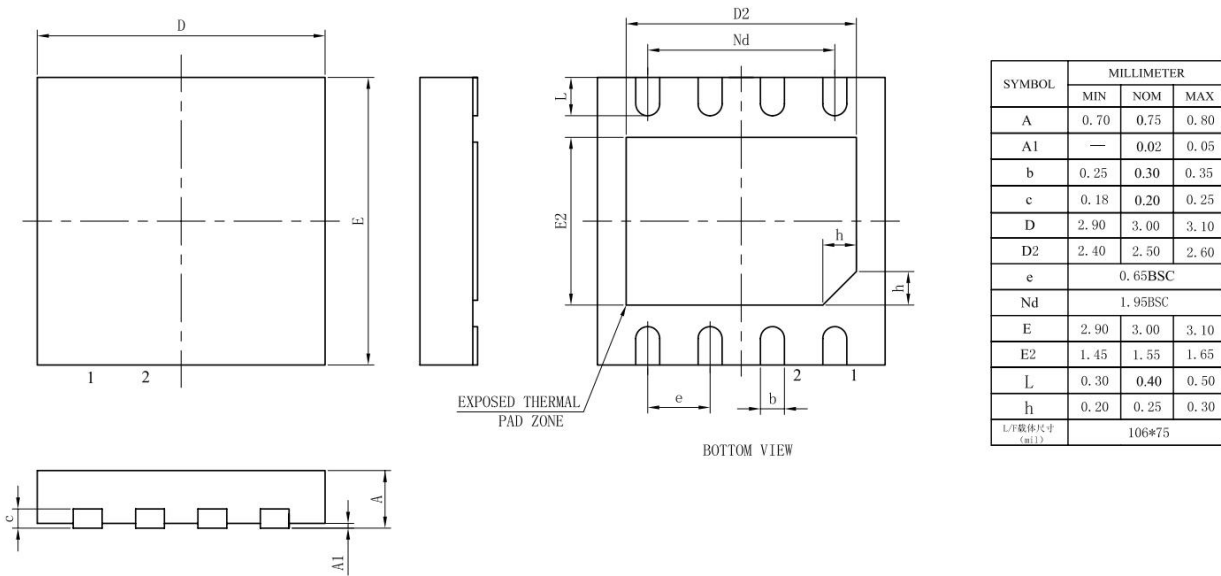
According to the above formula, the set temperature threshold can be calculated according to the feedback resistance value (R_f), or the required feedback resistance can be calculated according to the set temperature threshold.

Device end plugging detection



When the type-C interface is unplugged, CC voltage is pulled up to VDD by R_p, the chip would be reset. The internal NMOS switch would be shut off to pull down VBUS power supply to protect charging equipment. When the type-C interface is plugged in, CC voltage is pulled down by R_d below 0.44×VDD, the chip would enter normal mode after T_{vrel}.

Package Information



Ordering Information

Part Number	Package	Packing Quantity	Marking
WP1682	DFN8-3mm*3mm	3k/Reel	WP1682 XXXX

Contact Information

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For additional information, please contact your local Sales Representative.

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Specifications are subject to change without notice.

The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time

Users should verify actual device performance in their specific applications.

单击下面可查看定价，库存，交付和生命周期等信息

[>>WAY-ON\(维安\)](#)