BT169G

SCR

5 September 2018 **Product data sheet**

1. General description

Planar passivated Silicon Controlled Rectifier with sensitive gate in a SOT54 (TO-92) plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic ICs and other low power gate trigger circuits.

2. Features and benefits

- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate

3. Applications

- Ignition circuits
- Lighting ballasts
- Protection circuits
- Switched Mode Power Supplies

4. Quick reference data

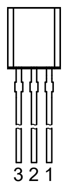
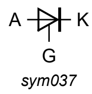
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq$ 83 °C; Fig. 1		-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq$ 83 °C; Fig. 2; Fig. 3		-	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	8	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	-	9	A
T_j	junction temperature			-	-	125	°C
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 7		-	50	200	µA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		500	800	-	V/µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{DM} = 402 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		-	25	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 TO-92 (SOT54)	
2	G	gate		
3	K	cathode		

6. Ordering information

Table 3. Ordering information

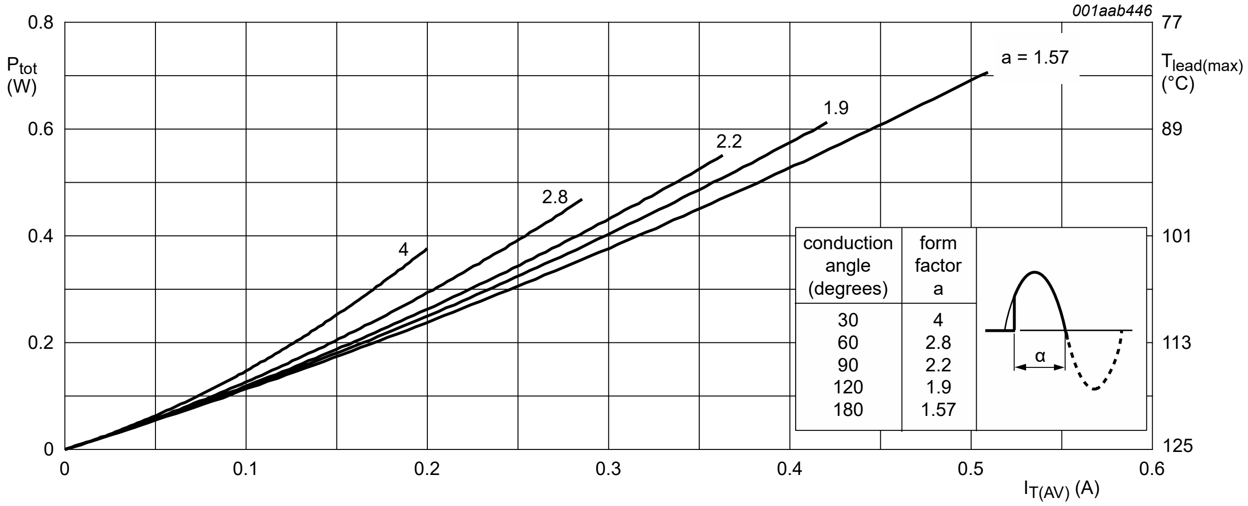
Type number	Package		
	Name	Description	Version
BT169G	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

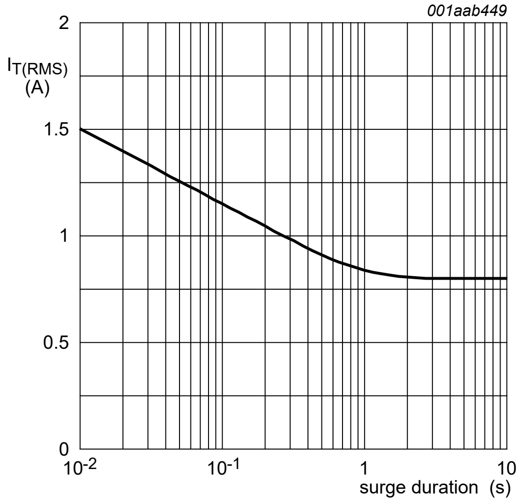
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	600	V
V_{RRM}	repetitive peak reverse voltage			-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq$ 83 °C; Fig. 1		-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq$ 83 °C; Fig. 2; Fig. 3		-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	8	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	9	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		-	0.32	A²s
dI_T/dt	rate of rise of on-state current	I_T = 2 A; I_G = 10 mA; dI_G/dt = 100 mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	1	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C



α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz; T_{lead} = 83 °C

Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents

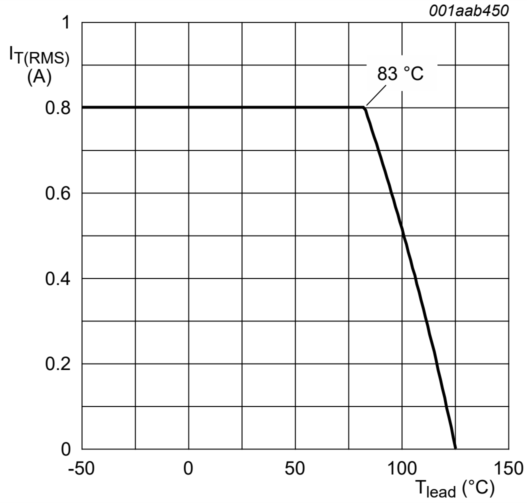
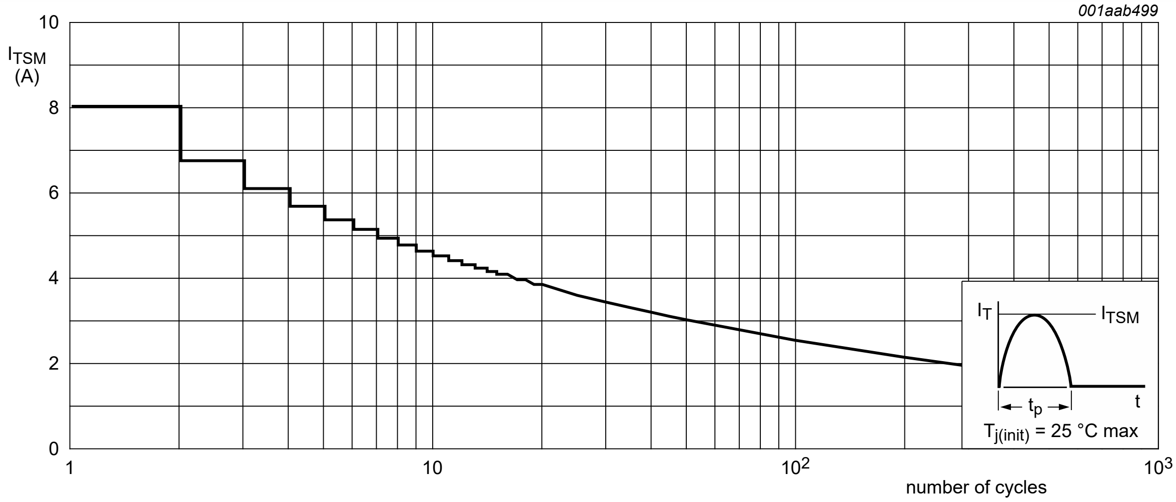
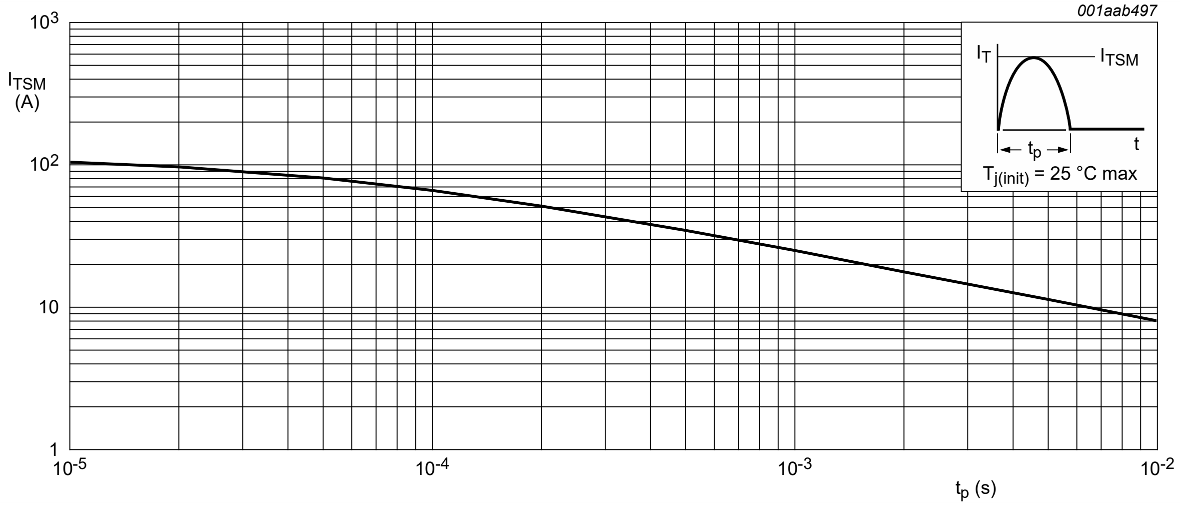


Fig. 3. RMS on-state current as a function of lead temperature; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	Fig. 6		-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm		-	150	-	K/W

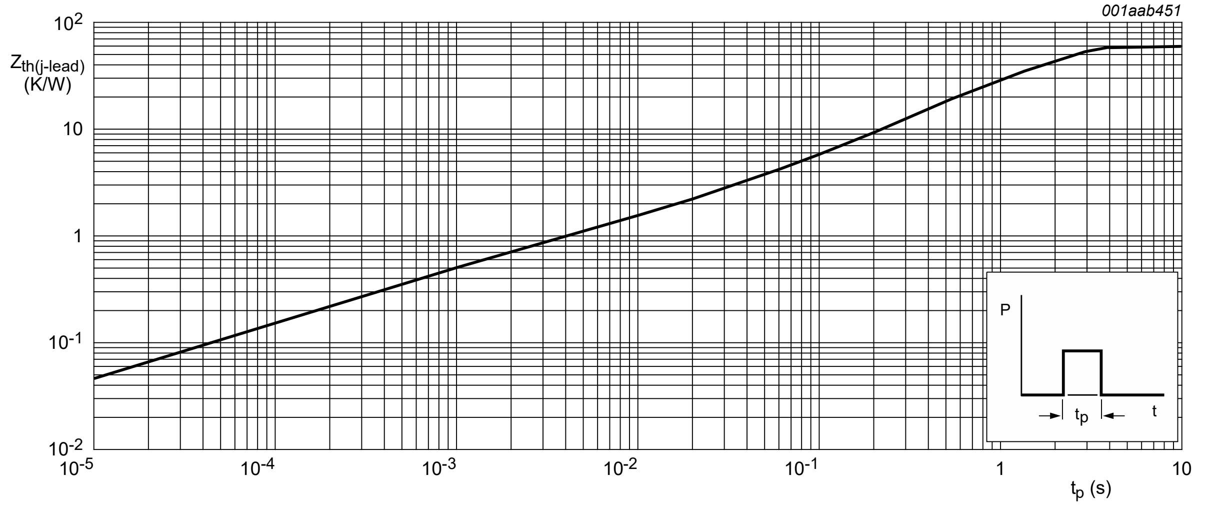


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 7		-	50	200	μA
I_L	latching current	V_D = 12 V; I_G = 0.5 mA; T_j = 25 °C; Fig. 8		-	2	6	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	2	5	mA
V_T	on-state voltage	I_T = 1.2 A; T_j = 25 °C; Fig. 10		-	1.25	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 11		-	0.5	0.8	V
		V_D = 600 V; I_T = 10 mA; T_j = 125 °C; Fig. 11		0.2	0.3	-	V
I_D	off-state current	V_D = 600 V; $R_{GK(ext)}$ = 1 kΩ; T_j = 125 °C		-	0.05	0.1	mA
I_R	reverse current	V_R = 600 V; T_j = 125 °C; $R_{GK(ext)}$ = 1 kΩ		-	0.05	0.1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		500	800	-	V/μs
		V_{DM} = 402 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		-	25	-	V/μs
t_{gt}	gate-controlled turn-on time	I_{TM} = 2 A; V_D = 600 V; I_G = 10 mA; dI_G/dt = 0.1 A/μs; T_j = 25 °C		-	2	-	μs
t_q	commutated turn-off time	V_{DM} = 402 V; T_j = 125 °C; I_{TM} = 1.6 A; V_R = 35 V; $(dI_T/dt)_M$ = 30 A/μs; dV_D/dt = 2 V/μs; $R_{GK(ext)}$ = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	μs

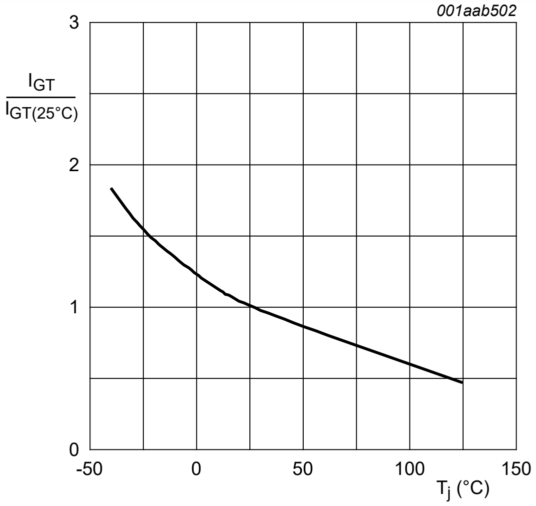
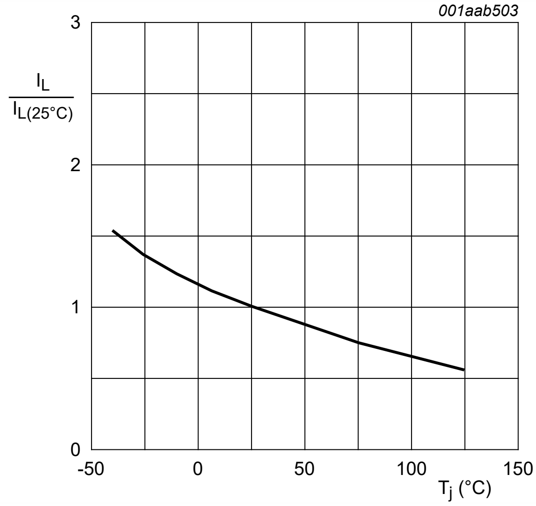
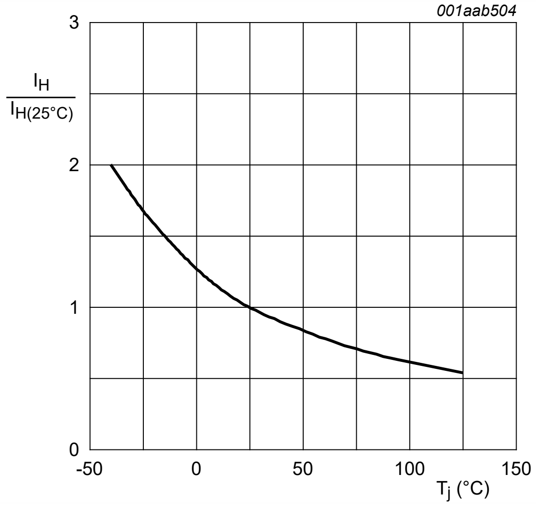


Fig. 7. Normalized gate trigger current as a function of junction temperature



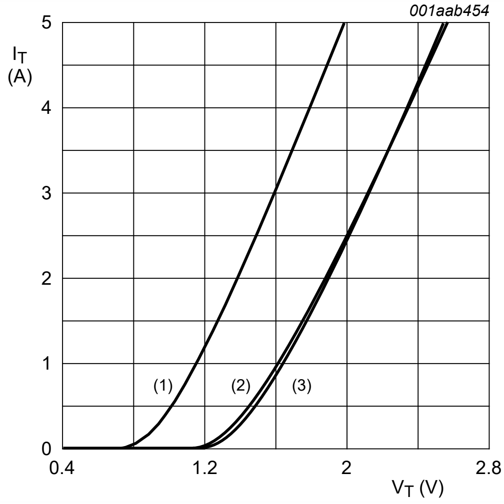
R_{GK} = 1 kΩ

Fig. 8. Normalized latching current as a function of junction temperature



R_{GK} = 1 kΩ

Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.067 V; R_s = 0.187 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

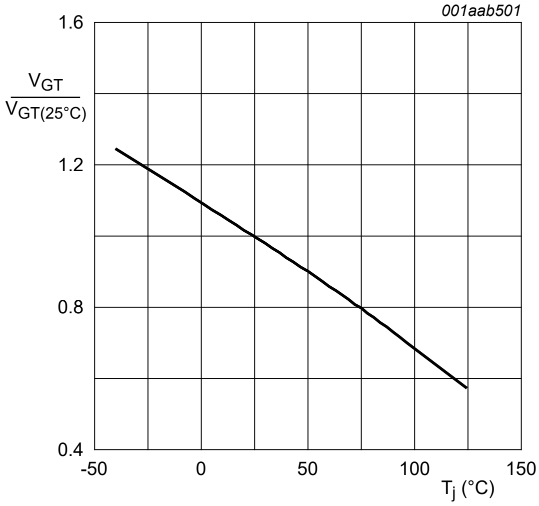
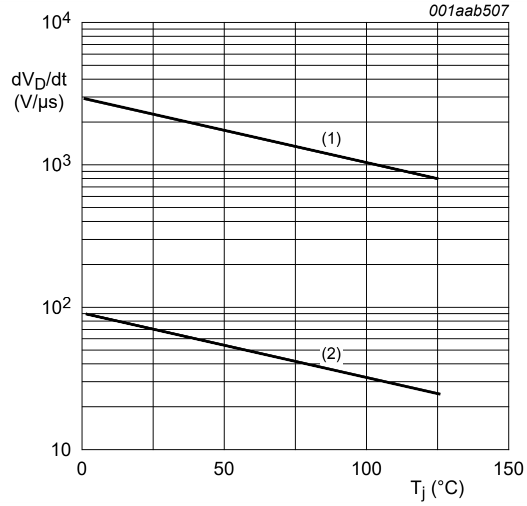


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



(1) R_{GK} = 1 kΩ

(2) gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

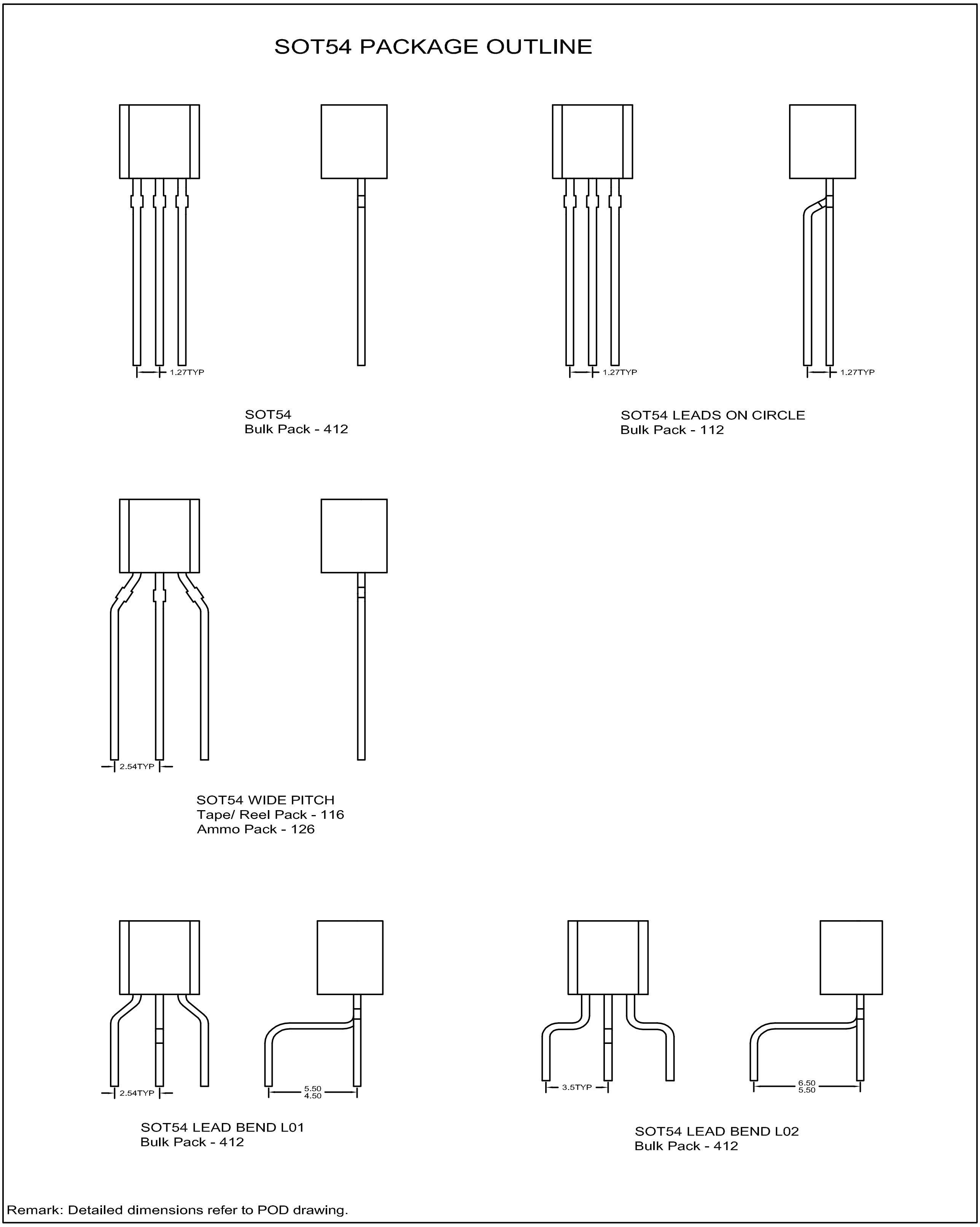


Fig. 13. Package outline TO-92 (SOT54)

11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 5 September 2018

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