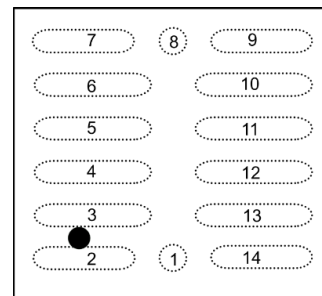


WNMD2196
Dual N-Channel, 12V, 19A, Power MOSFET
<https://www.omnivision-group.com>

V _{SSS} (V)	Max R _{SS(on)} (mΩ)
12	1.5@ V _{GS} =4.5V
	1.7@ V _{GS} =3.8V
	2.6@ V _{GS} =3.1V
	4.0@ V _{GS} =2.5V
ESD Rating:2000V HBM	



Gate1 (FET1) = 1

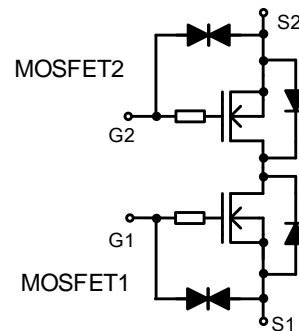
Source1 (FET1) = 2,3,4,5,6,7

Gate2 (FET2) = 8

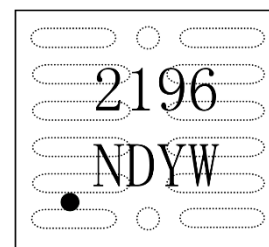
Source2 (FET2) = 9,10,11,12,13,14

CSP-14L (Top view)
Descriptions

The WNMD2196 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent R_{SS(ON)} with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2196 is available in CSP-14L package. Standard Product WNMD2196 is Pb-free and Halogen-free.


Pin Configuration
Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Common-drain type
- Small package CSP-14L



2196 = Device Code

ND = Special Code

Y = Year

W = Week

Marking
Applications

- Lithium-Ion battery protection circuit

Order information

Device	Package	Shipping
WNMD2196-14/TR	CSP-14L	3000/Reel&Tape

Absolute Maximum ratings

Parameter	Symbol	Maximum	Unit	
Source-Source Voltage	V_{SS}	12	V	
Gate-Source Voltage	V_{GS}	± 8		
Continuous Source Current	$T_A=25^\circ\text{C}$	I_S^a	19	A
		I_S^b	48	
Pulsed Source Current ^c	I_{SM}	189		
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D^a	0.57	W
		P_D^b	3.62	
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$	
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ\text{C}$	

Thermal resistance ratings

Single Operation				
Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}^a$	146	219	$^\circ\text{C/W}$
	$R_{\theta JA}^b$	30	35	

Note:

- FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) minimum pad covered with copper.
- Ceramic substrate (70 mm X 70 mm X t1.0 mm, 70um Copper) fully covered with copper.
- Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J=25^\circ\text{C}$, the maximum allowed junction temperature of 150°C .
- The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

Electronics Characteristics (T_A=25°C, unless otherwise noted)

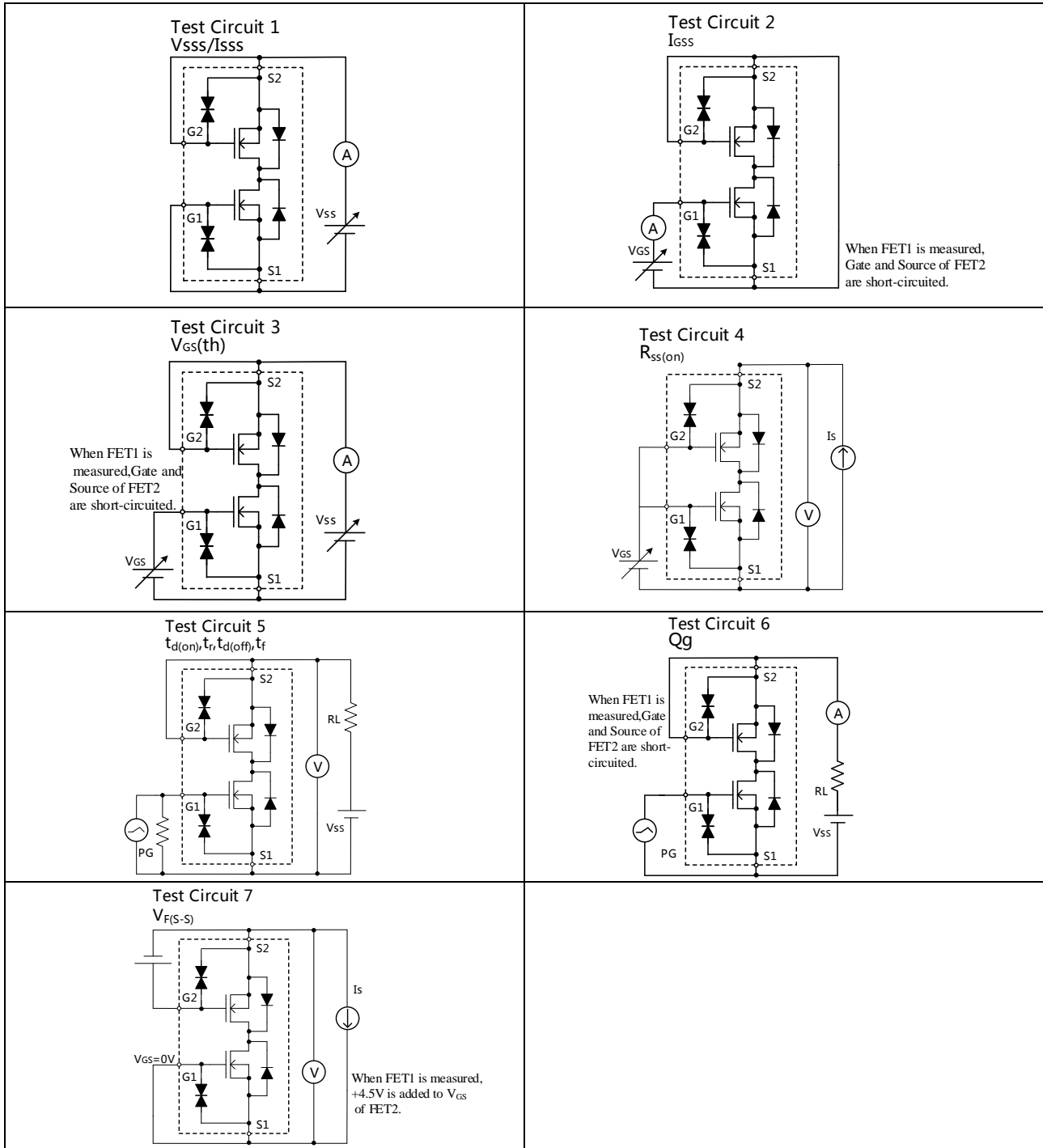
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Source to Source Voltage	V _{SSS}	V _{GS} = 0 V, I _S = 1mA	12			V
Zero Gate Voltage Drain Current	I _{SSS}	V _{SS} = 10 V, V _{GS} = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I _{GSS}	V _{SS} = 0 V, V _{GS} = ±8V TEST CIRCUIT 2			±10	uA
		V _{SS} = 0 V, V _{GS} = ±5V TEST CIRCUIT 2			±1	uA
ON CHARACTERISTICS						
Gate to Source Cut-off Voltage	V _{GS(th)}	V _{SS} = 10 V, I _S = 1mA TEST CIRCUIT 3	0.5	0.9	1.4	V
Source to Source On-state Resistance	R _{SS(on)}	V _{GS} = 4.5V, I _S = 9.8A TEST CIRCUIT 4	0.7	1.1	1.5	mΩ
		V _{GS} = 3.8V, I _S = 9.8A TEST CIRCUIT 4	0.75	1.2	1.7	
		V _{GS} = 3.1V, I _S = 9.8A TEST CIRCUIT 4	0.8	1.45	2.6	
		V _{GS} = 2.5V, I _S = 9.8A TEST CIRCUIT 4	0.9	1.95	4.0	
BODY DIODE CHARACTERISTICS						
Body Diode Forward Voltage	V _{F(S-S)}	V _{GS} = 0 V, I _F = 9.8A TEST CIRCUIT 7		0.7	1.2	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time*	td(ON)	V _{GS} = 4.0V, V _{SS} = 6.0V, I _S = 9.8A, TEST CIRCUIT 5		1.5		us
Rise Time*	tr			4.0		
Turn-Off Delay Time*	td(OFF)			6.5		
Fall Time*	tf			6.7		
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance*	C _{ISS}	V _{GS} = 0 V, f = 1kHz, V _{SS} = 10 V		5989		pF
Output Capacitance*	C _{OSS}			1200		
Reverse Transfer Capacitance*	C _{RSS}			927		
Total Gate Charge*	Q _{G(TOT)}	V _{G1S1} = 4.0 V, V _{SS} = 6.0V, I _S = 9.8A TEST CIRCUIT 6		62		nC
Threshold Gate Charge*	Q _{G(TH)}			6		
Gate-to-Source Charge*	Q _{GS}			14		
Gate-to-Drain Charge*	Q _{GD}			21		

Note:

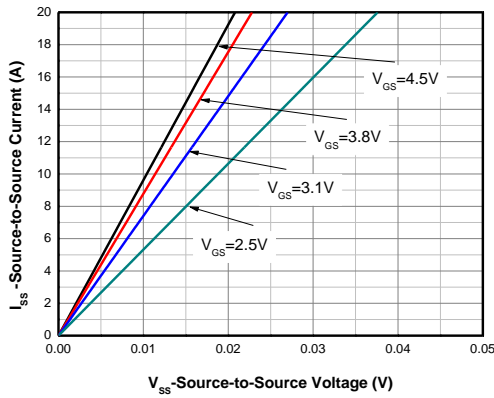
* Guaranteed by design, not subject to production testing

Test Circuit

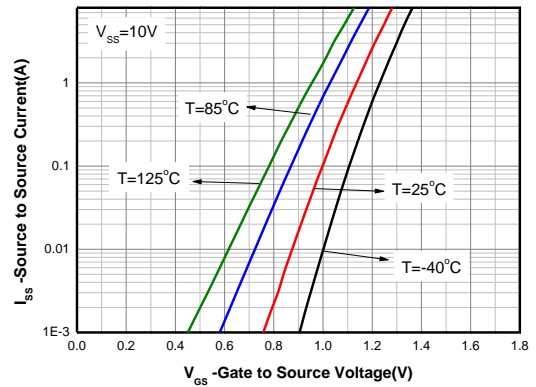
FET1 and the FET2 are both measured. Test circuits are example of measuring the FET1 side



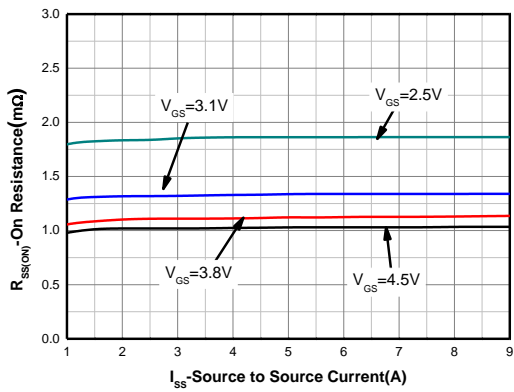
Typical Characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)



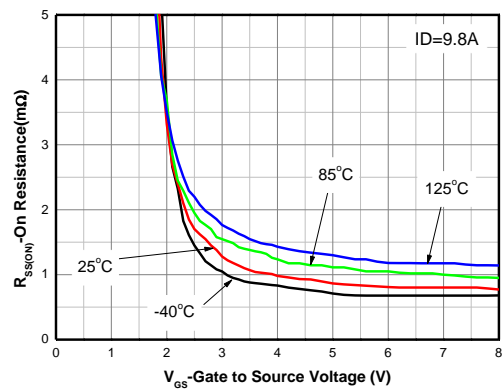
Output Characteristics ^d



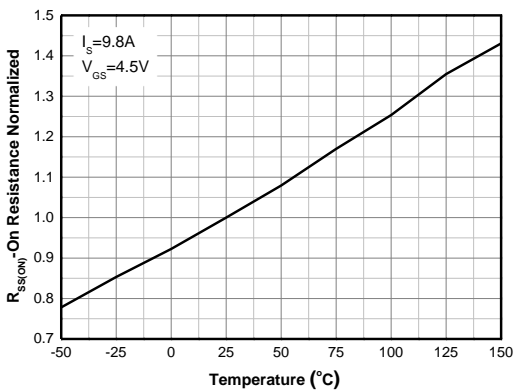
Transfer Characteristics ^d



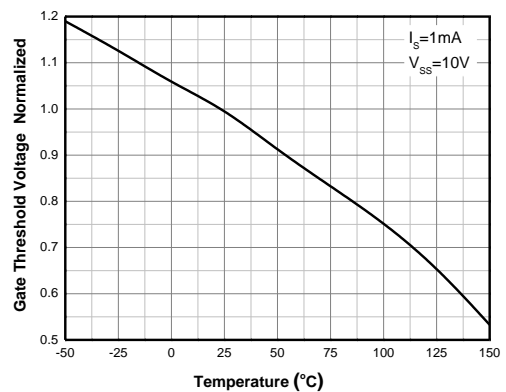
On-Resistance vs. Source Current ^d



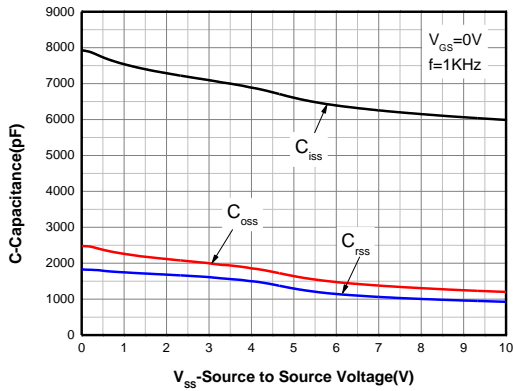
On-Resistance vs. Gate-to-Source Voltage ^d



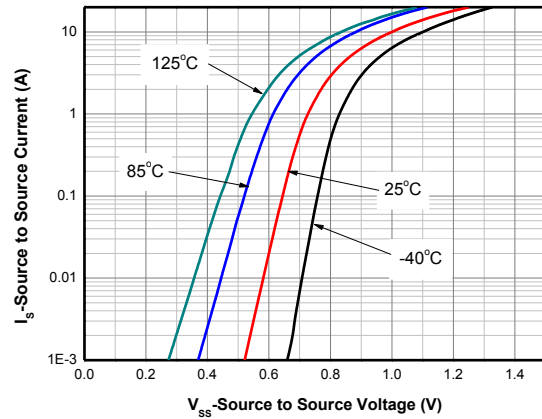
On-Resistance vs. Junction Temperature ^d



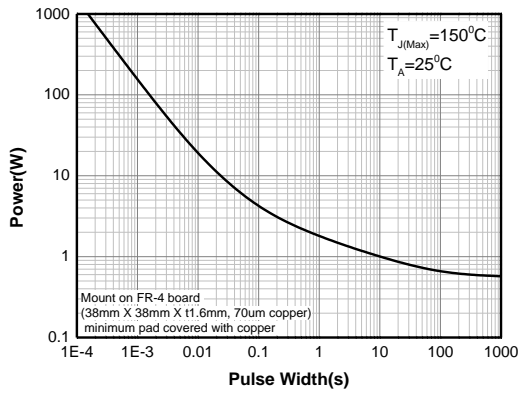
Threshold Voltage vs. Temperature



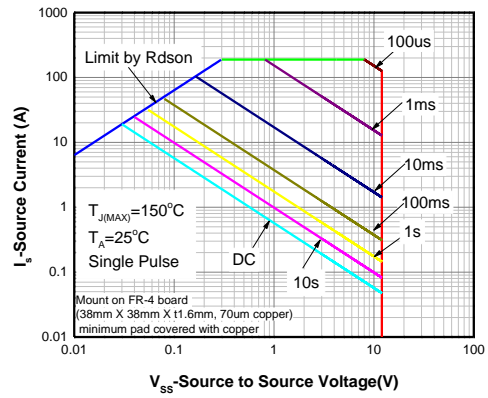
Capacitance



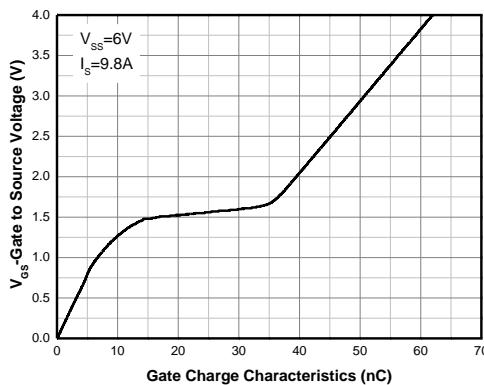
Body Diode Forward Voltage^d



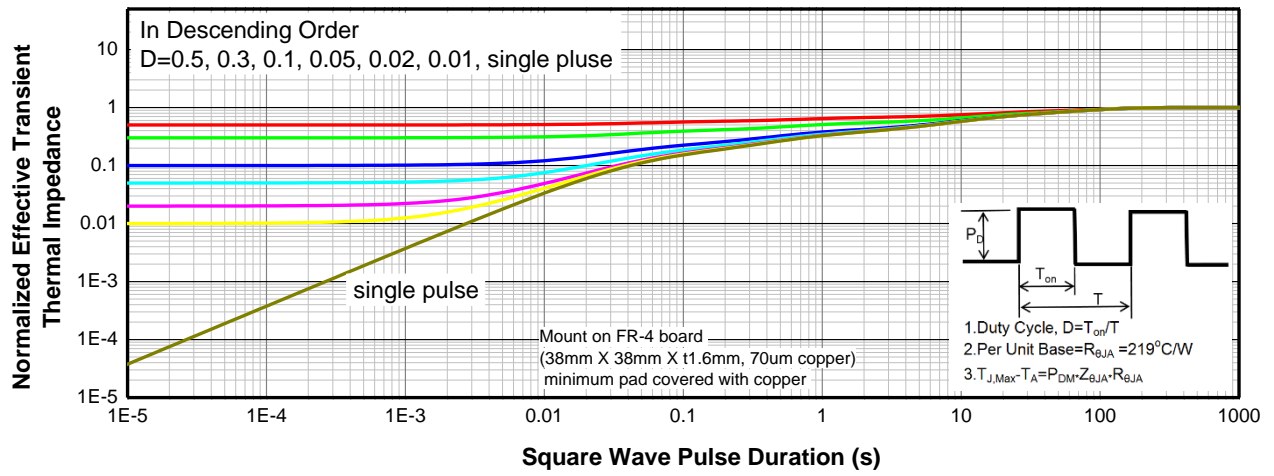
Single Pulse power



Safe Operating Power



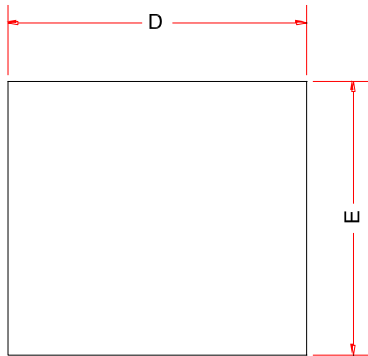
Gate Charge Characteristics



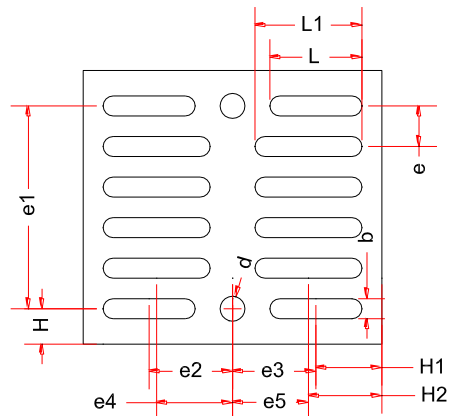
Transient thermal response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

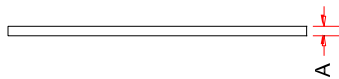
CSP-14L



TOP VIEW



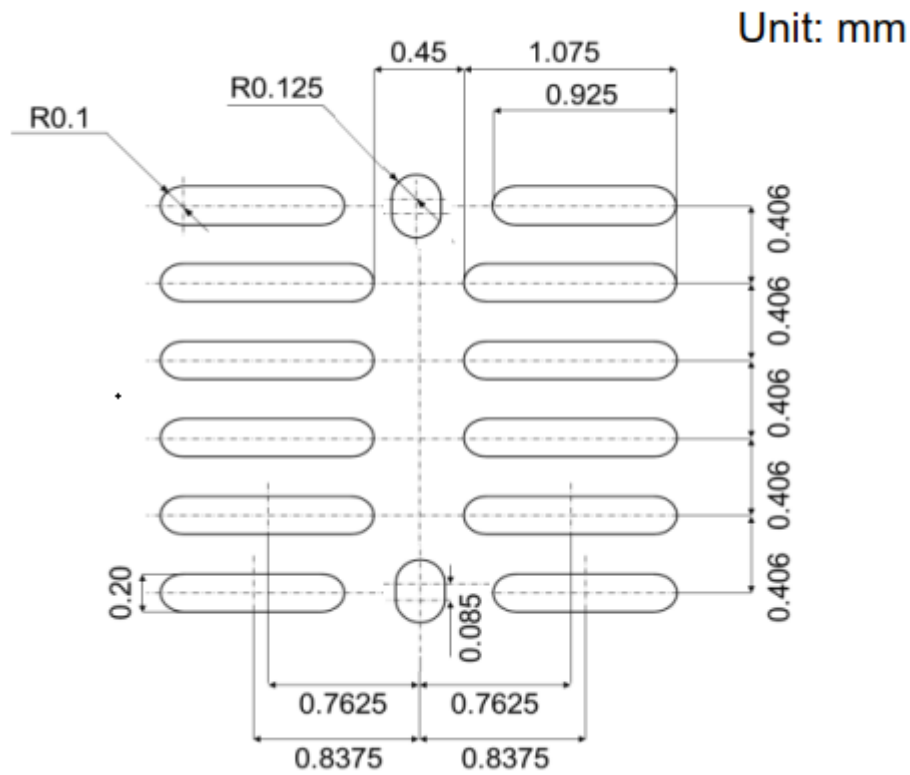
BOTTOM VIEW



SIDE VIEW

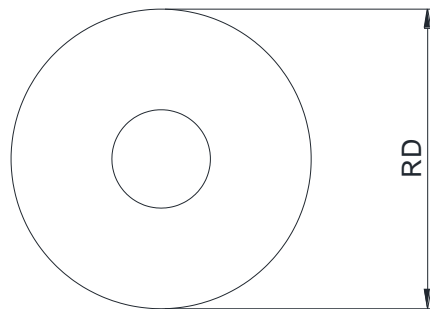
Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.075	0.095	0.125
D	2.96	3.00	3.04
E	2.70	2.74	2.78
b	0.17	0.2	0.23
d	0.25		
e	0.406		
e 1	2.03		
e 2	0.8375		
e 3	0.8375		
e 4	0.7625		
e 5	0.7625		
L	0.922	0.925	0.928
L1	1.072	1.075	1.078
H	0.355		
H1	0.6625		
H2	0.7375		

RECOMMENDED LAND PATTERN (Unit: mm)

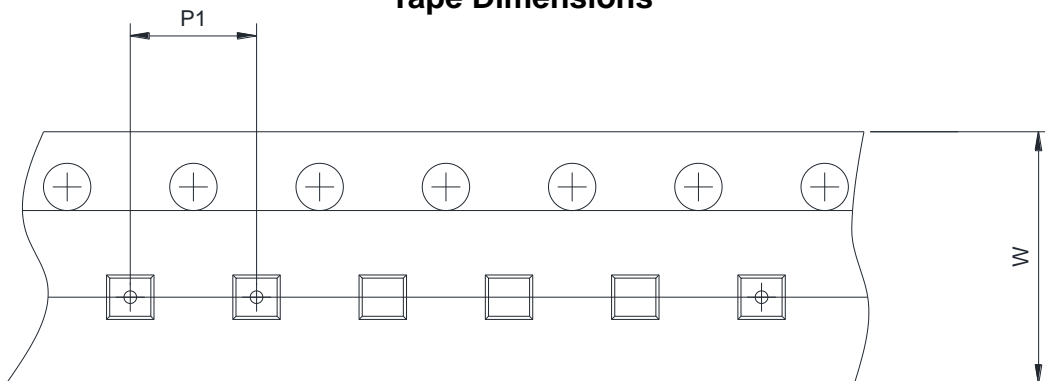


TAPE AND REEL INFORMATION

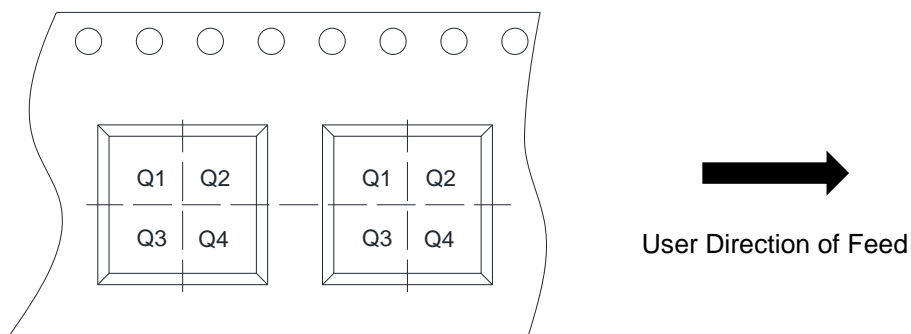
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch <input type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm <input type="checkbox"/> 12mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm <input checked="" type="checkbox"/> 4mm <input type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input type="checkbox"/> Q1 <input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input checked="" type="checkbox"/> Q4

单击下面可查看定价，库存，交付和生命周期等信息

[>>Willsemi\(韦尔半导体\)](#)