

### General Description

The WSF3012 is the highest performance trench N-ch and P-ch MOSFET with extreme high cell density, which provide excellent R<sub>DS(on)</sub> and gate charge for most of the synchronous buck converter applications. The WSF3012 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

### Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

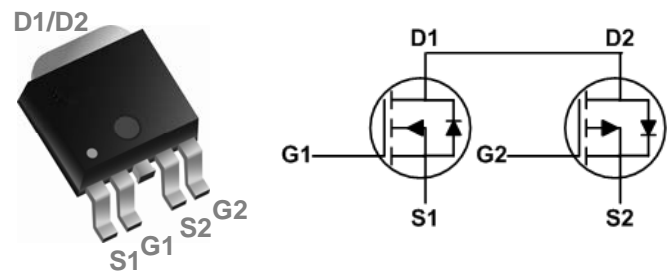
### Product Summary

BVDSS	R <sub>DS(on)</sub>	I <sub>D</sub>
30V	18mΩ	22A
-30V	30mΩ	-15A

### Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- CCFL Back-light Inverter

### TO-252-4L Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V <sub>DS</sub>	Drain-Source Voltage	30	-30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	23	-15	A
I <sub>D</sub> @T <sub>C</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	13.1	-9.6	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	55	-49	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	28	66	mJ
I <sub>AS</sub>	Avalanche Current	17.8	-27.2	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	32.5	32.5	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	---	5	°C/W

**N-Channel Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.033	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =12A	---	13	18	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	16	21	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.5	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	-4.52	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =8A	---	6.4	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	2.6	5.2	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =8A	---	7.4	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	2.3	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	3	---	
T <sub>d(on)</sub>	Turn-On Delay Time		---	3.8	---	
T <sub>r</sub>	Rise Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =8A	---	10	---	ns
T <sub>d(off)</sub>	Turn-Off Delay Time		---	22	---	
T <sub>f</sub>	Fall Time		---	6.6	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	620	---	pF
C <sub>oss</sub>	Output Capacitance		---	85	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	60	---	

**Guaranteed Avalanche Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy <sup>5</sup>	V <sub>DD</sub> =25V, L=0.1mH, I <sub>AS</sub> =10A	25	---	---	mJ

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,6</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	21	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,6</sup>		---	---	42	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.1	V

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=17.8A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

**P-Channel Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.011	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-7A	---	24	29	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	---	35	46	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.2	-1.6	-2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	4.31	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-6A	---	10	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	14	16	Ω
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-20V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-12A	---	8	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	3.3	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	2.3	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-1A	---	4.6	---	ns
T <sub>r</sub>	Rise Time		---	14	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	34	---	
T <sub>f</sub>	Fall Time		---	18	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	757	---	pF
C <sub>oss</sub>	Output Capacitance		---	122	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	88	---	

**Guaranteed Avalanche Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy <sup>5</sup>	V <sub>DD</sub> =-25V, L=0.1mH, I <sub>AS</sub> =-15A	20	---	---	mJ

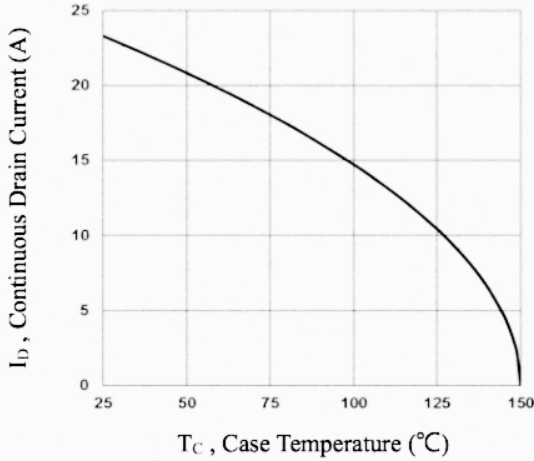
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,6</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-15	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,6</sup>		---	---	-35	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1	V

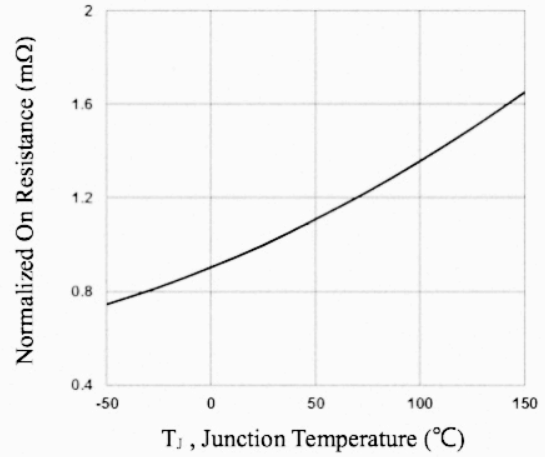
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=-25V, V<sub>GS</sub>=-10V, L=0.1mH, I<sub>AS</sub>=-27.2A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

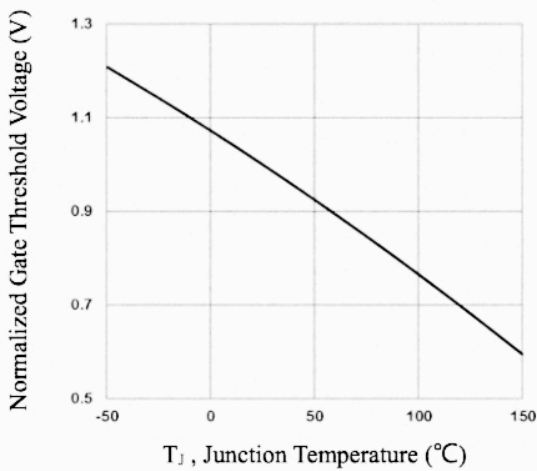
**N-Channel Typical Characteristics**



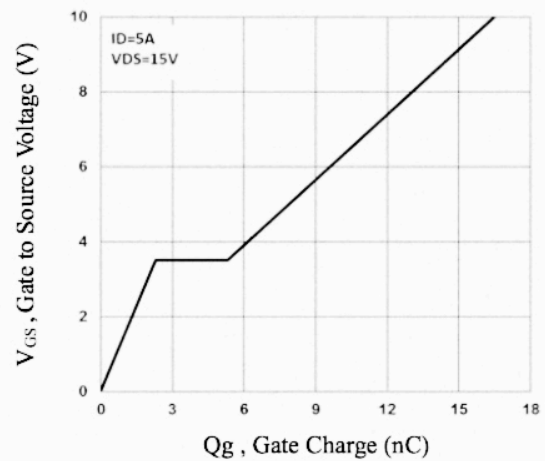
**Fig.1 Continuous Drain Current vs.  $T_c$**



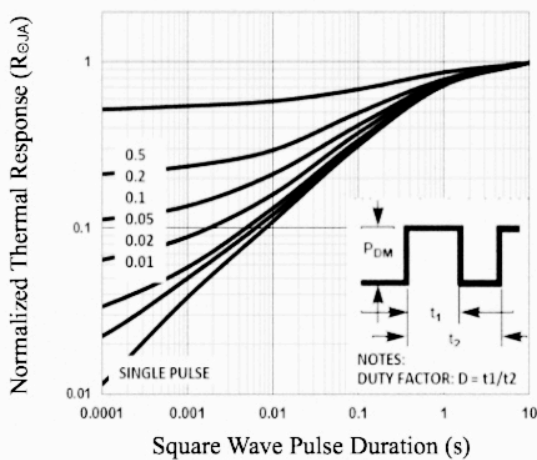
**Fig.2 Normalized  $R_{DS(on)}$  vs.  $T_j$**



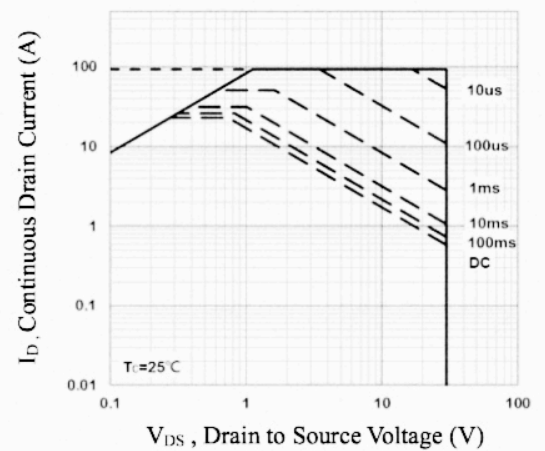
**Fig.3 Normalized  $V_{th}$  vs.  $T_j$**



**Fig.4 Gate Charge Waveform**

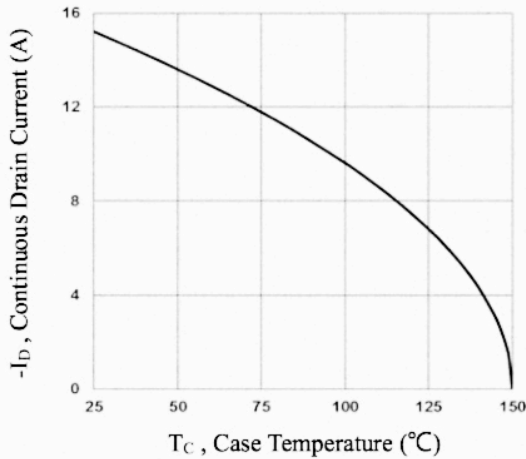


**Fig.5 Normalized Transient Response**

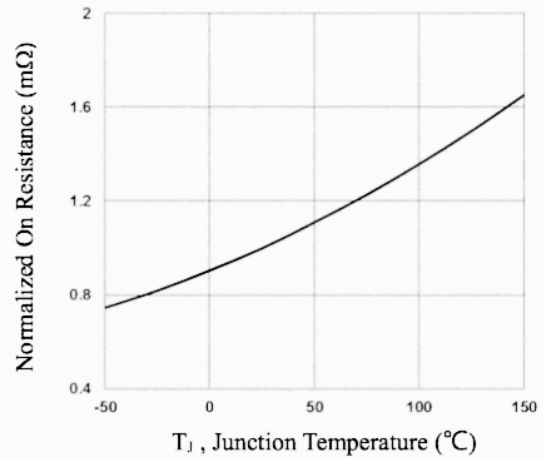


**Fig.6 Maximum Safe Operation Area**

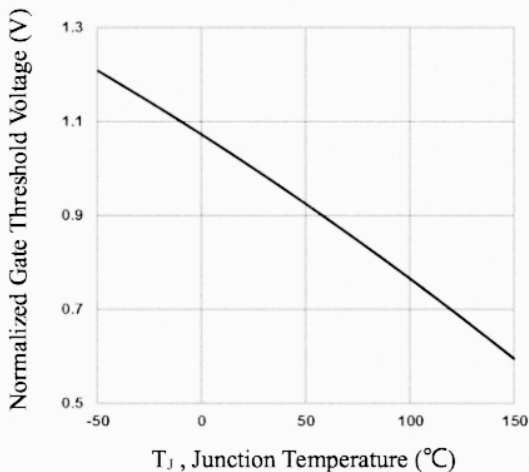
**P-Channel Typical Characteristics**



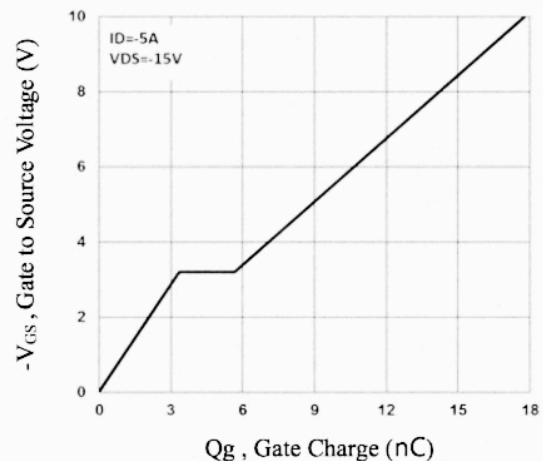
**Fig.1 Continuous Drain Current vs. T<sub>c</sub>**



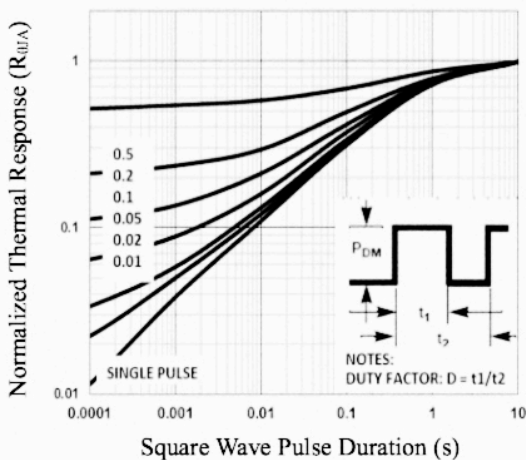
**Fig.2 Normalized RDSON vs. T<sub>j</sub>**



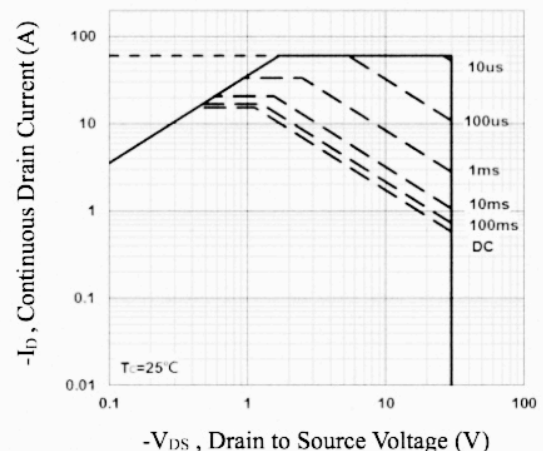
**Fig.3 Normalized V<sub>th</sub> vs. T<sub>j</sub>**



**Fig.4 Gate Charge Waveform**



**Fig.5 Normalized Transient Impedance**



**Fig.6 Maximum Safe Operation Area**

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