

**N-Ch MOSFET** 

## **General Description**

The WST3052 is the highest performance trench N-Ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WST3052 meet the RoHS and Green Product requirement with full function reliability approved.

#### **Features**

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

## **Product Summery**

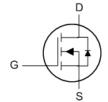
BVDSS	RDSON	ID
30V	60mΩ	2.5A

# **Applications**

 Power Management in Notebook Computer Portable Equipment and Battery Powered Systems.

# **SOT-323 Pin Configuration**





### **Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units	
$V_{DS}$	Drain-Source Voltage	30	V	
$V_{GS}$	Gate-Source Voltage	±12	V	
I <sub>D</sub> @T <sub>c</sub> =25℃	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	2.5	А	
I <sub>D</sub> @T <sub>c</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	2.0	Α	
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	13	А	
P <sub>D</sub> @T <sub>A</sub> =25℃	Total Power Dissipation <sup>3</sup>	0.7	W	
P <sub>D</sub> @T <sub>A</sub> =70°C	Total Power Dissipation <sup>3</sup>	0.45	W	
T <sub>STG</sub>	Storage Temperature Range -55 to 150		$^{\circ}$	
TJ	Operating Junction Temperature Range	-55 to 150	℃	

# **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit
$R_{ heta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>		180	°C/W
$R_{ heta JA}$	Thermal Resistance Junction-Ambient ¹ (t ≤10s)		120	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case <sup>1</sup>		100	°C/W



# Electrical Characteristics (T<sub>J</sub>=25 C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	30			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.025		V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =2.5A		50	60	mΩ
		V <sub>GS</sub> =2.5V , I <sub>D</sub> =2A		60	70	
$V_{GS(th)}$	Gate Threshold Voltage	-\/\/	0.5	0.7	1.0	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	$-V_{GS}=V_{DS}$ , $I_D=250uA$		-4.8		mV/℃
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	uA
		$V_{DS}$ =24V , $V_{GS}$ =0V , $T_J$ =55 $^{\circ}$ C			30	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}$ = $\pm 20V$ , $V_{DS}$ = $0V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =2A		7		S
$R_g$	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2.5	5	Ω
Qg	Total Gate Charge (4.5V)	V <sub>DS</sub> =10V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =1A		4.0	8.4	
$Q_gs$	Gate-Source Charge			0.3	3.5	nC
$Q_gd$	Gate-Drain Charge			1.5	2.9	
T <sub>d(on)</sub>	Turn-On Delay Time			3.5	5.2	
T <sub>r</sub>	Rise Time	$V_{DD}$ =10V , $V_{GS}$ =10V , $R_{G}$ =6 $\Omega$ ,		13.3	21	1
T <sub>d(off)</sub>	Turn-Off Delay Time	$I_D=1A$ , $R_L=10\Omega$ .		13.2	20	ns
T <sub>f</sub>	Fall Time			2	5	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =10V , V <sub>GS</sub> =0V , f=1MHz		286		
Coss	Output Capacitance			60		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			50		

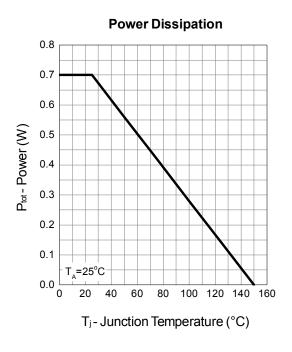
## **Diode Characteristics**

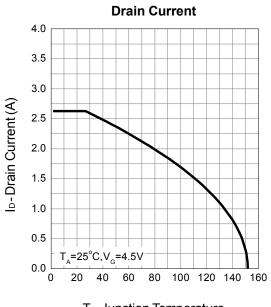
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current <sup>1,4</sup>	V =V =0V Force Current			2.5	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,4</sup>	$V_G=V_D=0V$ , Force Current			13	Α
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25℃			1.0	V
t <sub>rr</sub>	Reverse Recovery Time			15		nS
Q <sub>rr</sub>	Reverse Recovery Charge	lF=5A,dl/dt=100A/µs,T <sub>J</sub> =25℃		3.7		nC

#### Note

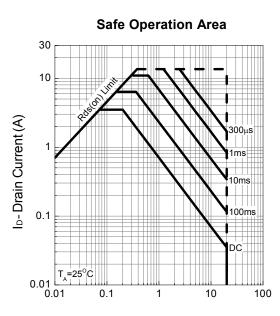
- 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, t<10 sec.
- 2.The data tested by pulsed , pulse width  $\leq 300 \text{us}$  , duty cycle  $\leq 2\%$
- 3. The power dissipation is limited by 150 ℃ junction temperature
- 4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



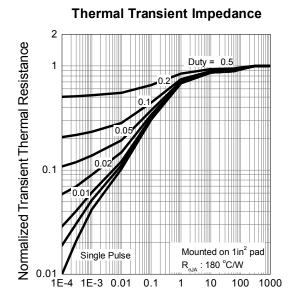




T<sub>j</sub> - Junction Temperature



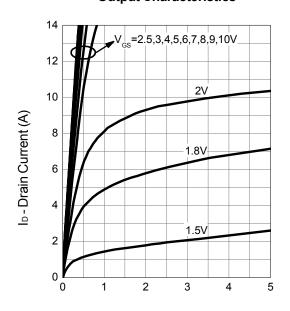
V<sub>DS</sub> - Drain - Source Voltage (V)



Square Wave Pulse Duration (sec)

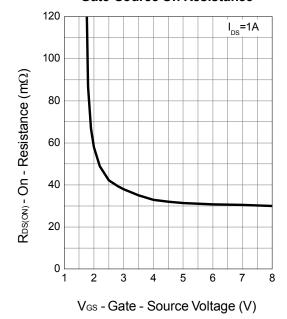


# **Output Characteristics**

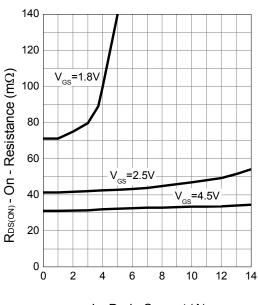


V<sub>DS</sub>-Drain - Source Voltage (V)

#### **Gate-Source On Resistance**

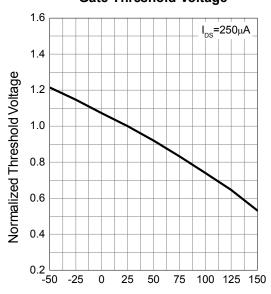


### **Drain-Source On Resistance**



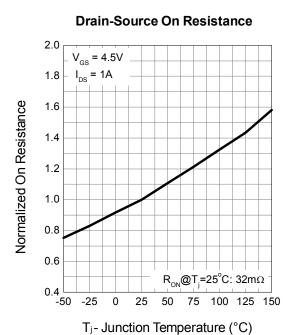
ID-Drain Current (A)

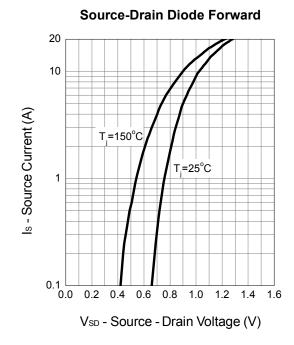
# **Gate Threshold Voltage**

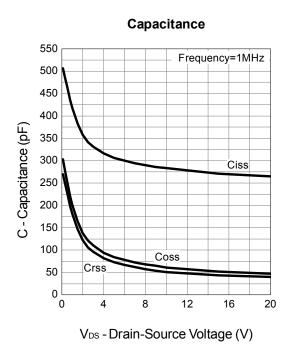


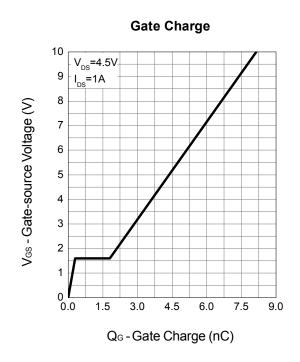
T<sub>j</sub> - Junction Temperature (°C)





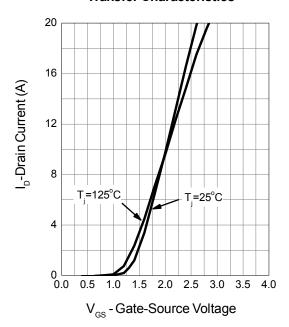








#### **Transfer Characteristics**





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