



#### **General Description**

The WST30P06 is the highest performance trench P-ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WST30P06 meet the RoHS and Green Prod uct requirement with full function reliability approved.

#### **Features**

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

#### **Product Summery**

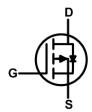
BVDSS	RDSON	ID
-60V	88mΩ	-3.5A

## **Applications**

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

## **SOT-23-3L Pin Configuration**





#### **Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units	
$V_{DS}$	Drain-Source Voltage	-60	V	
$V_{GS}$	Gate-Source Voltage	±20	V	
I <sub>D</sub> @T <sub>C</sub> =25℃	Continuous Drain Current, -V <sub>GS</sub> @ -10V <sup>1</sup>	-3.5	Α	
I <sub>D</sub> @T <sub>C</sub> =100℃	Continuous Drain Current, -V <sub>GS</sub> @ -10V <sup>1</sup>	-2.8	Α	
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	-20	Α	
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>3</sup>	1.0	W	
T <sub>STG</sub>	Storage Temperature Range -55 to 150		$^{\circ}$	
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	℃	

# **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit
$R_{ heta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>		125	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case <sup>1</sup>		80	°C/W



**P-Channel MOSFET** 

## Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-60			V
$\triangle BV_{DSS}/\triangle T_{J}$	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =-1mA		-0.021		V/℃
В	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-2A		88	110	- mΩ
R <sub>DS(ON)</sub>		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-1A		110	150	
$V_{GS(th)}$	Gate Threshold Voltage	V V I 050 A	-1.0	-1.5	-3.0	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	$V_{GS}=V_{DS}$ , $I_D=-250uA$		4.08		mV/℃
l	$\begin{array}{c c} I_{DSS} & Drain-Source \ Leakage \ Current \end{array} \qquad \begin{array}{c} V_{DS}\text{=-}48V \ , \ V_{GS}\text{=-}0V \ , \ T_J\text{=-}25 ^{\circ}\text{C}} \\ \hline V_{DS}\text{=-}48V \ , \ V_{GS}\text{=-}0V \ , \ T_J\text{=-}55 ^{\circ}\text{C}} \end{array}$			1	uA	
IDSS		$V_{DS}$ =-48V , $V_{GS}$ =0V , $T_J$ =55 $^{\circ}\mathrm{C}$			5	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}$ = $\pm 20 V$ , $V_{DS}$ = $0 V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-10V , I <sub>D</sub> =-6A		5.8		S
Qg	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-20V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-2A		6.3		
$Q_{gs}$	Gate-Source Charge			2.3		nC
$Q_{gd}$	Gate-Drain Charge			1.8		
T <sub>d(on)</sub>	Turn-On Delay Time			20		
Tr	Rise Time	$V_{DD}$ =-15V , $V_{GS}$ =-10V , $R_{G}$ =3.3 $\Omega$ ,		33.1		no
T <sub>d(off)</sub>	Turn-Off Delay Time	I <sub>D</sub> =-1A		34		ns
T <sub>f</sub>	Fall Time			3.8		
C <sub>iss</sub>	Input Capacitance			364		
Coss	Output Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		41		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			12		

## **Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			-3.5	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,4</sup>	VG-VD-UV , FOICE Cullell			-18	Α
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	$V_{GS}$ =0V , $I_{S}$ =-1A , $T_{J}$ =25 $^{\circ}$ C			-1.2	V

- 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper,t<10sec.
- 2.The data tested by pulsed , pulse width  $\leq 300$ us , duty cycle  $\leq 2\%$  3.The power dissipation is limited by 150°C junction temperature
- 4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.





## **Typical Characteristics**

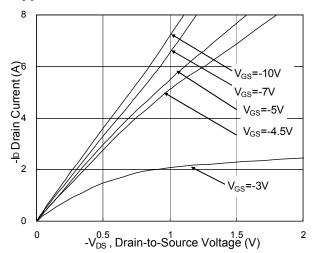


Fig.1 Typical Output Characteristics

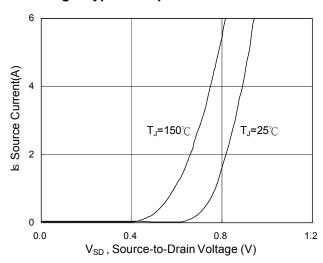


Fig.3 Forward Characteristics Of Reverse

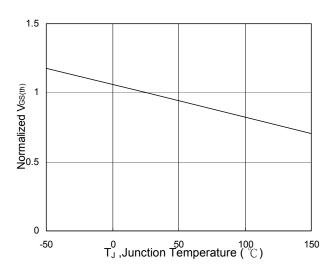


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$ 

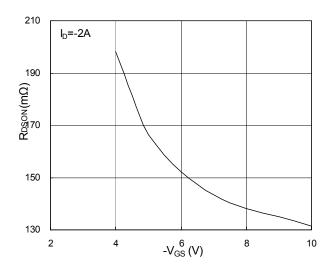


Fig.2 On-Resistance v.s Gate-Source

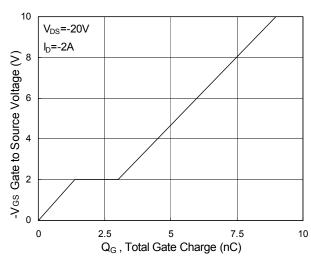


Fig.4 Gate-Charge Characteristics

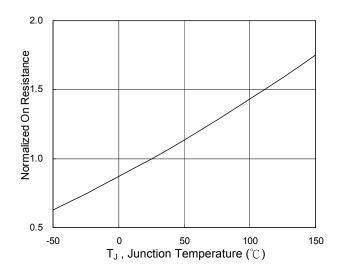
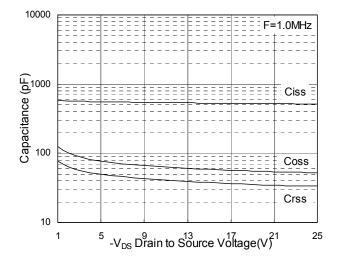


Fig.6 Normalized R<sub>DSON</sub> v.s T<sub>J</sub>







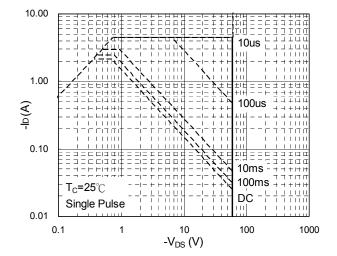


Fig.7 Capacitance

Fig.8 Safe Operating Area

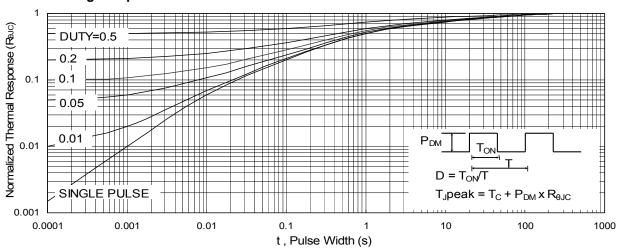
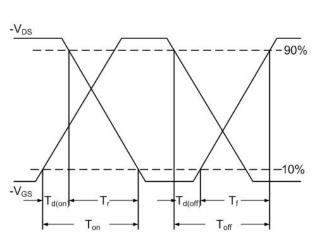
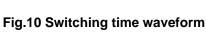


Fig.9 Normalized Maximum Transient Thermal Impedance





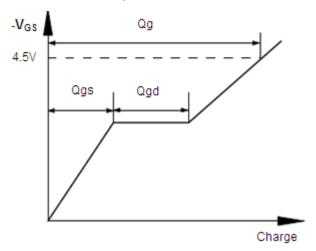


Fig.11 Gate Charge waveform



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