

General Description

The WSD30100DN56 is the highest performance trench N-Ch MOSFET with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The WSD30100DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

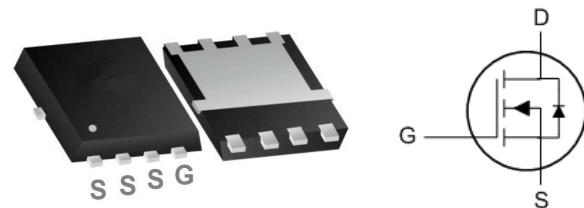
Product Summary

BVDSS	R _{DS(on)}	I _D
30V	3.3mΩ	100A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

DFN5X6-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	100	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	56	A
I _{DM}	Pulsed Drain Current ²	140	A
EAS	Single Pulse Avalanche Energy ³	45	mJ
I _{AS}	Avalanche Current	30	A
P _D @T _C =25°C	Total Power Dissipation ⁴	46.3	W
T _{STG}	Storage Temperature Range	-55 to 175	°C
T _J	Operating Junction Temperature Range	-55 to 175	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	50	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	2.7	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.0213	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	---	3.3	4	mΩ
		V _{GS} =4.5V, I _D =15A	---	4.6	6.2	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.5	1.8	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-5.73	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	---	28	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.0	2.0	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =20A	---	9.2	---	nC
Q _{gs}	Gate-Source Charge		---	6	---	
Q _{gd}	Gate-Drain Charge		---	2	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =12V, V _{GEN} =10V, R _G =2.9Ω, I _D =5.7A, R _L =2.1Ω	---	14.3	---	ns
T _r	Rise Time		---	26	---	
T _{d(off)}	Turn-Off Delay Time		---	24	---	
T _f	Fall Time		---	4.4	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1350	---	pF
C _{oss}	Output Capacitance		---	900	---	
C _{riss}	Reverse Transfer Capacitance		---	65	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =25V, L=0.1mH, I _{AS} =30A	30	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V, Force Current	---	---	20	A
I _{SM}	Pulsed Source Current ^{2,6}		---	---	140	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =20A, T _J =25°C	---	---	1	V

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, t<10sec.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=30A
- The power dissipation is limited by 175°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

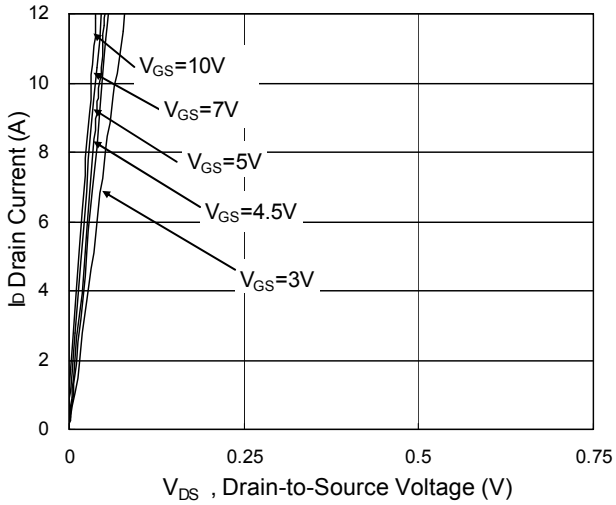


Fig.1 Typical Output Characteristics

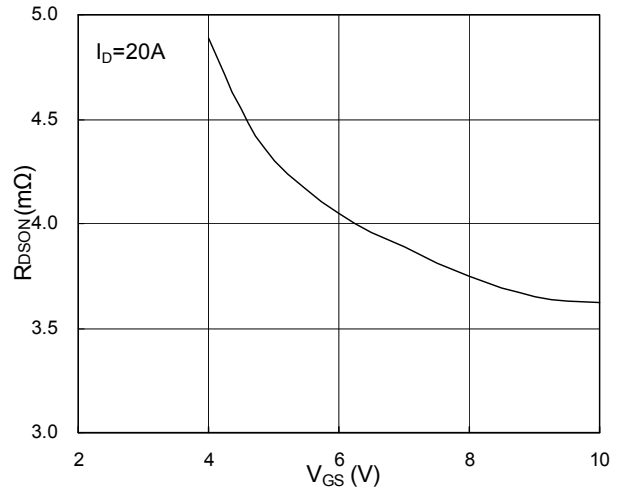


Fig.2 On-Resistance vs. G-S Voltage

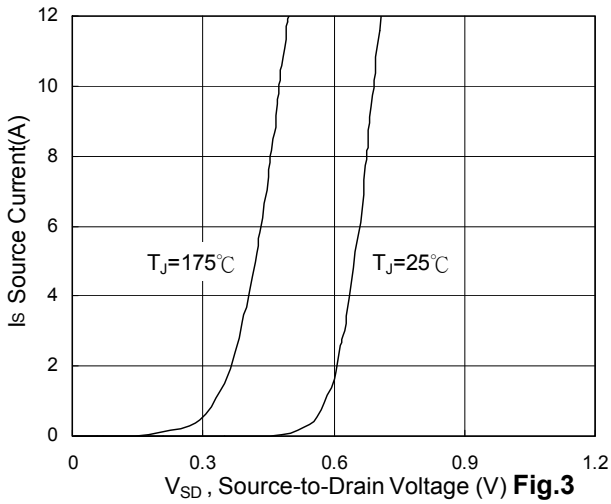


Fig.3

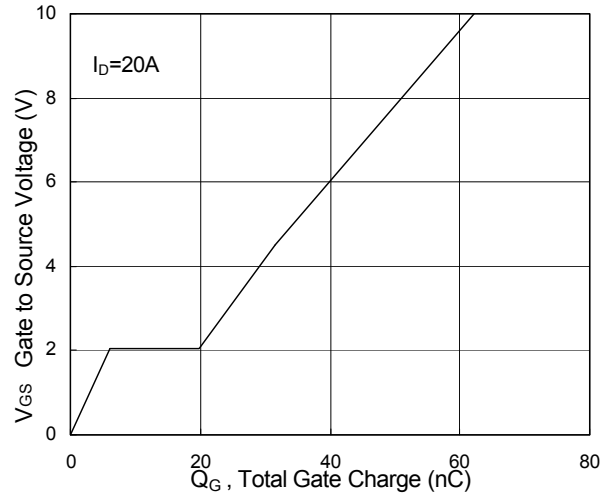


Fig.4 Gate-charge Characteristics

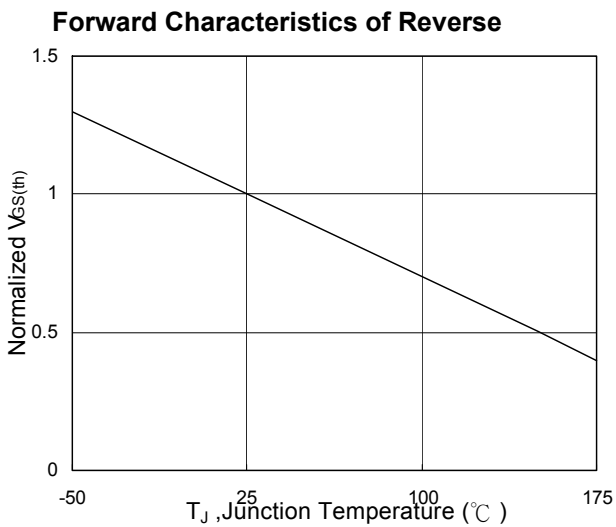


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

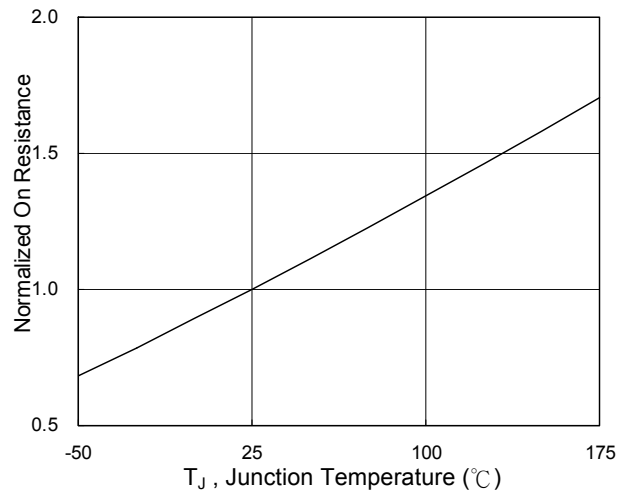


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

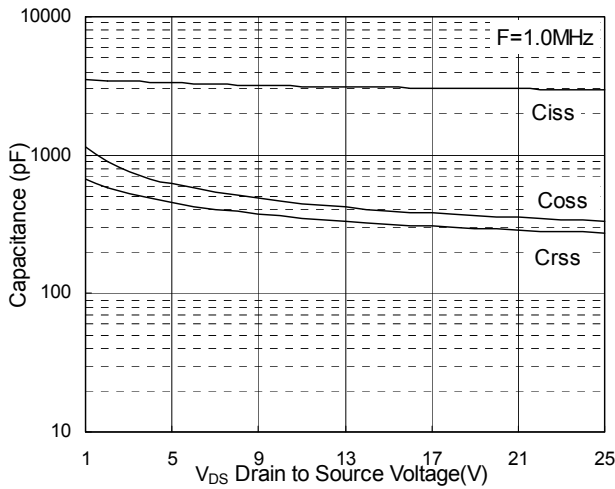


Fig.7 Capacitance

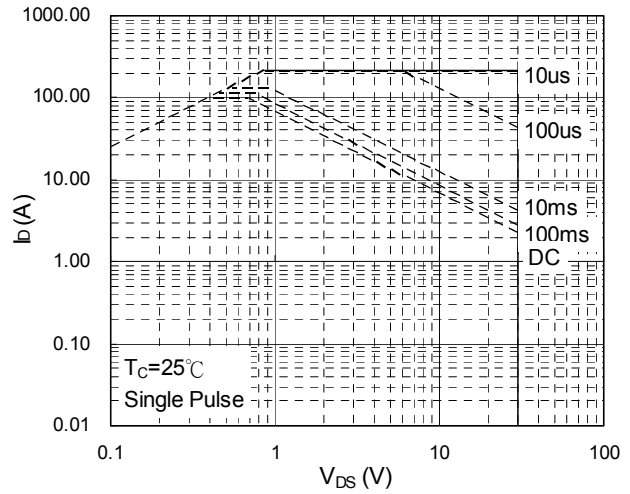


Fig.8 Safe Operating Area

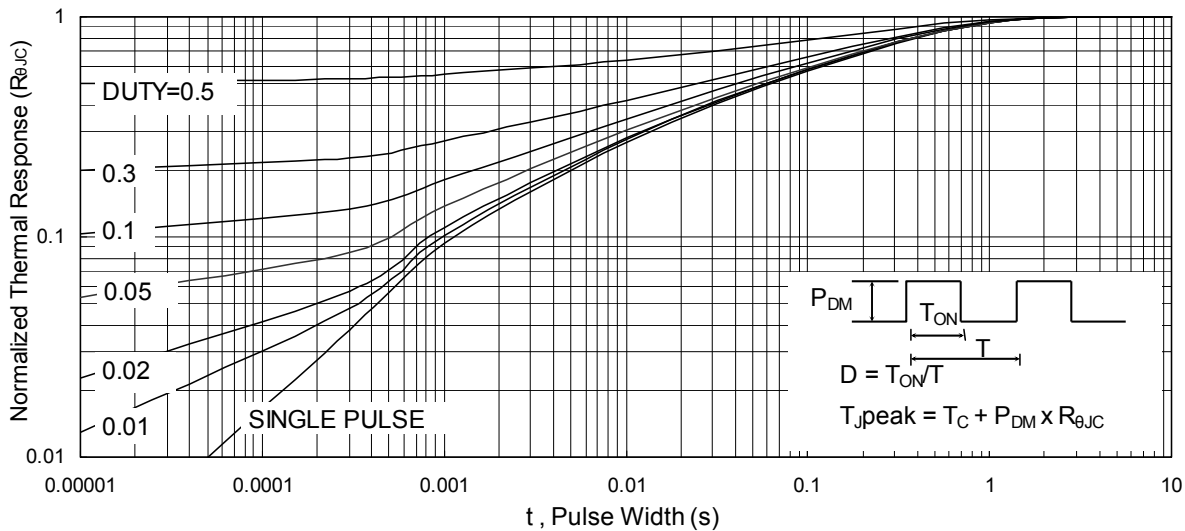


Fig.9 Normalized Maximum Transient Thermal Impedance

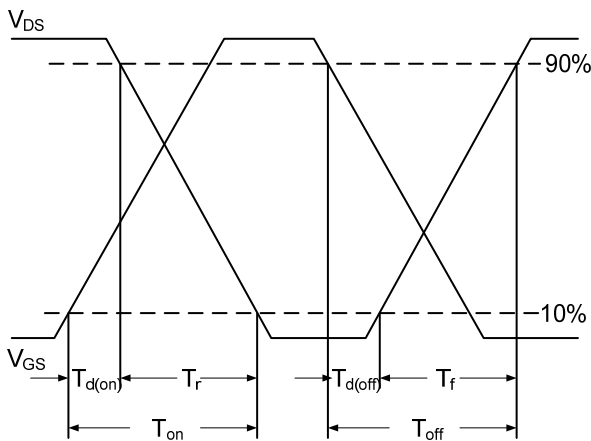


Fig.10 Switching Time Waveform

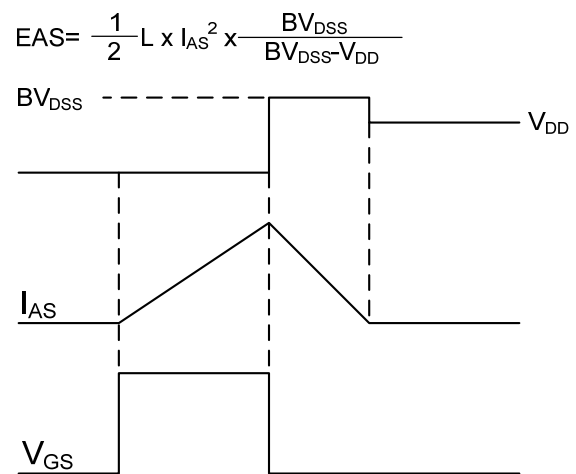


Fig.11 Unclamped Inductive Switching Wave

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