General Description

The WSP10N10 is the highest performance trench N-Ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSF08N10 meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.

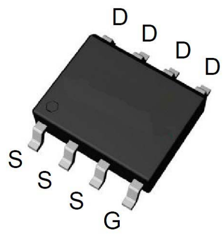
Product Summery

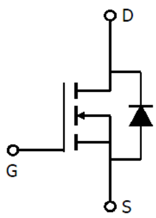
BVDSS	RDSON	ID
100V	22mΩ	10A

Applications

- Power Management in DC/DC Converter.

SOP-8 Pin Configuration





Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	10	A
I_D@T_C=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	8.2	A
I_{DM}	Pulsed Drain Current[2]	60	A
EAS	Single Pulse Avalanche Energy[3]	42	mJ
I_{AS}	Avalanche Current	30	A
P_D@T_A=25℃	Total Power Dissipation[4]	3.1	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{θJA}$	Thermal Resistance Junction-ambient [1]	---	40	℃/W
$R_{θJC}$	Thermal Resistance Junction-Case[1]	---	24	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	100	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.098	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=10A	---	22	28	mΩ
		V_{GS}=4.5V , I_D=6.5A	---	25	31	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, I_D =250uA	1.5	2.0	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.52	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V , V_{GS}=0V , T_J=25℃	---	---	10	uA
		V_{DS}=80V , V_{GS}=0V , T_J=55℃	---	---	100	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	0.65	1.0	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=80V , V_{GS}=10V , I_D=10A	---	28	---	nC
Q_{gs}	Gate-Source Charge		---	9	---	
Q_{gd}	Gate-Drain Charge		---	10	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=30V , V_{GEN}=10V , R_G=6Ω I_D=1A ,R_L=30Ω	---	12	---	ns
T_r	Rise Time		---	4	---	
$T_{d(off)}$	Turn-Off Delay Time		---	17	---	
T_f	Fall Time		---	5	---	
C_{iss}	Input Capacitance	V_{DS}=30V , V_{GS}=0V , f=1MHz	---	1769	---	pF
C_{oss}	Output Capacitance		---	164	---	
C_{rss}	Reverse Transfer Capacitance		---	53	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V , L=0.3mH , I_{AS}=10A	30	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	$V_G=V_D$=0V , Force Current	---	---	5	A
I_{SM}	Pulsed Source Current[2,6]		---	---	30	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=6A , T_J=25℃	---	---	1.1	V
t_{rr}	Reverse Recovery Time	IF=10A , dI/dt=100A/µs , T J=25℃	---	27	---	nS
Q_{rr}	Reverse Recovery Charge		---	28	---	nC

Note :

1.The data tested by surface mounted on a 1 $inch^2$ FR-4 board with 2OZ copper,t<10sec.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.3mH,I_{AS}=10A

4.The power dissipation is limited by 150℃ junction temperature

5.The Min. value is 100% EAS tested guarantee.

6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

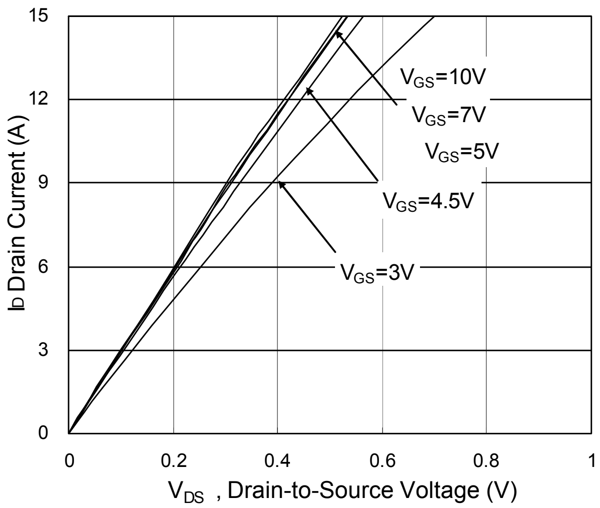


Fig.1 Typical Output Characteristics

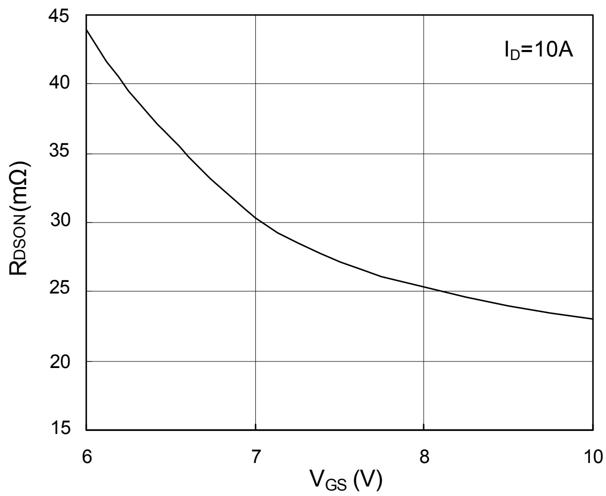


Fig.2 On-Resistance vs. Gate-Source

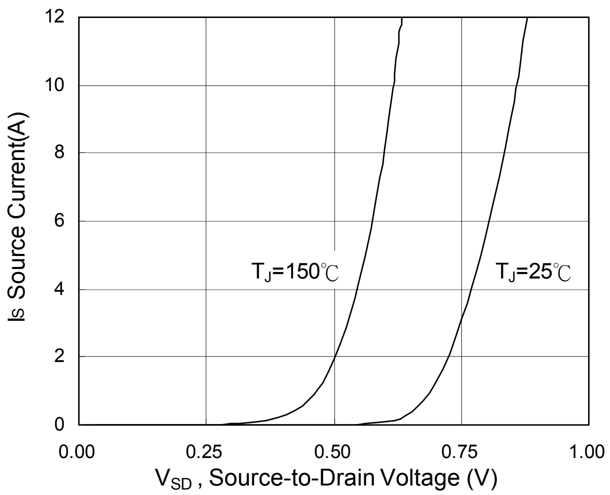


Fig.3 Forward Characteristics Of Reverse

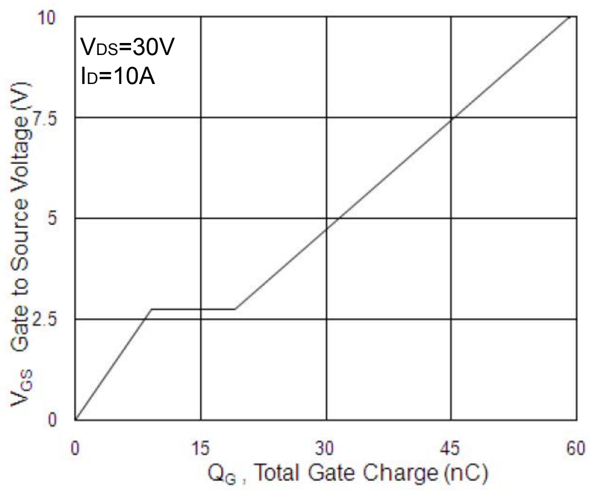


Fig.4 Gate-Charge Characteristics

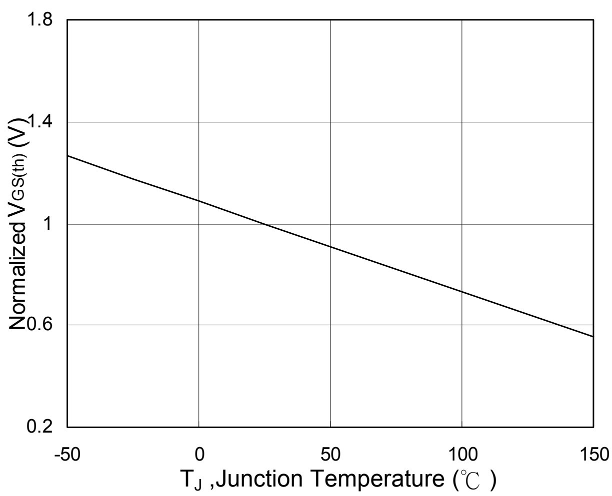


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

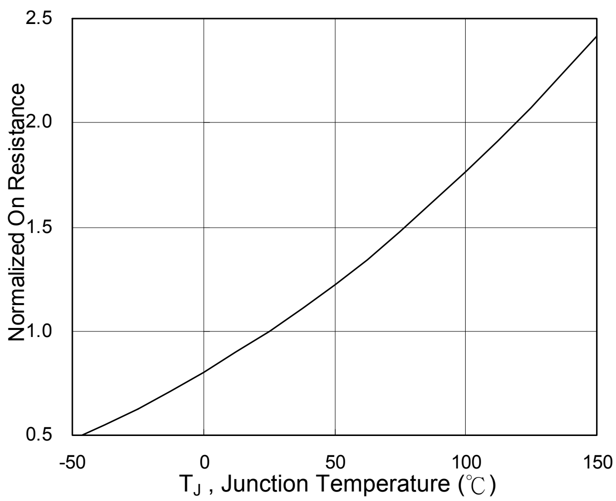


Fig.6 Normalized R_{DSON} vs. T_J

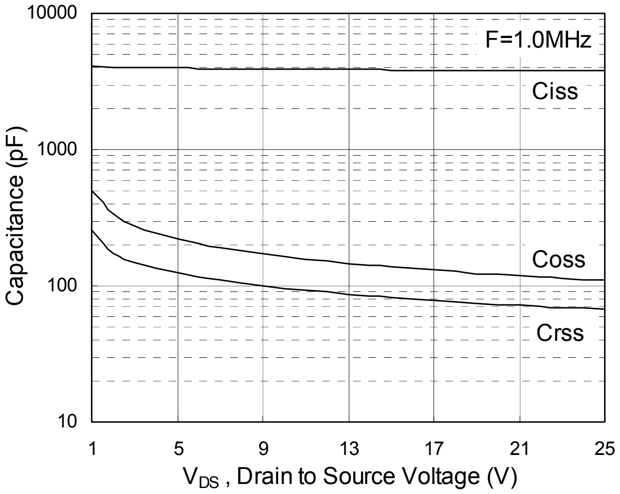


Fig.7 Capacitance

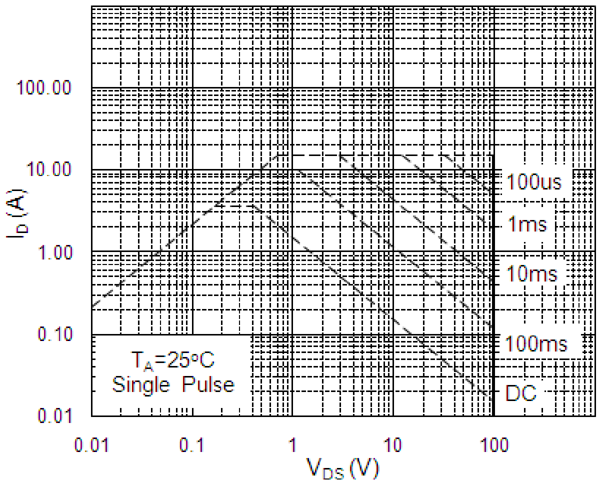


Fig.8 Safe Operating Area

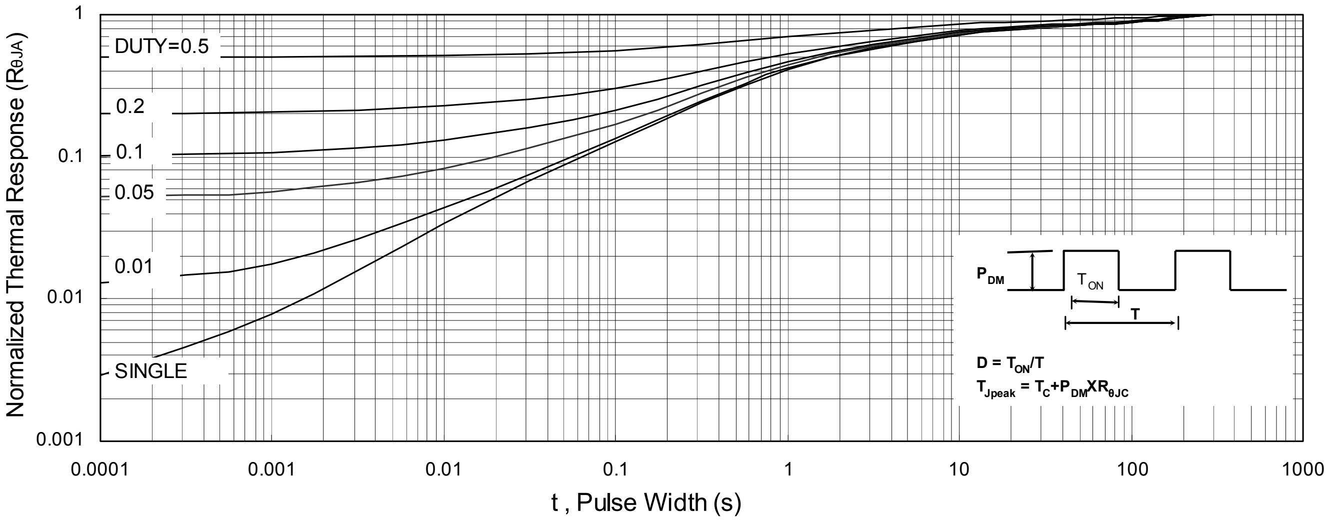


Fig.9 Normalized Maximum Transient Thermal Impedance

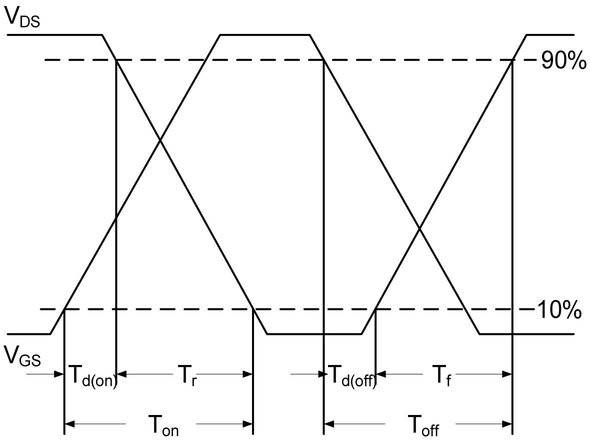


Fig.10 Switching Time Waveform

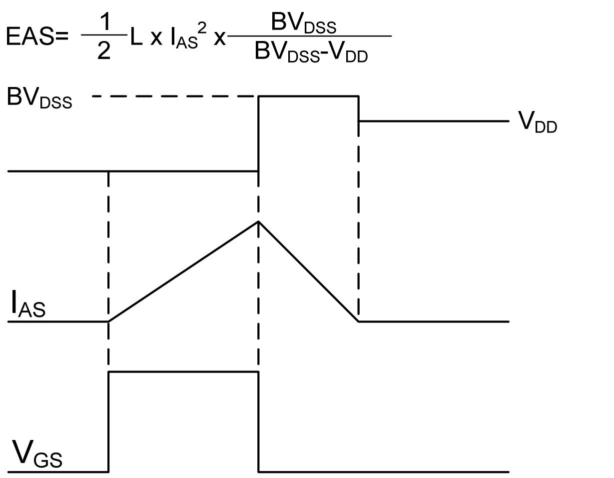


Fig.11 Unclamped Inductive Switching Waveform

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