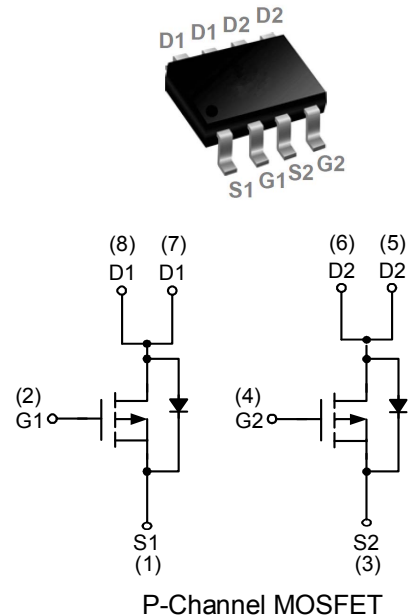


Features

- -30V/-8.9A,
 $R_{DS(ON)} = 21m\Omega(\text{max.}) @ V_{GS} = -10V$
 $R_{DS(ON)} = 32m\Omega(\text{max.}) @ V_{GS} = -4.5V$
- Reliable and Rugged
- Lead Free and Green Devices Available
 (RoHS Compliant)

Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

SOP-8 Pin Configuration

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
Common Ratings			
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 25	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	
I_S	Diode Continuous Forward Current	$T_A = 25^\circ\text{C}$ -1	A
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$ -8.9	
		$T_A = 70^\circ\text{C}$ -7.1	
I_{DM}^a	Pulsed Drain Current	$T_A = 25^\circ\text{C}$ -35	
P_D	Maximum Power Dissipation	$T_A = 25^\circ\text{C}$ 2.5	W
		$T_A = 70^\circ\text{C}$ 1.6	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	$t \leq 10s$ 50	$^\circ\text{C/W}$
		Steady State 90	
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	Steady State 20	
I_{AS}^b	Avalanche Current, Single pulse	$L = 0.1mH$ 24	A
		$L = 0.5mH$ 14	
E_{AS}^b	Avalanche Energy, Single pulse	$L = 0.1mH$ 29	mJ
		$L = 0.5mH$ 49	

Note a : Pulse width is limited by maximum junction temperature.

Note b : UIS tested and pulse width are limited by maximum junction temperature 150°C (initial temperature $T_j = 25^\circ\text{C}$).

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

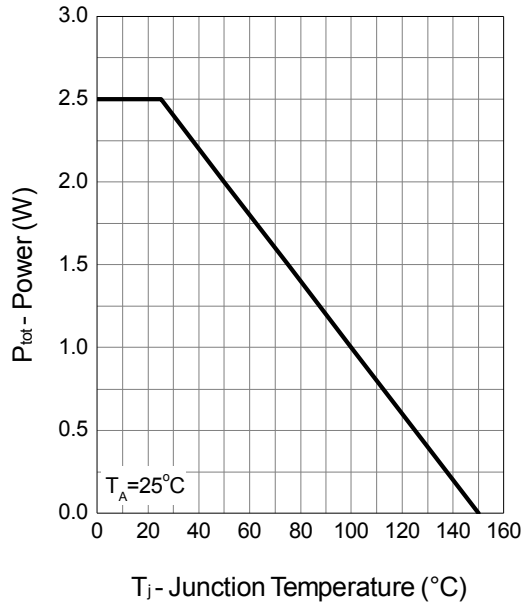
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=-250\mu A$	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0V$	-	-	-1	μA
		$T_J=85^\circ\text{C}$	-	-	-30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250\mu A$	-1.0	-1.5	-2.3	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	± 100	nA
$R_{DS(ON)}^c$	Drain-Source On-state Resistance	$V_{GS}=-10V, I_{DS}=-8.9A$	-	15	21	m Ω
		$V_{GS}=-4.5V, I_{DS}=-5.6A$	-	22	32	
Diode Characteristics						
V_{SD}^c	Diode Forward Voltage	$I_{SD}=-1A, V_{GS}=0V$	-	-0.7	-1	V
t_{rr}^d	Reverse Recovery Time	$I_{SD}=-8.9A,$	-	18	-	ns
Q_{rr}^d	Reverse Recovery Charge	$dI_{SD}/dt=100A/\mu s$	-	9	-	nC
Dynamic Characteristics^d						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$	-	3.6	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=-15V,$ Frequency=1.0MHz	-	1004	-	pF
C_{oss}	Output Capacitance		-	204	-	
C_{riss}	Reverse Transfer Capacitance		-	154	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-15V, R_L=15\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	-	8.8	-	ns
t_r	Turn-on Rise Time		-	10.4	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	35.2	-	
t_f	Turn-off Fall Time		-	46.8	-	
Gate Charge Characteristics^d						
Q_g	Total Gate Charge	$V_{DS}=-15V, V_{GS}=-10V,$ $I_{DS}=-8.9A$	-	20	-	nC
	Total Gate Charge		-	10	-	
Q_{gs}	Gate-Source Charge	$V_{DS}=-15V, V_{GS}=-4.5V,$ $I_{DS}=-8.9A$	-	3.8	-	
Q_{gd}	Gate-Drain Charge		-	5.7	-	
Q_{gth}	Threshold Gate Charge		-	1	-	

Note c : Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

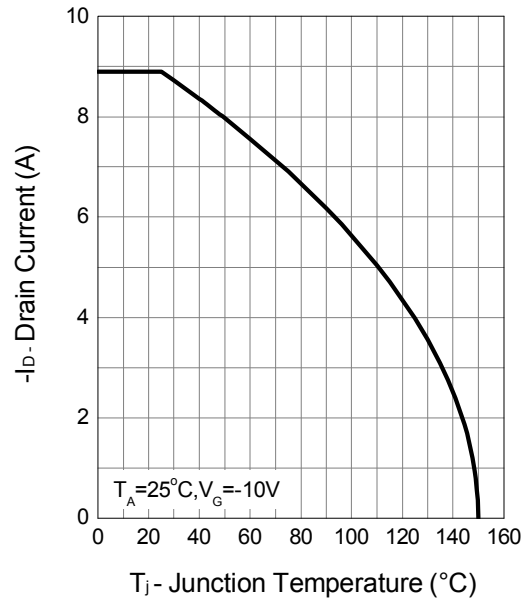
Note d : Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

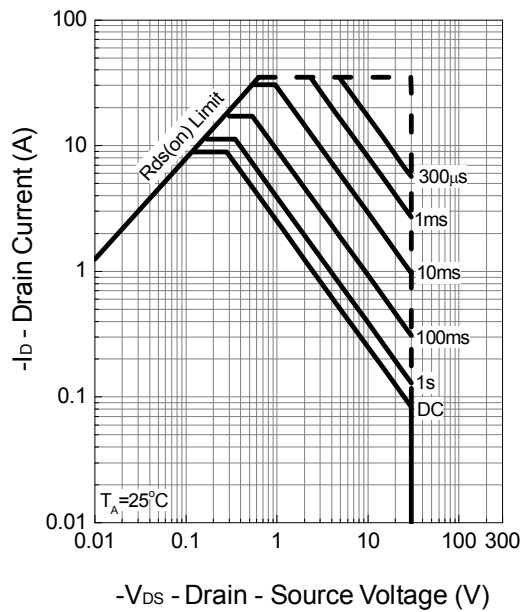
Power Dissipation



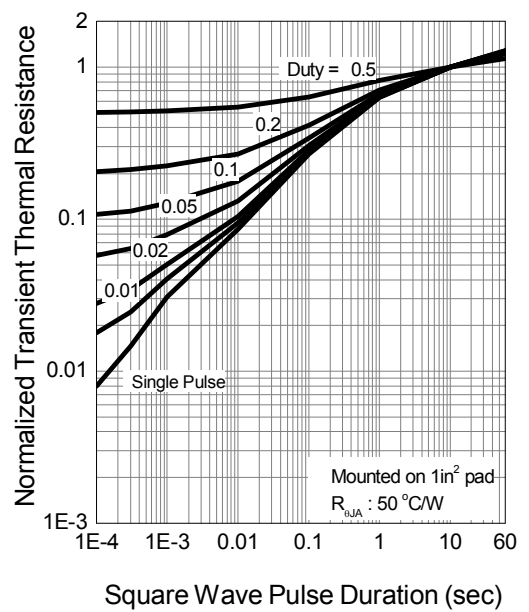
Drain Current



Safe Operation Area

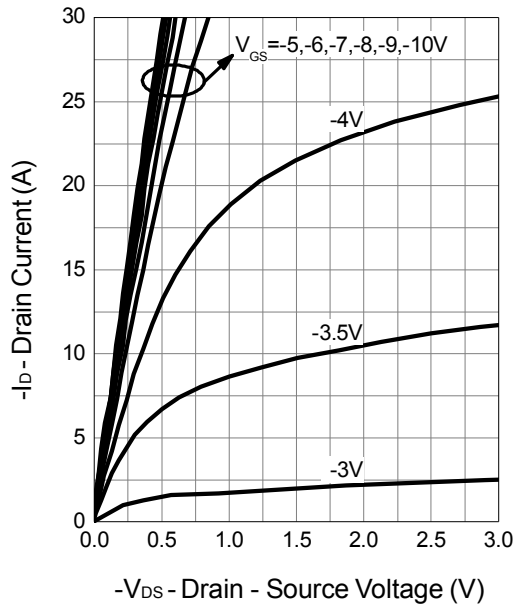


Thermal Transient Impedance

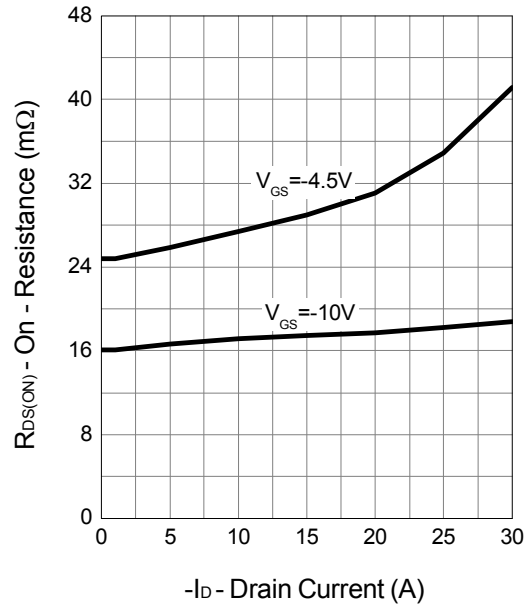


Typical Operating Characteristics (Cont.)

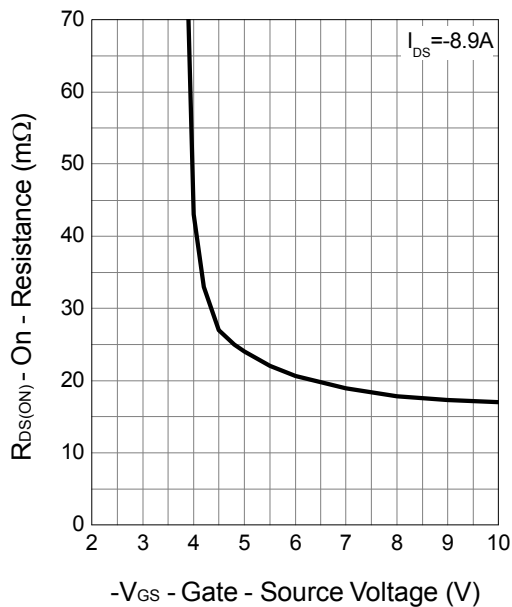
Output Characteristics



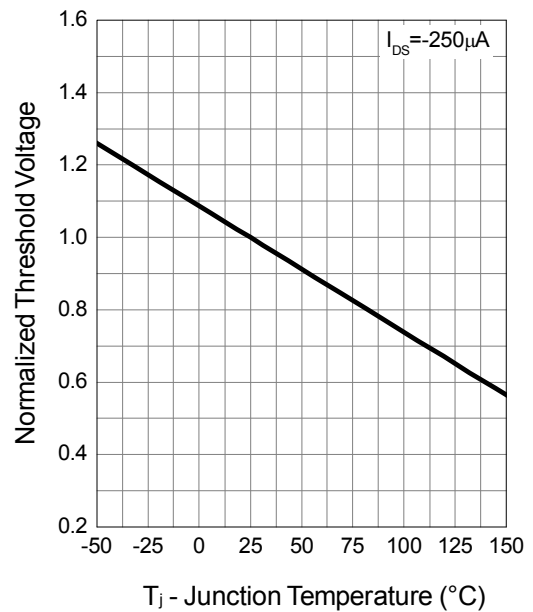
Drain-Source On Resistance



Gate-Source On Resistance

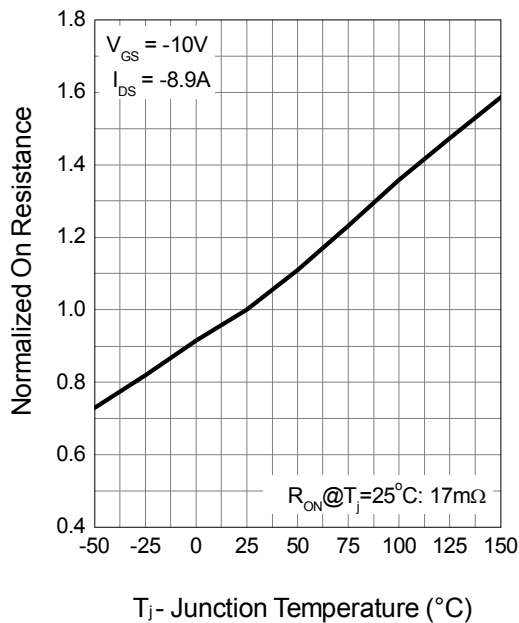


Gate Threshold Voltage

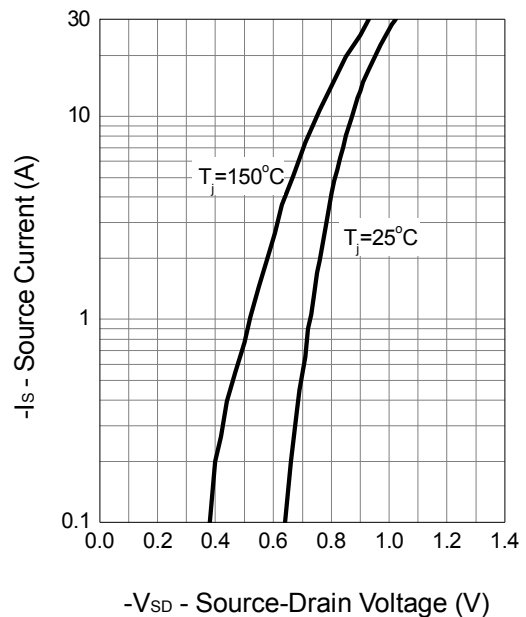


Typical Operating Characteristics (Cont.)

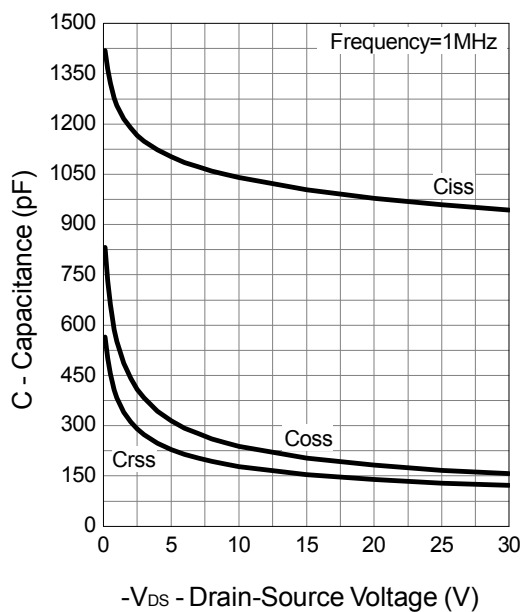
Drain-Source On Resistance



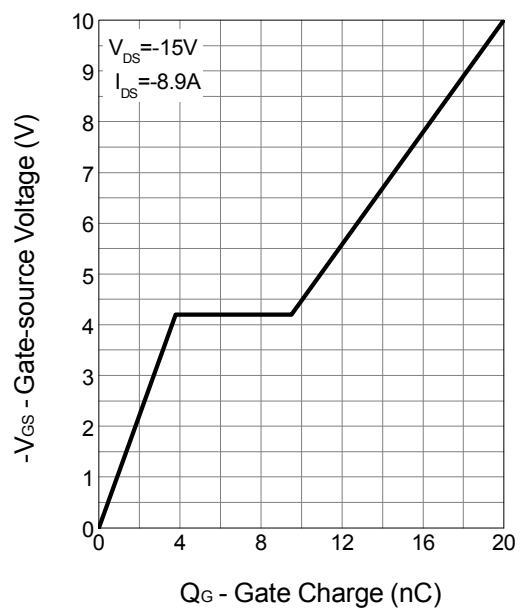
Source-Drain Diode Forward



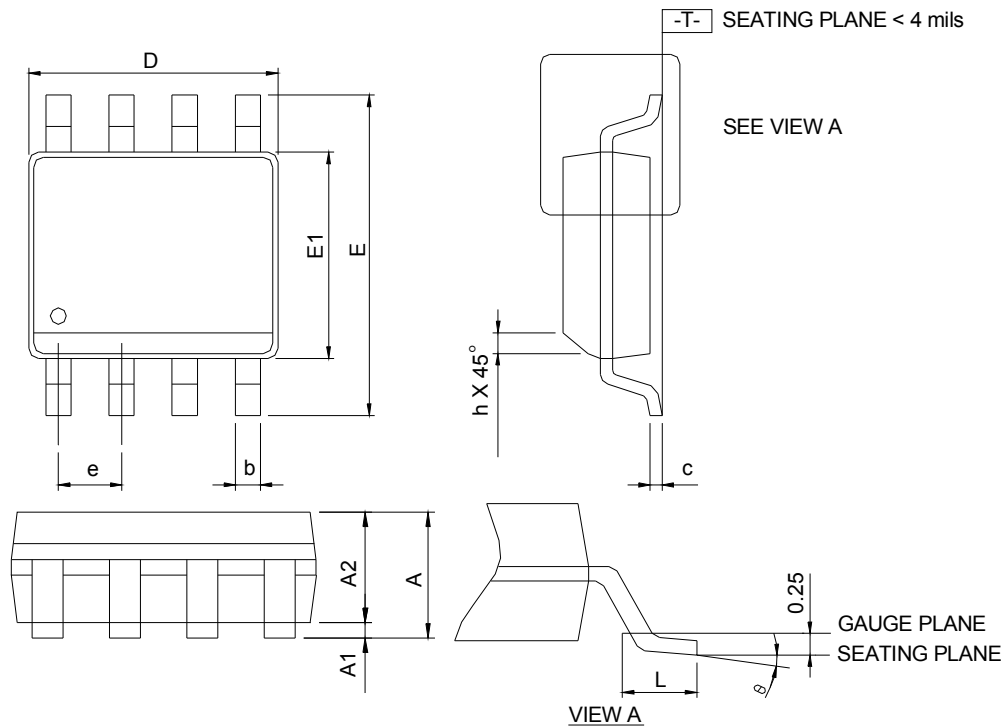
Capacitance



Gate Charge

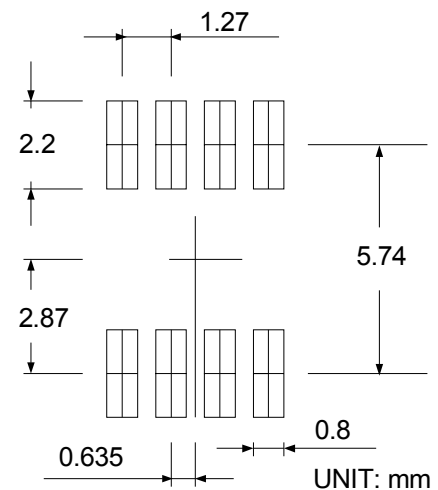


Package Information SOP-8



DIMENSIONS	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
- Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

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